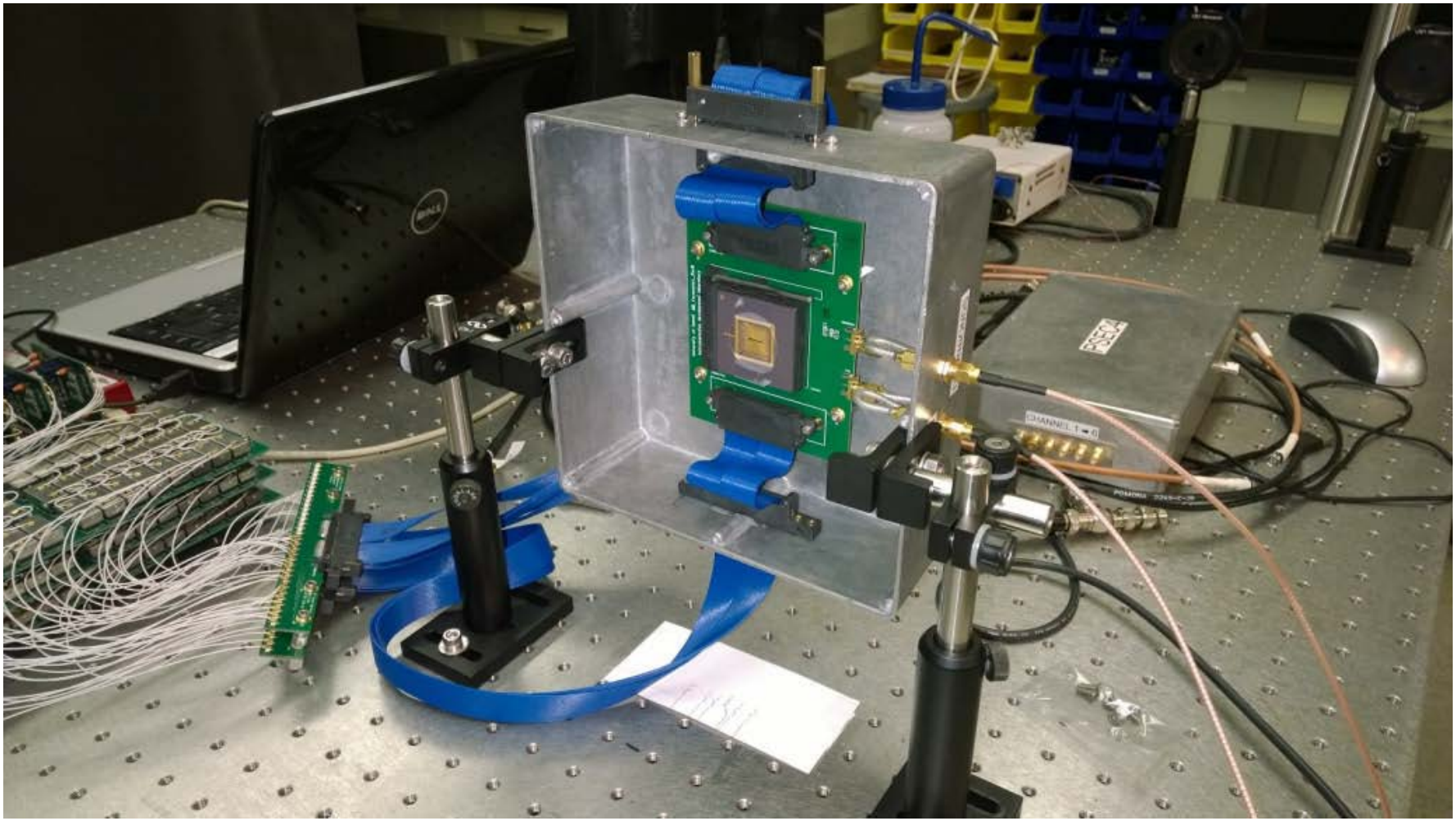
XRM Readout Upgrade



G. Varner

July 2, 2014

Current Issues / Proposal

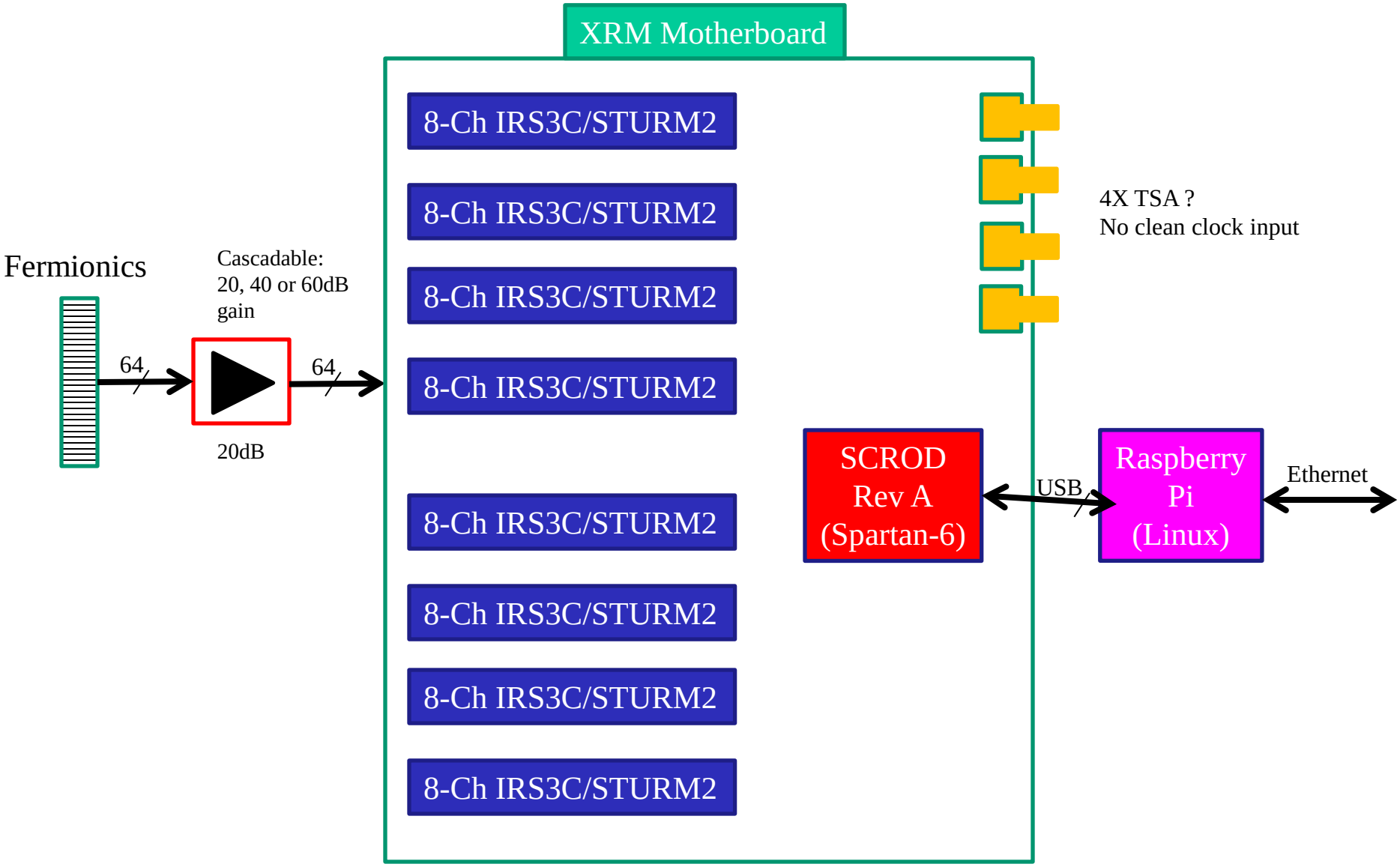
• Detector packaging, cabling, and configurable amplifier chain seems to be in reasonable shape (if a bit flying-lead)

• Readout Motherboard and clock distribution/triggering need serious restructuring

• Upgrade principles:
  - **New, independent timing input**
  - IRSX ASIC with interleaved operation
  - Modularize readout into 64 channel unit (make 2x for 128 element detector)
  - Flexible operating modes [4x BX all the time, through full orbit logging (at ~200 Hz)]

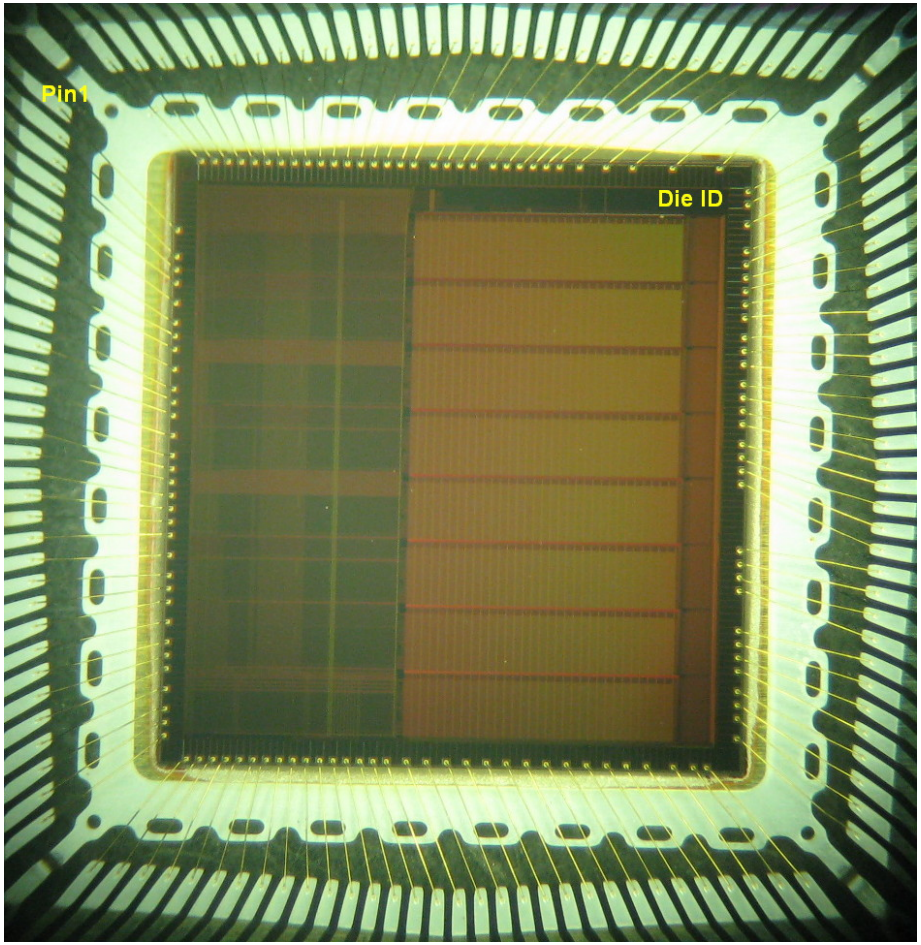
• Upgraded back-end

Current System Overview



IRSX ASIC

• Baseline Belle II iTOP ASIC for production (~670 were fabricated in pre-production run [March 2014])



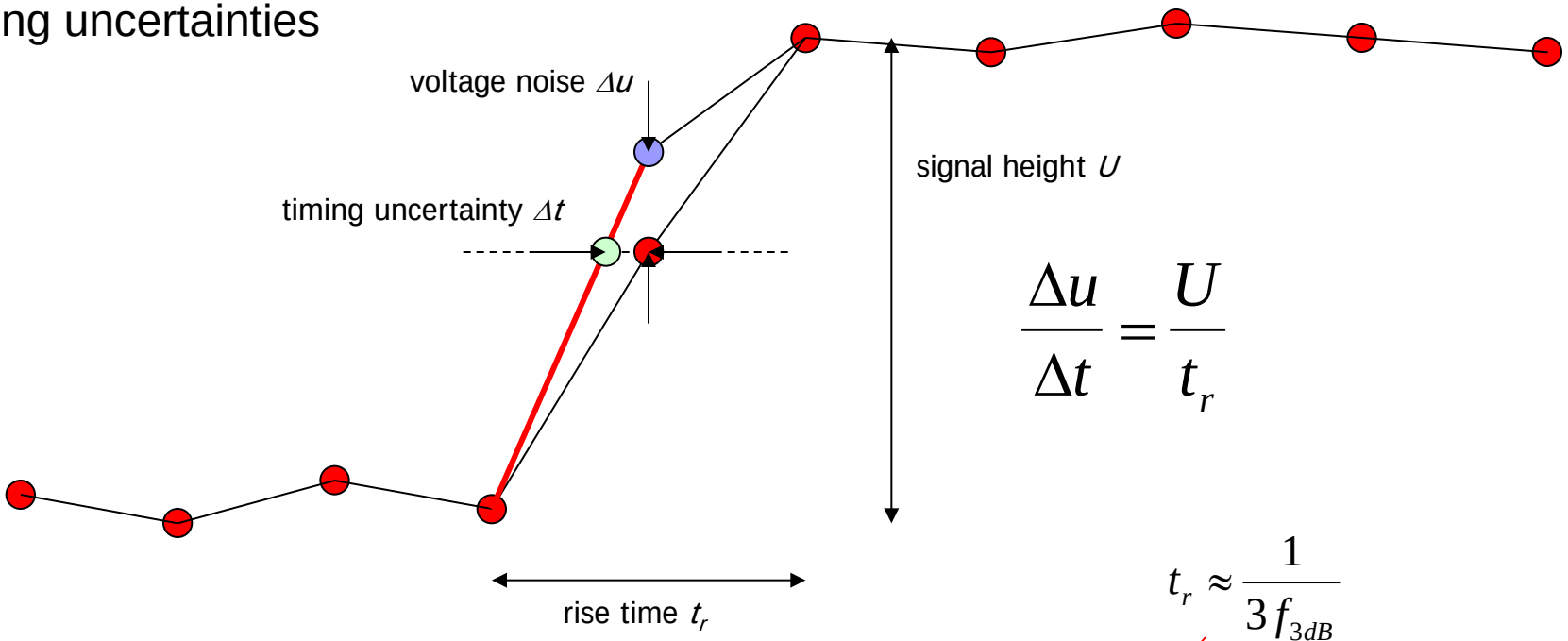
2.6M transistors, 7.7k resistors (DACs)

• High-speed, lower power/EMI LVDS outputs for fast, asynchronous signals
• Extended dynamic range comparator
• Lower-power Gray Code Counter and internal DLL
• Hardware timebase correction

Calibration and Sources of Timing Error

Contributions to timing resolution:

- Voltage uncertainties
- Timing uncertainties



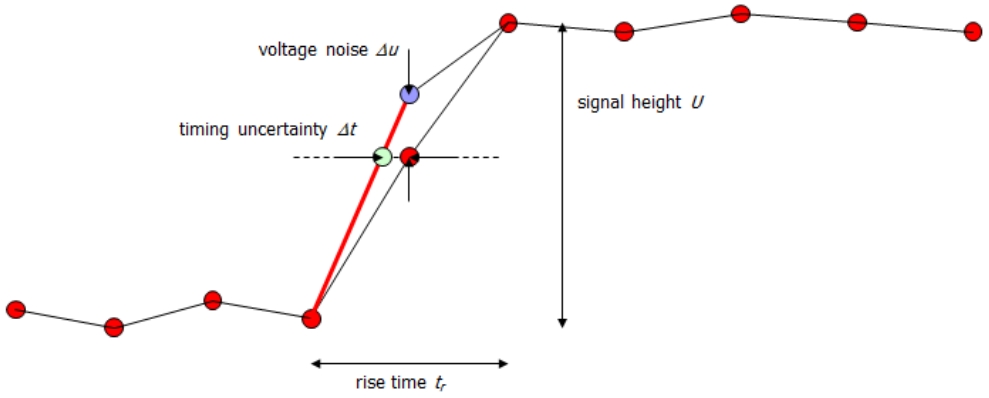
$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}$$

$$t_r \approx \frac{1}{3 f_{3dB}}$$

$$\Delta t = \frac{\Delta u}{U} \cdot t_r = \frac{\Delta u}{U\sqrt{n}} \cdot t_r = \frac{\Delta u}{U} \cdot \frac{t_r}{\sqrt{t_r \cdot f_s}} = \frac{\Delta u}{U} \cdot \frac{\sqrt{t_r}}{\sqrt{f_s}} = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

*Diagram, formulas from Stefan Ritt

Calibration and Sources of Timing Error

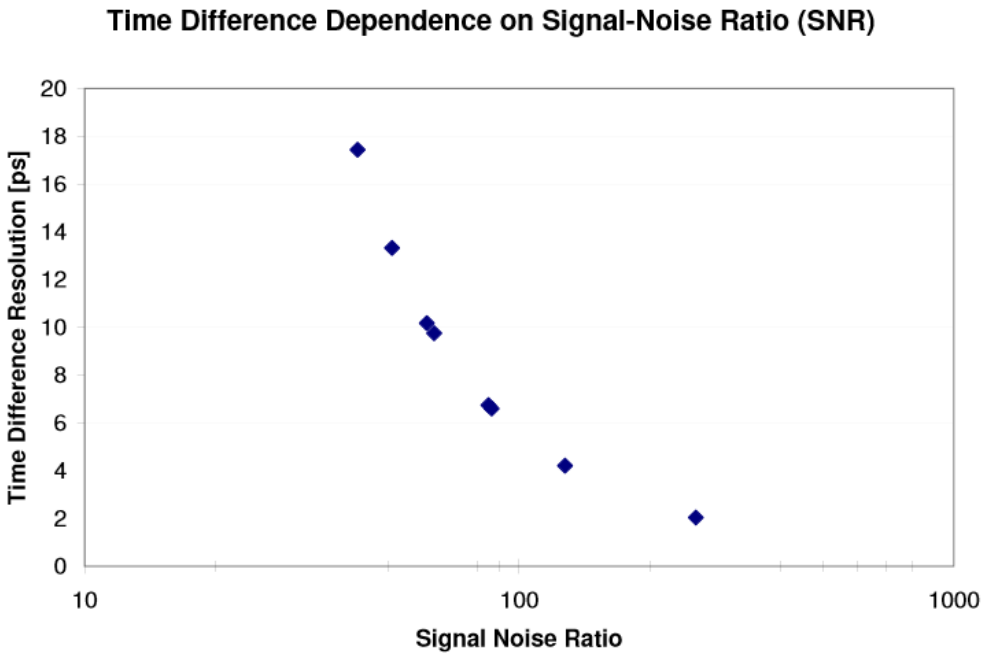


$\Delta u = 2mV$

$U = 1V$

$f_s = 26$ GSPS

$f_{3dB} = 1.2GHz$

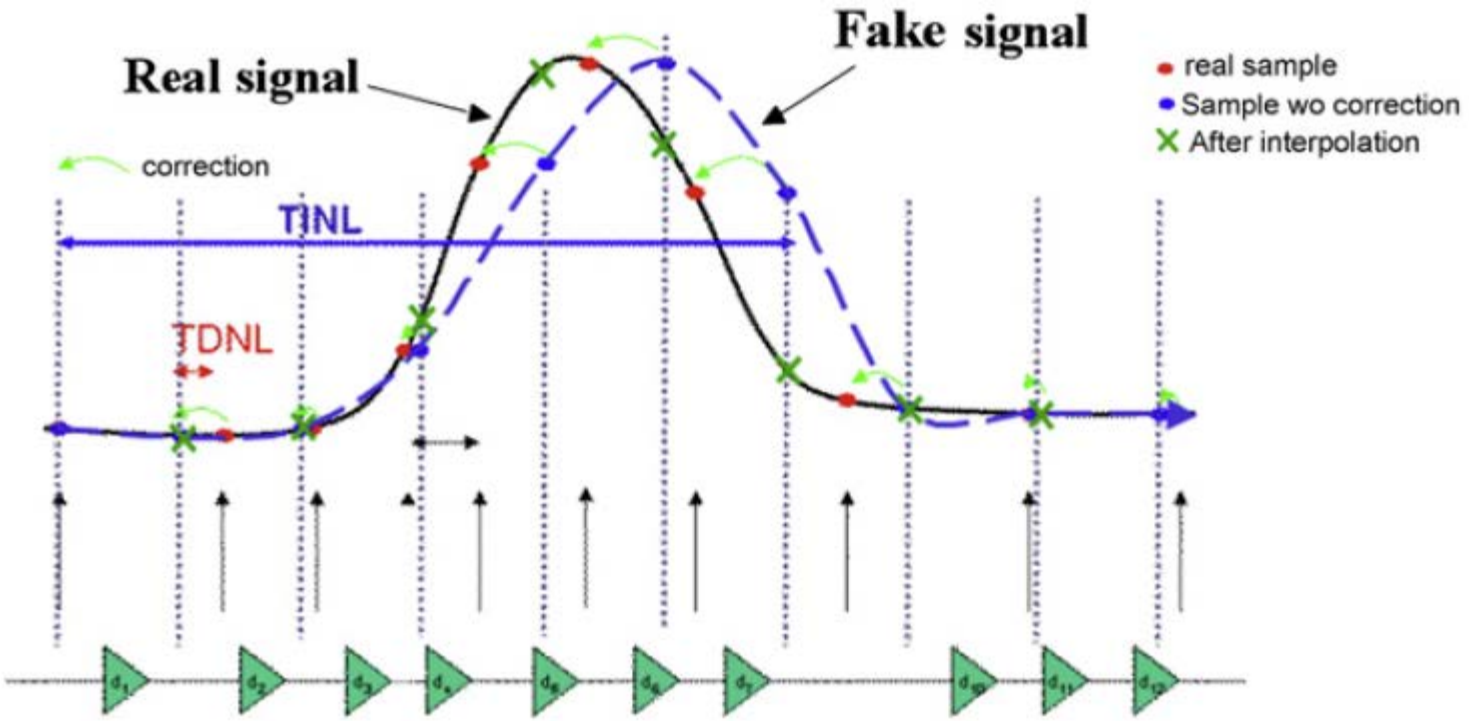


$$\frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}} \sim 200 \text{ fs}$$

Aperture stability is key

Timing Uncertainties and Timing Calibration

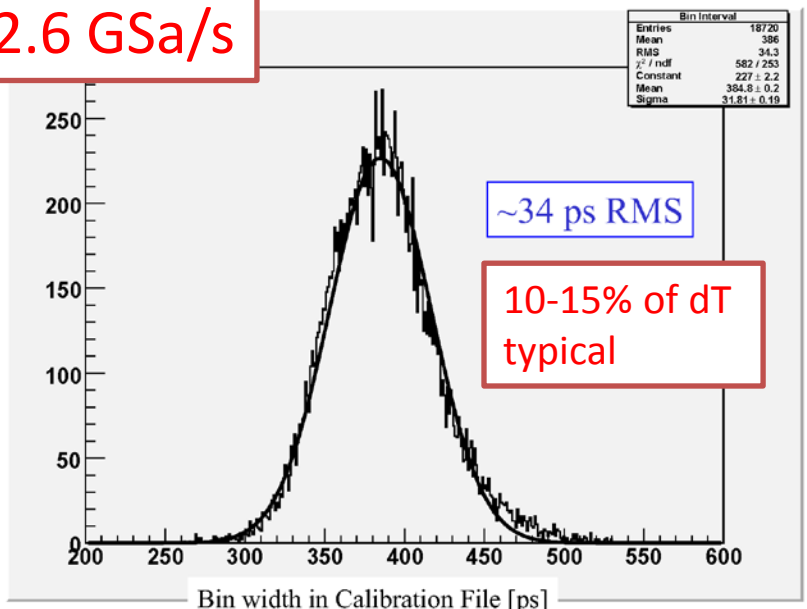
- Time interval between delay line stages has intrinsic variation.
- Not accounting for this properly causes significant timing error



Nuclear Instruments and Methods in Physics Research A 629 (2011) 123–132

Time base non-uniformity…

2.6 GSa/s



If can correct, reduces processing time dramatically, as this is the most computationally-intensive aspect of "fast feature extraction"

IRSX Improvements over IRS3C/STURM2

1. Improved Trigger Sensitivity*
2. Timebase Servo-locking
3. dT hardware adjust
4. Improved linearity/dynamic range
5. Improved Wilkinson ADC

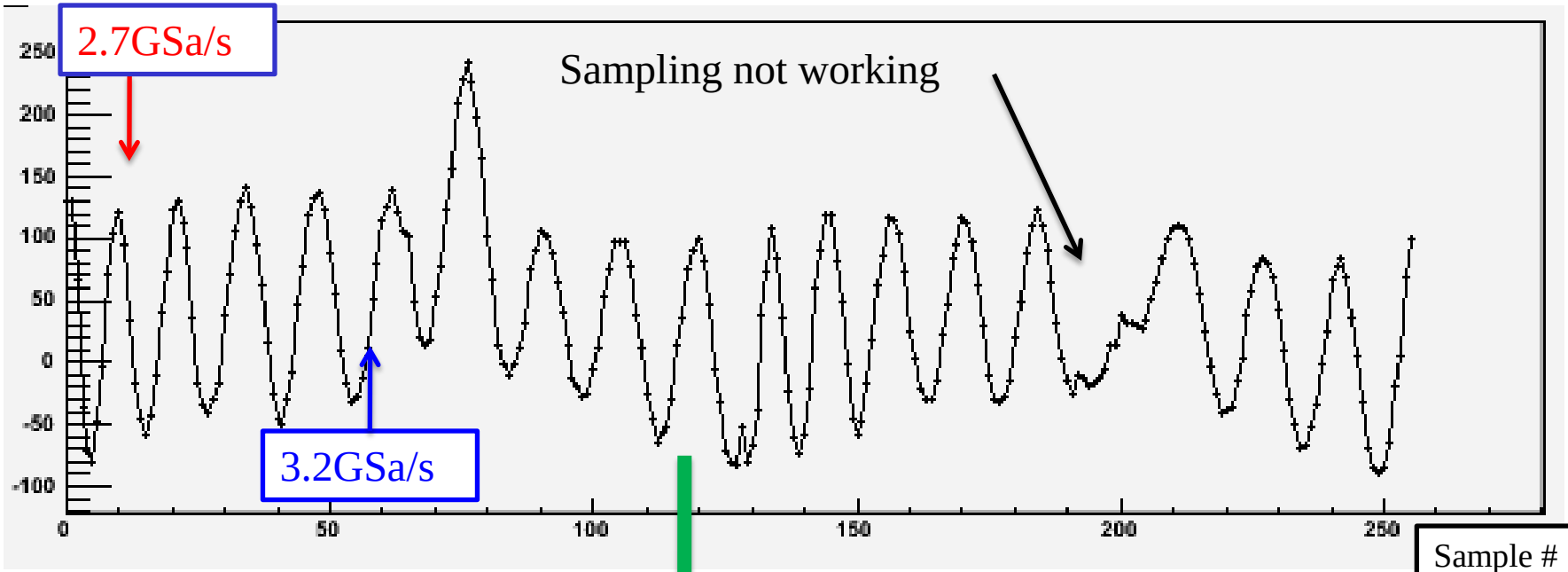
* (not relevant for XRM)

= originally reported for TARGET7/X

= demonstrated initially (TARGET7/X), detailed timing confirmed

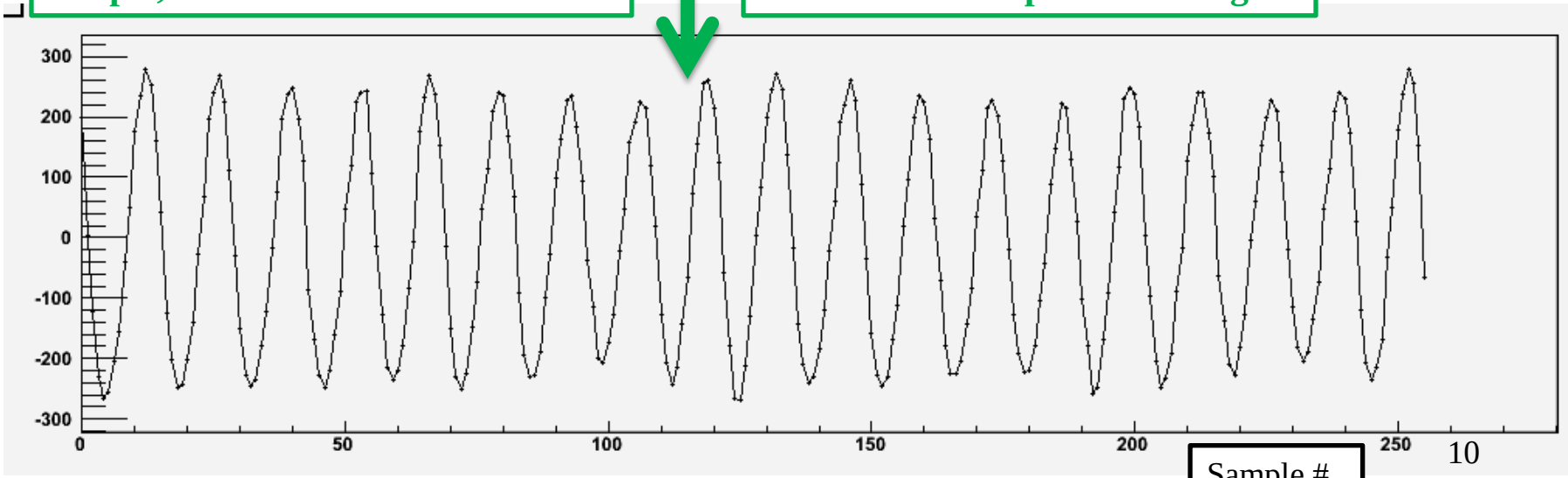
= IRS3D, LABRADOR4 also

Roughly Adjusted dT Sampling

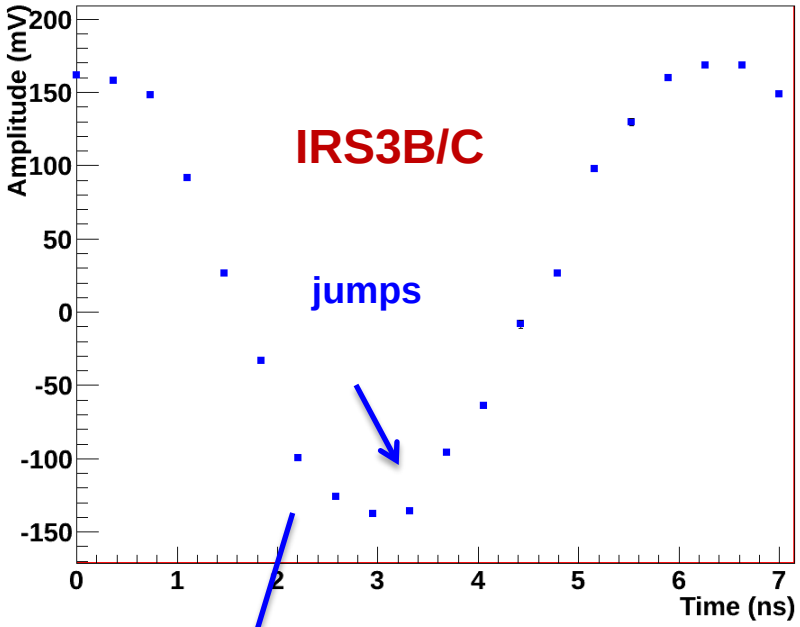


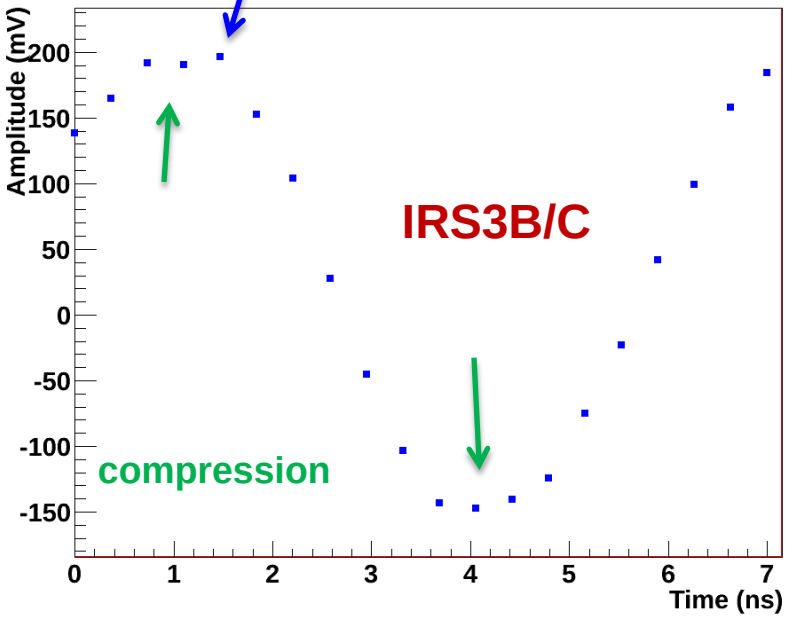
Simple, linear dT slew correction

Still room for improved tuning

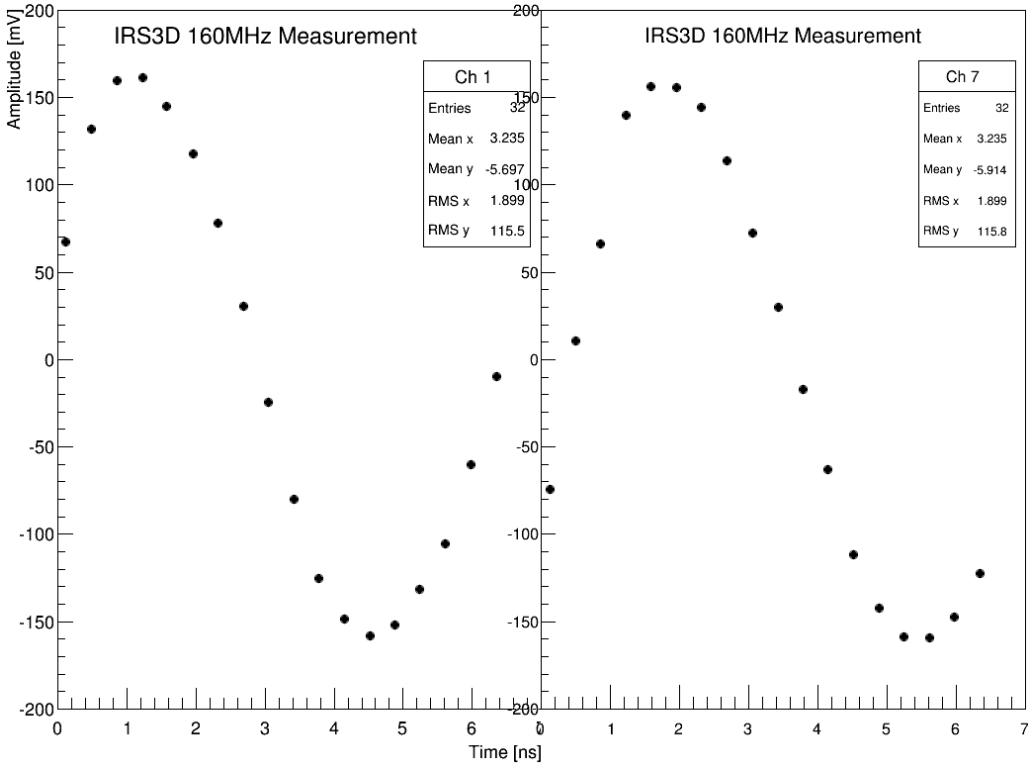


Result: visually nicer waveforms



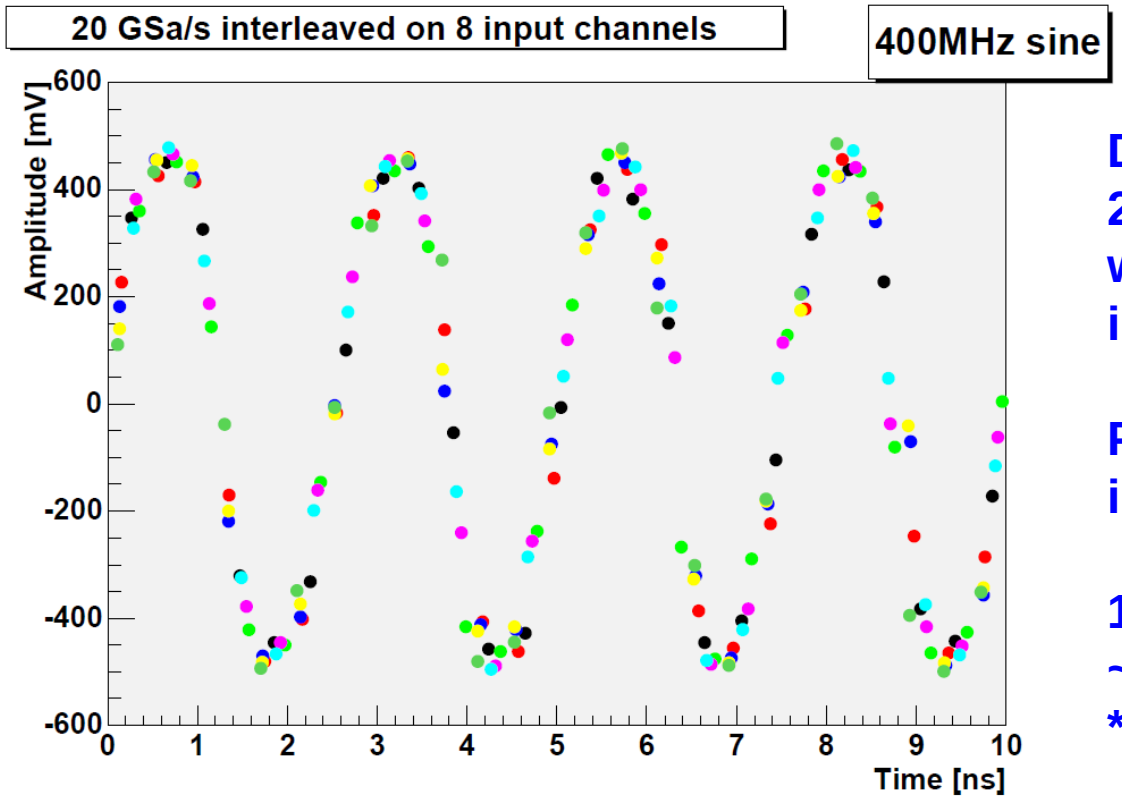


Difference most evident at the extrema of the waveforms



IRS3D

Interleaved Operation



Demonstrated this back in 2006, but wasn't practical without ability to trim the individual delays (dT's)

Propose to run IRSX in interleave-by-8 mode

10μs orbit / 32,768 samples
~3.3 GSPS
***8 ~ 26 GSPS**

Fig. 23. Example of 20GSa/s interleaved, single-shot waveform recording of a 400MHz sine wave signal on 8 LAB3 input channels, each plotted with a different color.

The large analog bandwidth recorder and digitizer with ordered readout (LABRADOR) ASIC
G.S. Varner, L.L. Ruckman, (*et al.*), Nucl.Instrum.Meth. **A583** (2007) 447-460.

Precision timing distribution

- Belle II FTSW as model for programmable timing module to generate clean copy of SuperKEKB clock
- Bunch ID/revolution marker synchronization
- Use clock jitter cleaner for <1ps jitter

20110805 version

Timing signals over CAT7 cables

7 ports, O1 to O7

- ACK → ACK: 254 Mbps serialized, unused
- TRG ← TRG: 254 Mbps serialized
- RSV ← RSV: pulled down to GND
- CLK ← CLK: 127 Mhz

JTAG signals over CAT7 cables

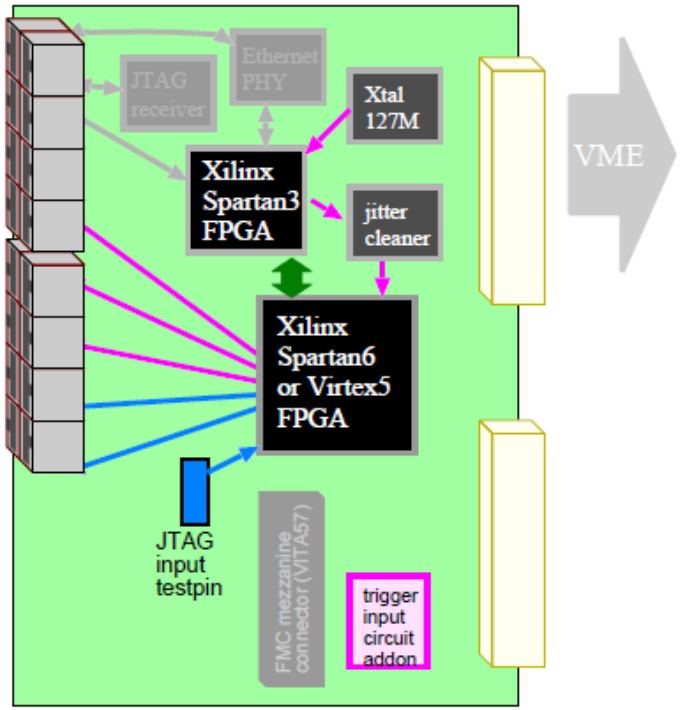
4 ports, O9 to O12

- TCK ←
- TMS ←
- TDI ←
- TDO →

Monitoring signals over a CAT7 cable

AUX port

- trgin ← copy of trigger input
- trg21 ← latched with 21MHz clock
- trgpulse ← trgin and (not trg21)
- clk21 ← 21MHz clock



Don't go through FPGA!!

Micro-TCA

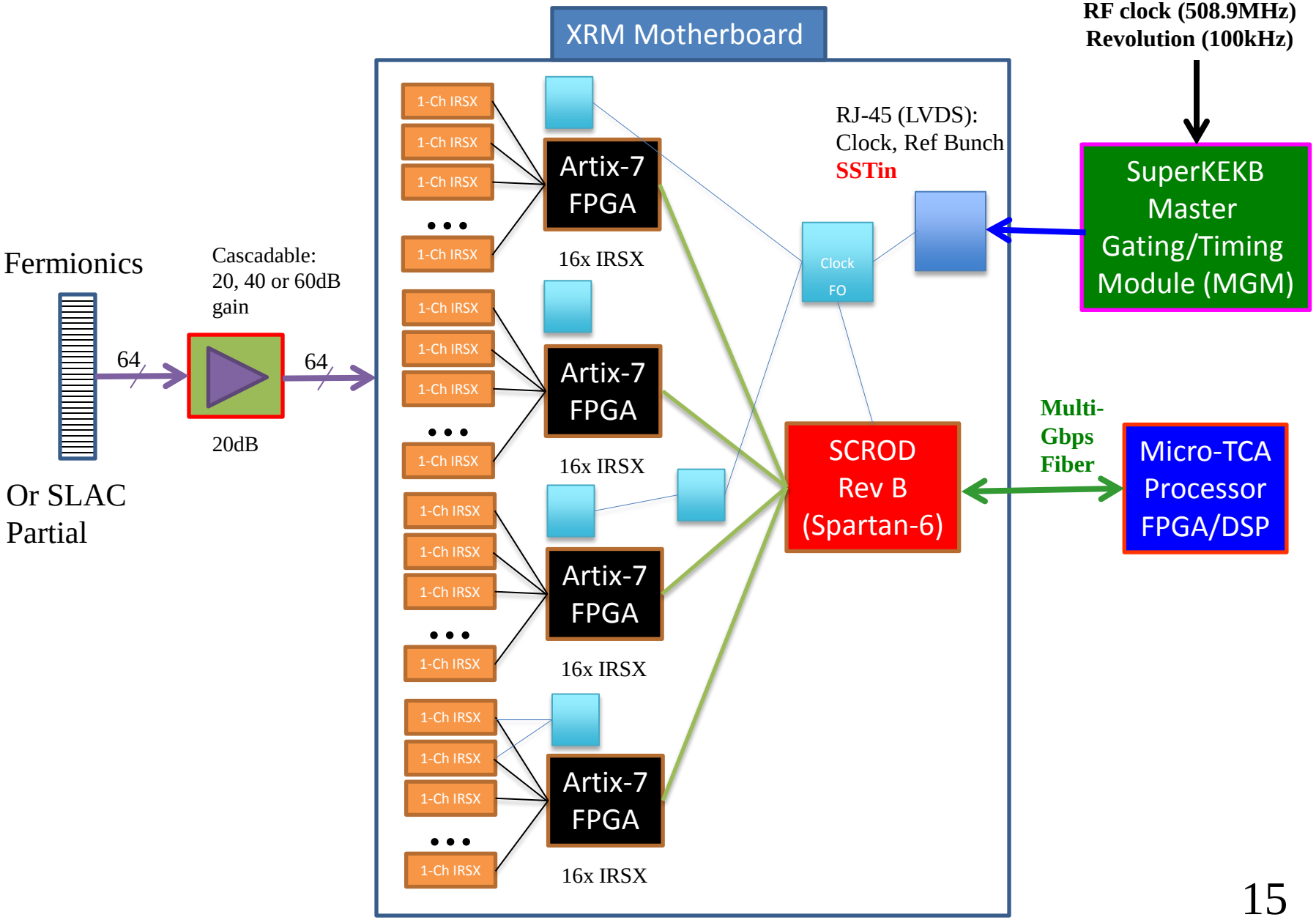
- Based upon advanced TeleCom standard, but a light version, preferred by particle physics community
- Designed for intensive signal processing/handling
- Engineered from the start for extremely high reliability and performance

2U height, 19” rack-mount ($3,750)

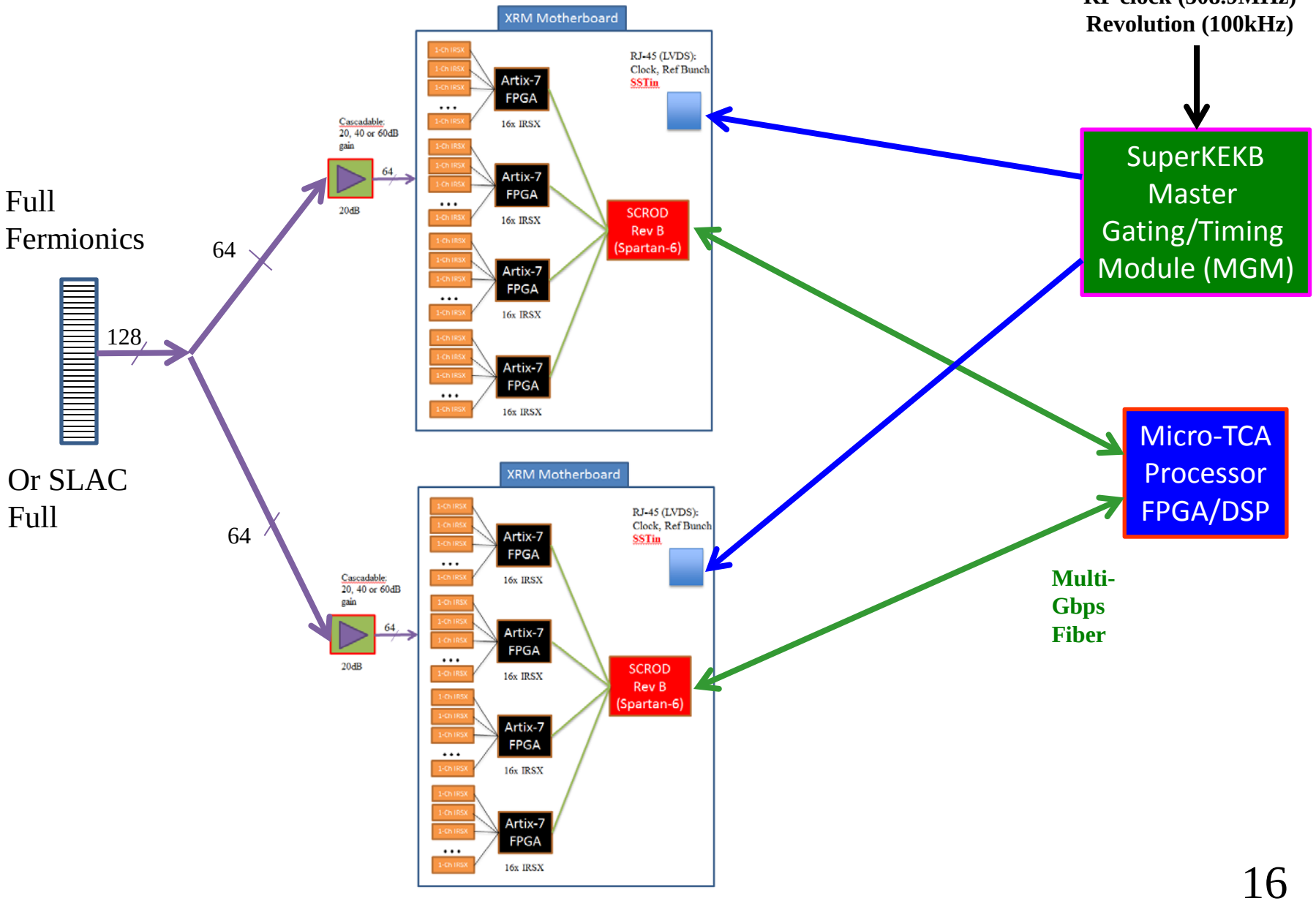
mTCA Hub Controller ($5,341)

CPU (Intex Xeon E3) ($3,360)

Revised System Overview



Revised Full System Overview



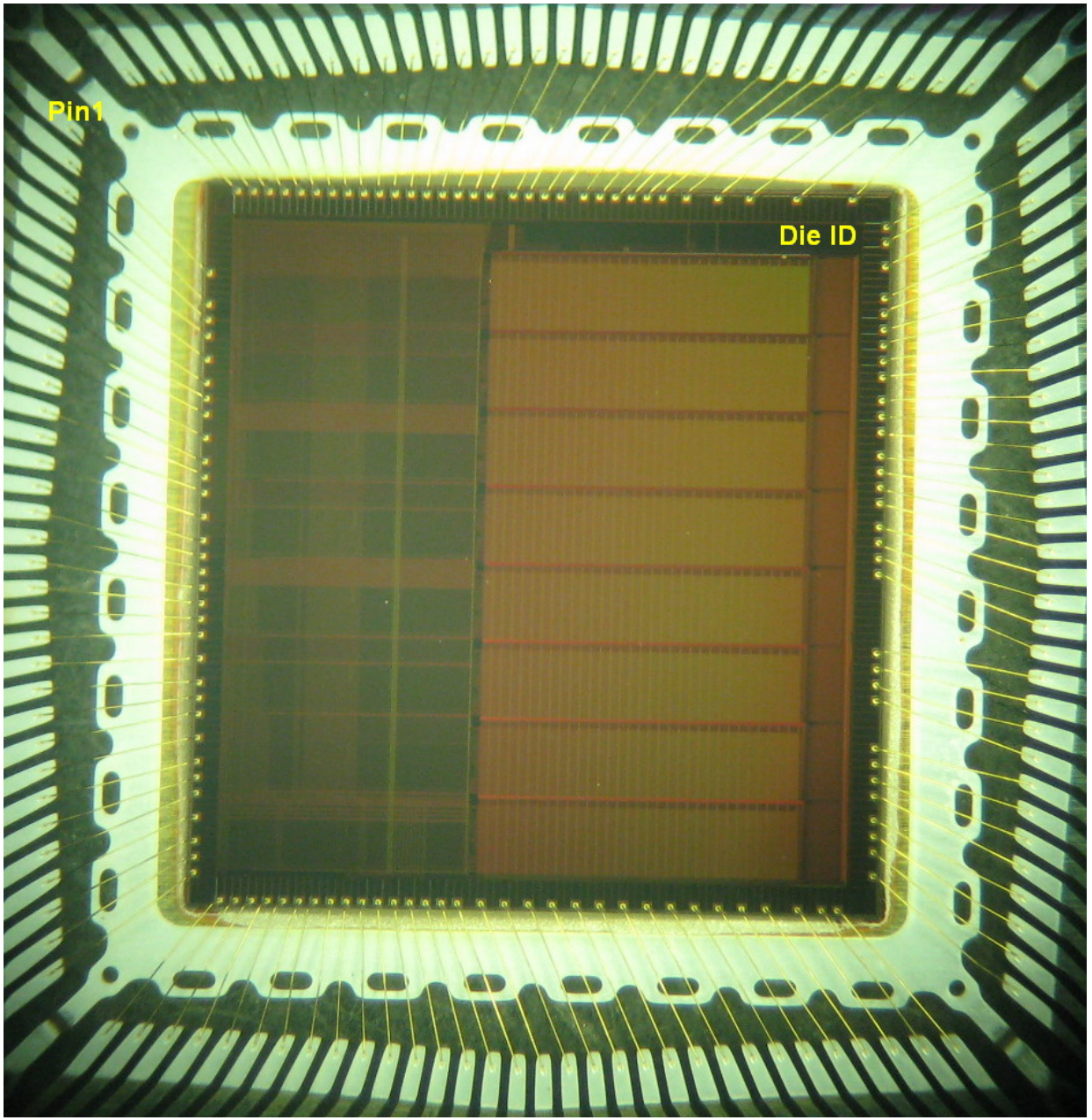
Summary

- Final system specifications/configuration
  - **Becoming clearer**
  - **Leverage ASIC, FPGA/firmware development**
  - **Upgrade back-end processing power**

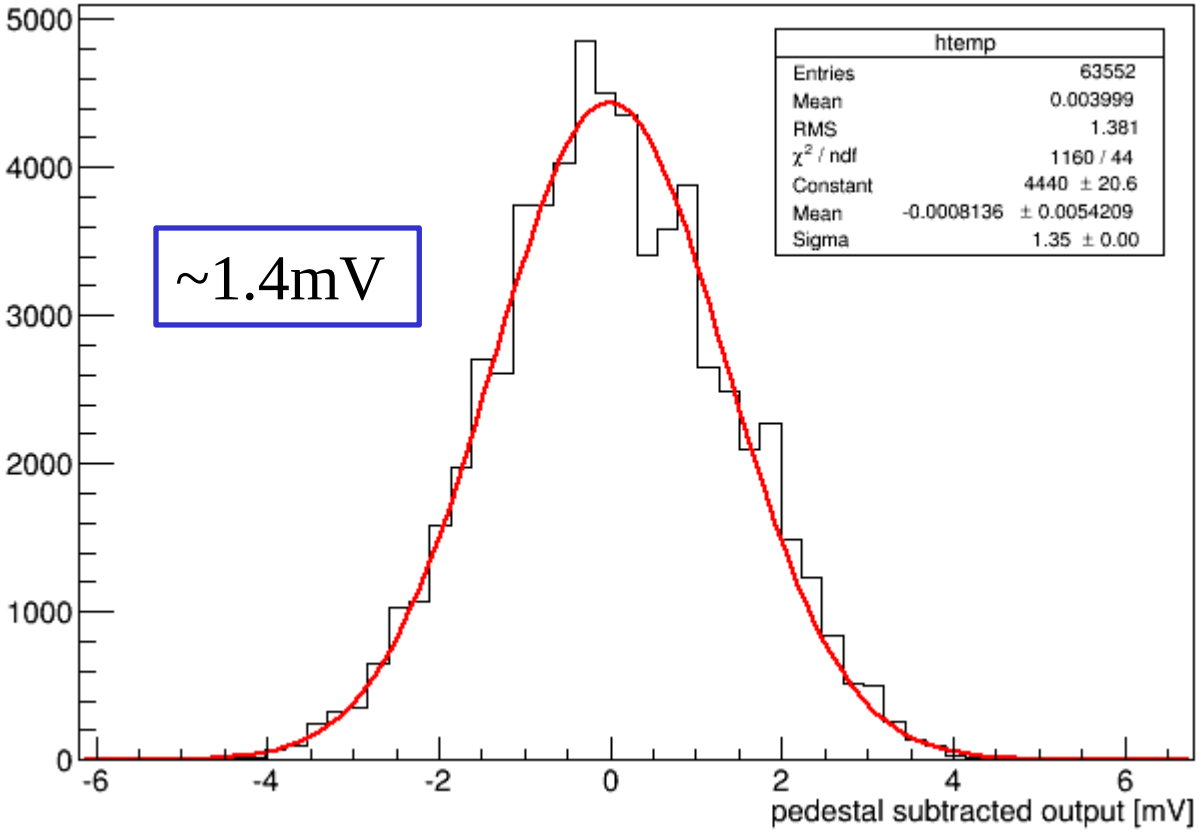
- **Next actions:**
  - **Design and prototype Timing Distribution module**
  - **New IRSX daughtercard prototype**
  - **Start revised Motherboard design for SCROD Rev. B**
  - **Track progress – Jussi back next week**

- **This is the system we plan to use for first phase of SuperKEKB operation (both Fermionics and new SLAC detector)**

Back-up slides



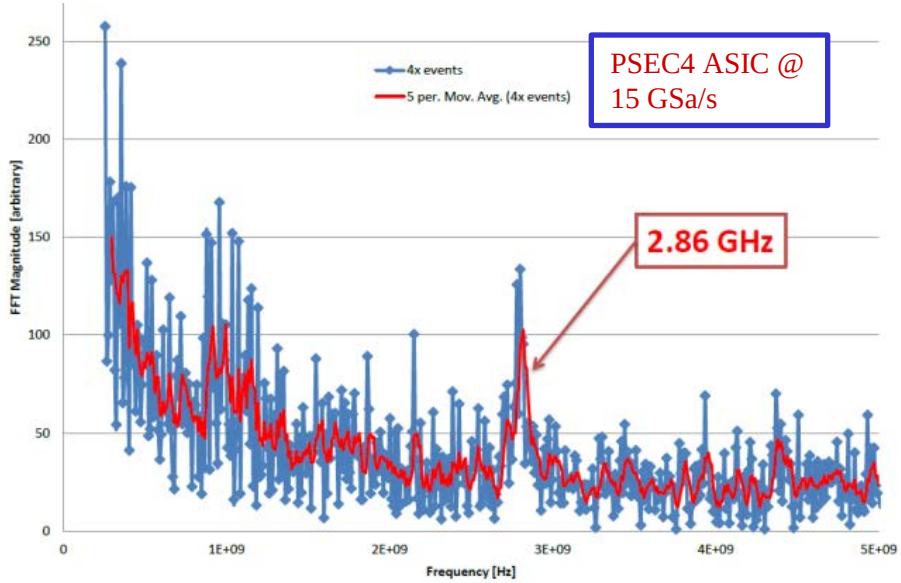
Observed IRSX noise



Non-gaussian distributions expected for small noise amplitude due to non-linearity in Gray-code least count

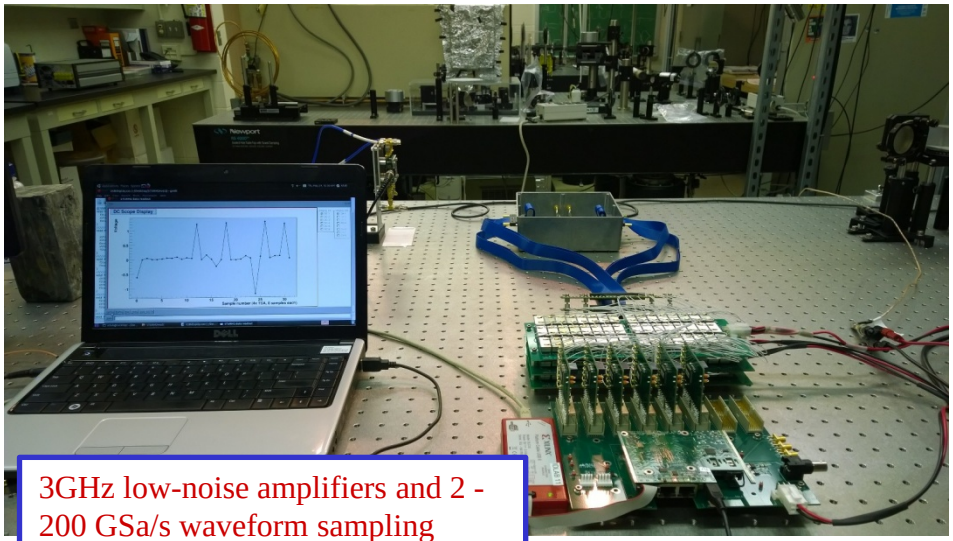
Take away message: noise is comparable, or better than IRS3B/C, and acquired while sampling continues to run

Ongoing Evaluation Program



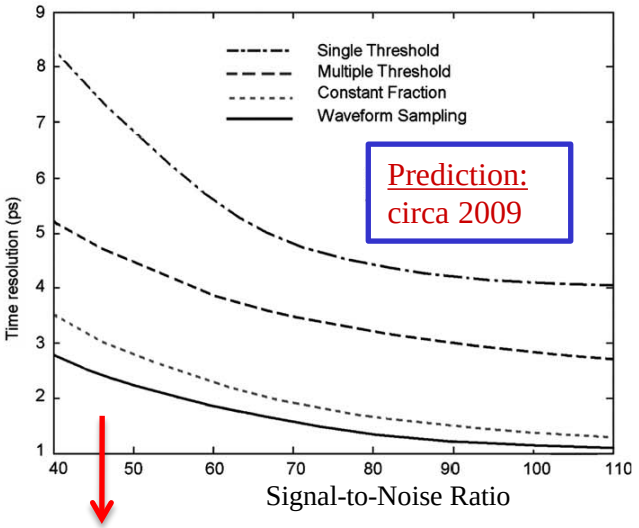
PSEC4 ASIC @ 15 GSa/s

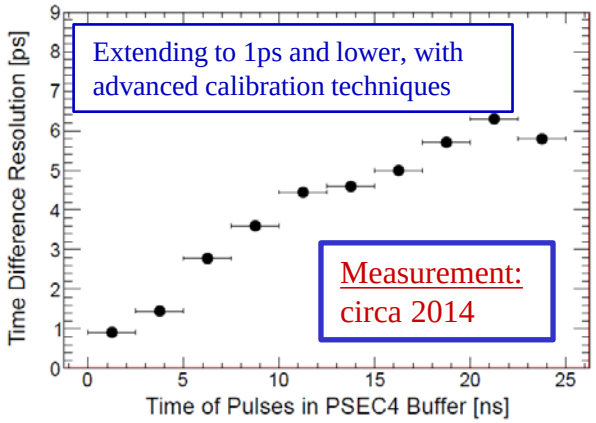
Detectors and readout with pico-second Timing and µm spatial resolution



3GHz low-noise amplifiers and 2 - 200 GSa/s waveform sampling

In a number of communities, a growing interest in detectors capable of operating at the pico-second resolution and µm spatial resolution limit (for light 1 ps = 300 µm)





Front-End Electronics