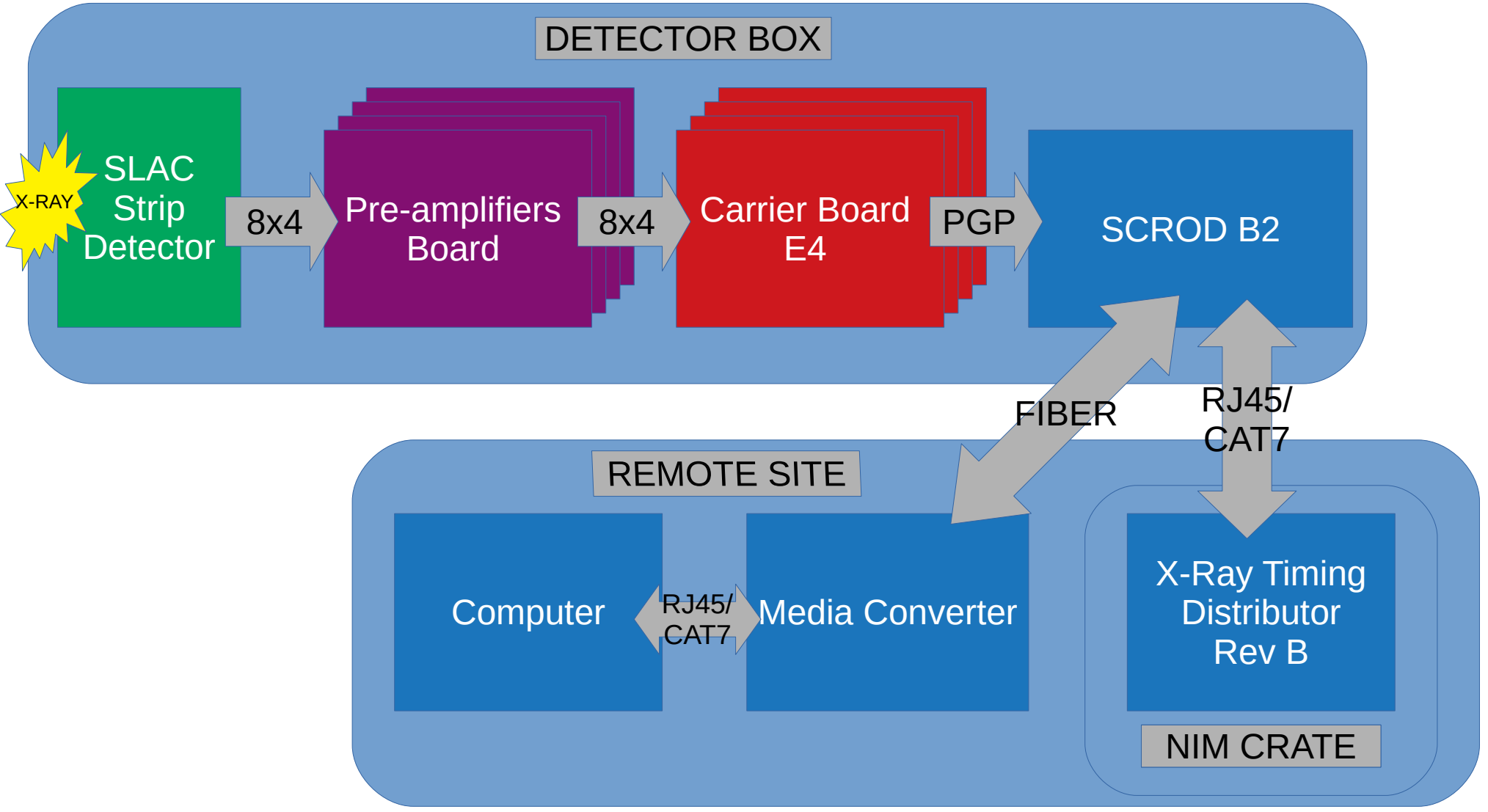
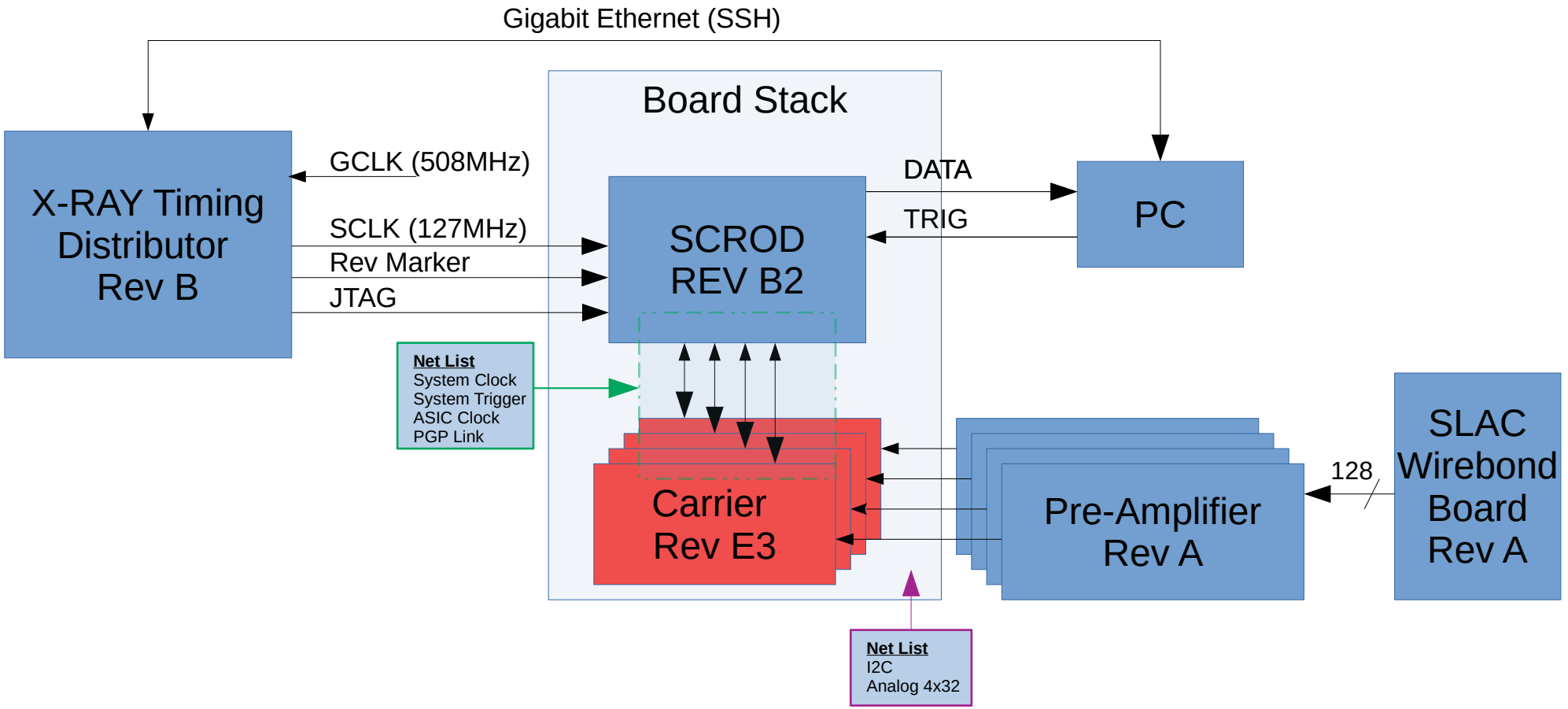
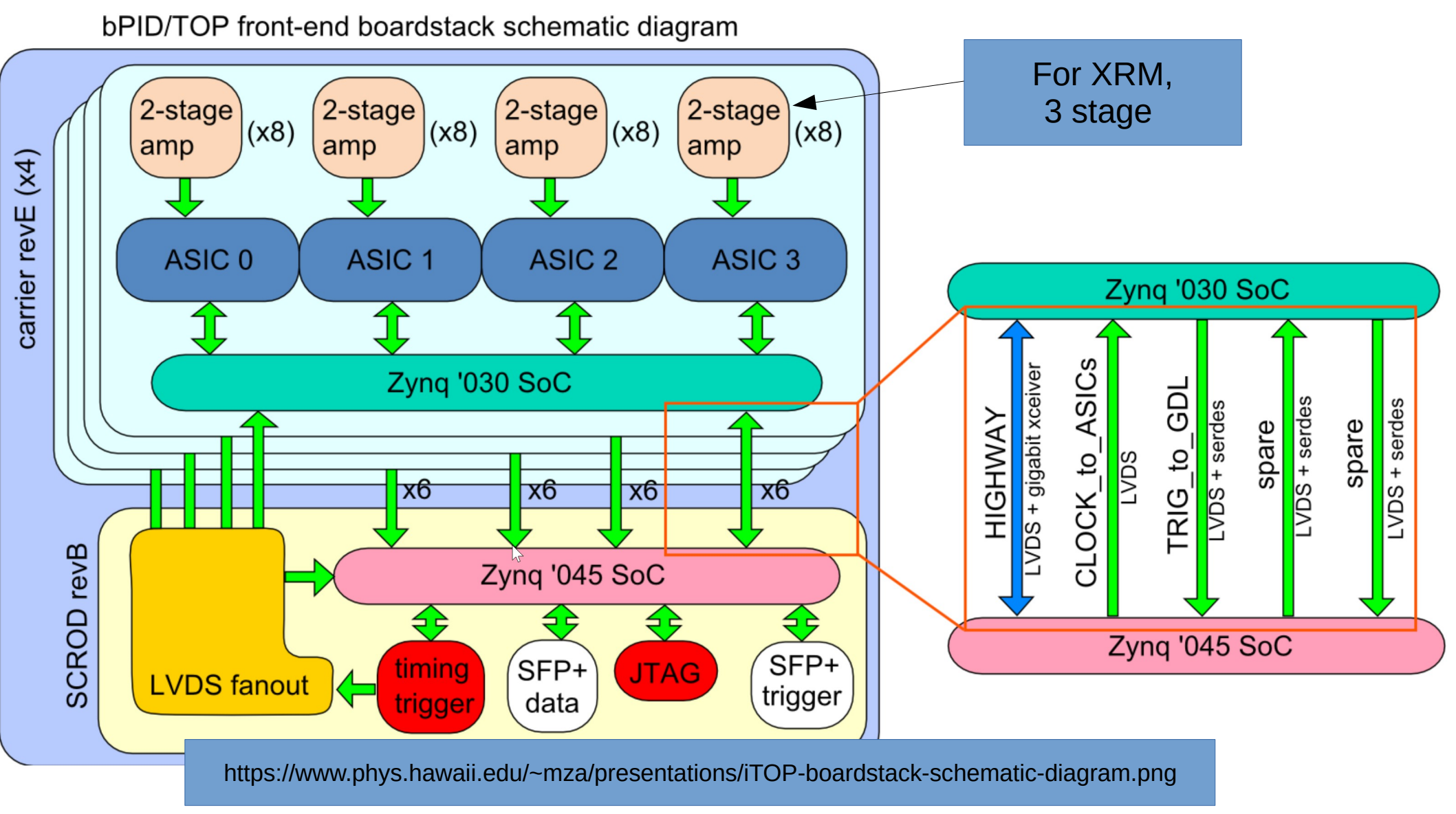

DETECTOR BOX
X-RAY
SLAC
Strip
Detector
8x4
Pre-amplifiers
Board
8x4
Carrier Board
E4
PGP
SCROD B2
FIBER
RJ45/
CAT7
REMOTE SITE
Computer
RJ45/
CAT7
Media Converter
X-Ray Timing
Distributor
Rev B
NIM CRATE


Gigabit Ethernet (SSH)
Board Stack
X-RAY Timing
Distributor
Rev B
GCLK (508MHz)
SCLK (127MHz)
Rev Marker
JTAG
SCROD
REV B2
DATA
TRIG
PC
Net List
System Clock
System Trigger
ASIC Clock
PGP Link
Carrier
Rev E3
Pre-Amplifier
Rev A
128
SLAC
Wirebond
Board
Rev A
Net List
I2C
Analog 4x32


bPID/TOP front-end boardstack schematic diagram
For XRM,
3 stage
carrier revE (x4)
2-stage amp
(x8)
2-stage amp
(x8)
2-stage amp
(x8)
2-stage amp
(x8)
ASIC 0
ASIC 1
ASIC 2
ASIC 3
Zynq '030 SoC
x6
x6
x6
x6
SCROD revB
Zynq '045 SoC
LVDS fanout
timing trigger
SFP+ data
JTAG
SFP+ trigger
Zynq '030 SoC
HIGHWAY
LVDS + gigabit xceiver
CLOCK_to_ASICs
LVDS
TRIG_to_GDL
LVDS + serdes
spare
LVDS + serdes
spare
LVDS + serdes
Zynq '045 SoC
https://www.phys.hawaii.edu/~mza/presentations/iTOP-boardstack-schematic-diagram.png

Commonalities

SLAC

1. PGP
   - Communication between SCROD and Carriers via GTX is handled by PGP blocks.
   - Partitioned into 4 virtual lanes each.
   - At present only 2 are used: data (VC 0) and register (VC 1).
2. AXI4Lite
   - Two masters on each board:
     - One from DAQ system (GbE or B2link).
     - One from PS.
   - The primary way to communicate with registers and peripheral devices is through AXI4Lite buses.
   - When a different interface exists (e.g., IRSX register controllers), we wrap it into an AXI4Lite interface.
3. AXIStream
   - Waveform data is transmitted via AXIStreams.
   - Simple valid, start-of-frame, end-of-frame protocol.
4. Synchronizers, FIFOs, other SLAC StdLib interfaces.
   - More on these later today.