Jetting Your Way to Fine-pitch 3D Interconnects

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An insatiable consumer appetite for instant access to exponential functionality at reduced cost is powering the smart phone and intelligent tablet device markets. The question is: why? Goldman Sachs uses the 5C's to describe the attraction of these devices: consumption, content, connected, constant-on and commerce. While they were referring to the Apple iPad, the 5C's can be applied to the continuous push by "smart" device manufacturers to meet consumers' ongoing thirst for instant access to electronic content regardless of how it is supplied. These smart devices are finding their way into a wide range of markets such as automotive (smart cars); appliances (catch the latest episode of Food Network right on your refrigerator); search the web, check out a book from the library, watch that latest on-demand movie while downloading the latest exercise video — all controlled through a Wii multi-media console.

So how do manufacturers deliver a compelling product that fits within increasingly smaller packages and supports streaming audio, video, fast search/download, and touch screen commerce, all at attractive prices? Is through silicon via (TSV) the only packaging solution?

Challenges abound with the TSV approach, although the majority can be solved with time and money. The most challenging obstacles are 3D infrastructure and the associated supply chain to enable broad adoption of 3D ICs. 3D TSV interconnects have many possible implementation scenarios ranging from when in the process flow (first, middle, or last) the via is formed, to which process is used in its creation (e.g. front, or back-side). Another key challenge is I/O standardization between memory and application layers. Lastly, as package complexity increases, thermal management may become a troublesome issue. Yes, TSV holds lots of promise, but the fact remains: manufacturing challenges are yet to be fully addressed.

Can wire-bond solutions continue to meet system-in-package (SiP) scaling demands? While wire bonding attempts to address growing interconnect density challenges — the overall diameter of the bonding wire is <35µm and equipment placement accuracy is improving — the sheer number of interconnects between memory stacked 8-16 chips high present both performance and manufacturing challenges. Issues, such as signal integrity, become real show stoppers as customers push performance goals of these devices. The challenge is exacerbated when stacking sophisticated multi-chip packages that integrate processors. While wire-bond technology remains viable for the majority of today's semiconductor interconnect applications, it may be reaching an inflection point as 3D packaging demands push the functionality envelope.

Is there another way to meet these advanced packaging challenges without having to completely reinvent manufacturing processes and technologies?

Replacing traditional wire bonds with fully printed conformal interconnects using evolutionary packaging steps may be the answer to these complex issues. A proprietary aerosol jet technology has been used in a variety of printing applications ranging from crystalline silicon solar wafers and next-generation touch screen displays, to fully printed transistors. The ability of this technology to print a variety of materials onto a wide array of substrates at feature sizes as small as 10µm makes it a logical choice for addressing fine-pitch semiconductor packaging requirements.

Aerosol Jet Process - How it Works

Aerosol jet[1] printing begins with atomization of an ink, which can be heated up to 80°C, producing droplets on the order of one to two microns in diameter. The atomized droplets are entrained in a gas stream and delivered to the print head, which also can be heated to 80°C. Here, an annular flow of clean gas is introduced around the aerosol stream to focus the droplets into a tightly collimated beam of material that also serves to eliminate nozzle clogging. The combined gas streams exit the print head through a converging nozzle that compresses the aerosol stream to a diameter as small as 10µm. The jet of droplets exits the print head at high velocity (~50 m/s) and impinges upon the substrate. Electrical interconnects are formed by moving the print head, equipped with a mechanical stop/start shutter, relative to the substrate. All printing occurs without the use of vacuum or pressure chambers and at room temperature.

The high velocity of the jet enables a relatively large separation between the print head and the substrate, typically 2-5mm **(Figure 1)**. The droplets remain tightly focused over this distance, resulting in the ability to print conformal patterns over three dimensional

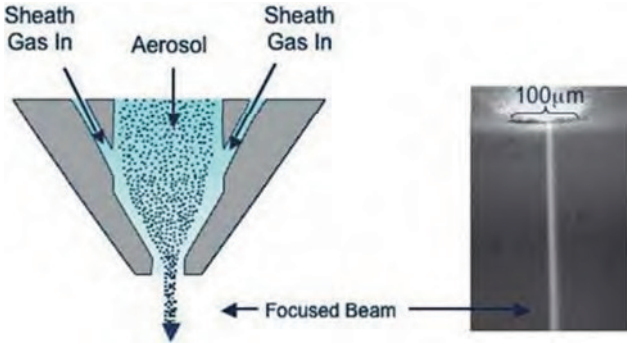

Figure 1. Aerosol jet print head

substrates such as stacked die. Despite the high velocity, the printing process is gentle; substrate damage does not occur and there is generally no splatter or overspray from the droplets.

Once patterning is complete, the printed ink typically requires post-treatment to attain final electrical and mechanical properties. Post-treatment is driven more by the specific ink and substrate combination than by the printing process.

The atomization step is very flexible compared to inkjet. Particulate suspensions are easily atomized, although as a general rule, suspended particles should be on the order of 0.5µm or less. Ink viscosity may be in the range of 1-1000 cP, although it may be necessary to optimize the viscosity for a particular application. The materials used to construct the printing system hardware are generally not susceptible to degradation by the ink solvents, allowing a wide range of solvent vehicles to be used in the process.

Direct Write of Interconnects

The relatively large working distance (the distance from the print tip to the substrate) of the aerosol jet print head enables conformal printing along stacked dies of 2mm or less in total height without having to adjust Z-height positioning. Typical interconnects are 25-30µm wide by >5µm in height. Total length of the interconnects are typically 1.5mm long with throughput for a single nozzle reaching up to 5,000 interconnects per hour **(Figure 2)**. The aerosol jet print head is highly scalable, supporting 2, 3, 5, or more nozzles at a time, enabling projected throughputs of > 20,000 or more interconnects per hour. The print head can handle extended print runtimes of twelve hours or more before ink refill is required. An automated ink refill system that will extend ink runtime to twenty-four hours or more is under development.

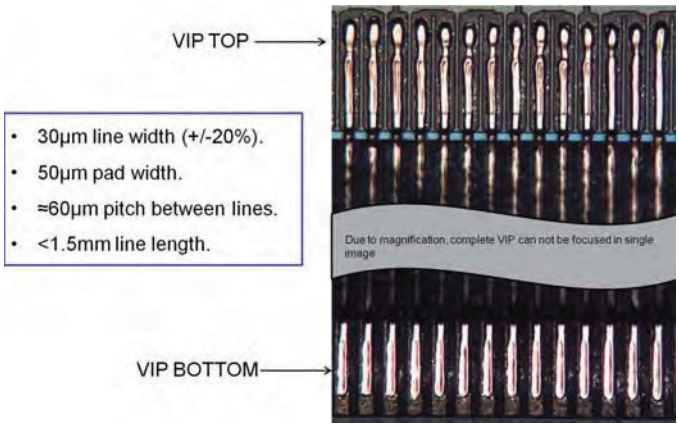

Figure 2. Vertical interconnect package

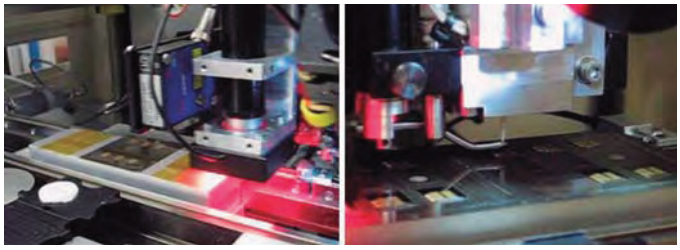

Figure 3. Integrated aerosol jet print solution

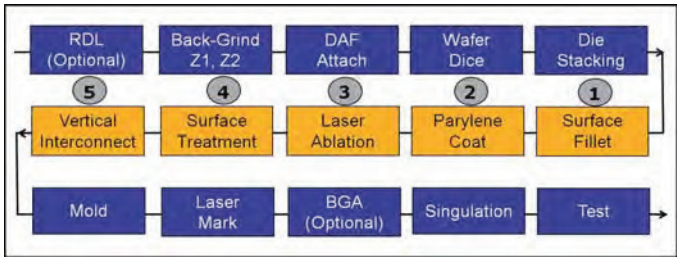

Figure 4. Vertical interconnect pillar (ViP) process

Automation Integration

The aerosol jet print engine has been integrated into an electronics automation supplier's production proven platform **(Figure 3)**. The automation platform accommodates the print engine including the atomizer and print head, heater, shutter, and process controls. Additionally, the automation platform is equipped with auto-fiducial synching; shutter cleaning station; motion control with +/- 5µm of accuracy; heated platen to 150° C; auto board load and unload; and GUI driven interface with on board system diagnostics. The platform is highly scalable and capable of supporting evolving semiconductor packaging form factors.

A Working Process

This novel solution is suited for printing fine featured interconnects and other materials meeting demanding manufacturing specifications. However, printing is only one step in the manufacturing of fully functioning SiP's using the vertical interconnect pillar (VIP) process.[2] In addition to industry standard package manufacturing steps, five additional steps **(Figure 4)** that fully enable the implementation of fine-pitch vertical interconnect printing are necessary and include surface fillet, parylene coating, laser ablation, surface treatment, and fine-pitch vertical interconnect.

Typical print inks tend to flow downhill regardless of their viscosity. The surface fillet **(Figure 4)** is used to create a gentle sloped surface on the stacked die, typically creating 45-60° inclines, which prevent the material from free flow at steep angles. The parylene coating is applied to the entire stack and then an excimer laser is used to open specific pads on the dies and substrate where an electrical connection is required. A surface treatment is used to clean away ablated material and change the surface tension to enable printing of fine-pitch vertical interconnects without shorting between parallel lines on the stacked die over 3D topology.

Using inks that meet both mechanical and electrical requirements is key to the fine-pitch interconnect process. These

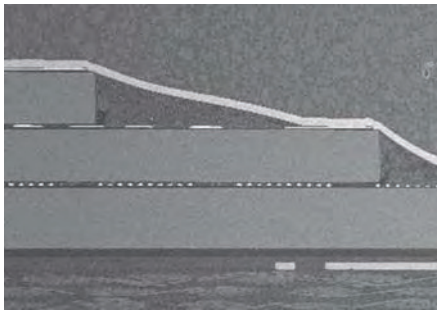

Figure 5. Aerosol jet printed interconnect

inks must be capable of extended 8+ hour production runs without any changes in output rates or electrical characteristics. They need to stack properly without overspray or satellites, maintaining mechanical dimensions throughout the course of a manufacturing shift. As direct-write printed electronic applications continue to grow, a new class of nanoparticle electrically conductive materials (inks) has found its way into the market, fully meeting manufacturing specifications.

As interconnects are printed from board connectors along the die stack, they come into contact with the laser ablated (exposed) pads and create electrical connections. A single printed interconnect may connect with openings on several die, thereby creating a more compact electrical connection and efficient circuit **(Figure 5)**.

With wire bond, interconnects extend from one pad to another, requiring the need for multiple physical wires to create a complete pad-to-pad circuit. As package densities increase the number of wire-bond connections increase, creating the potential for cross talk and/or signal integrity challenges within SiP packages. This may force a vendor to slow the operational efficiency of the circuit and limit full device functionality.

Validating the process

The steps in the ViP process have been optimized over the past twelve months. Each process step has been fully analyzed and optimized for SiP packages. Actual boards filled with functioning SiP's have gone through the proprietary process steps, including the aerosol jet fine line interconnect print step with printed conformal interconnects of 25-30µm wide by > µm high, and fully functioning parts have been manufactured.

Any product that will be commercially sold needs to pass industry standard reliability testing **(Figure 6)**. Complete product qualification tests are underway that will re-validate the process and product by Q3 of 2010. Pilot production sites are due online before the end of 2010, with full, high-volume production systems available by Q1 2011.

Expanding Capabilities

Fine line printing for SiP technology is just at the beginning of its life cycle. When direct write ViP technology was introduced more than two years ago, the minimum line width was 100µm, with a pitch of 200µm. With the introduction of the aerosol jet technology, line widths of 25-30µm are being achieved with pitches of < 65µm. With further refinement of the technology, line widths as small as 10-15µm at 25µm pitch are expected to be possible.

Aerosol jet technology also has the added benefit of printing a wide array of materials. Investigation is underway for utilizing the process to print a dielectric material coating to selectively insulate pads. The benefit of this

	VCI DRAM (BGA) Pass Server Level Reliability	VCI FLASH (µSD) PASS	VCI FLASH (LGA) PASS	VCI SiP (BGA) Under Qual
Moisture Resist Test:	JEDEC Level 3 @260°C	JEDEC Level 3 @260°C	JEDEC Level 3 @260°C	JEDEC Level 3 @260°C
Biased-HAST:	Bias 3.6V, 130°C, 85% RH, 144 hours	Bias 3.6V, 130°C, 85% RH, 96 hours	Bias 3.6V, 130°C, 85% RH, 96 hours	Bias 3.6V, 130°C, 85% RH, 96 hours
Autoclave/PCT:	Unbiased, 121°C, 2atm, 100%RH, 96 hours	NO	Unbiased, 121°C, 2atm, 100%RH, 96 hours	Unbiased, 121°C, 2atm, 100%RH, 96 hours
High Temp Storage:	150°C, 1000 hours	150°C, 1000 hours	150°C, 1000 hours	150°C, 1000 hours
Temp Cycle:	-55/+125°C, 1000 cycles (B)	-55/+125°C, 1000 cycles (B)	-55/+125°C, 1000 cycles (B)	-55/+125°C, 1000 cycles (B)
Card Tests: (DBT/Insert/Salt)	N/A	SDI Spec.	N/A	N/A

Figure 6. VCI reliability test criteria

approach is further reduction in process and equipment costs. Other areas, such as surface fillet printing and printing redistribution layers (RDLs) with this process are also being explored.

Viable Interconnect Alternative

Wire-bond solutions will not just fade away and TSV is emerging as the solution for the most complex packaging challenges. However there is the middle ground where 3D printed interconnects can provide real cost and functional benefits for the production of multi-chip stacked die in SiP applications. Aerosol jet's fine line printing capabilities enable significant pitch reductions, thereby increasing interconnect densities and affording greater semiconductor packaging functionality at a fraction of the cost of TSV technology. With its ability to use off-the-shelf materials and print in normal atmospheric conditions, equipment and maintenance costs are greatly reduced. This multi-function platform is clearly poised to enable high density interconnect solutions for a range of advanced 3D semiconductor packaging applications.

References

1. Aerosol Jet is a trademark of Optomec, Inc.
2. Vertical Interconnect Pillar process is a trademark of Vertical Circuits, Inc.

For questions concerning the Aerosol Jet print solution, email the company at requestinfo@optomec.com
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