

6

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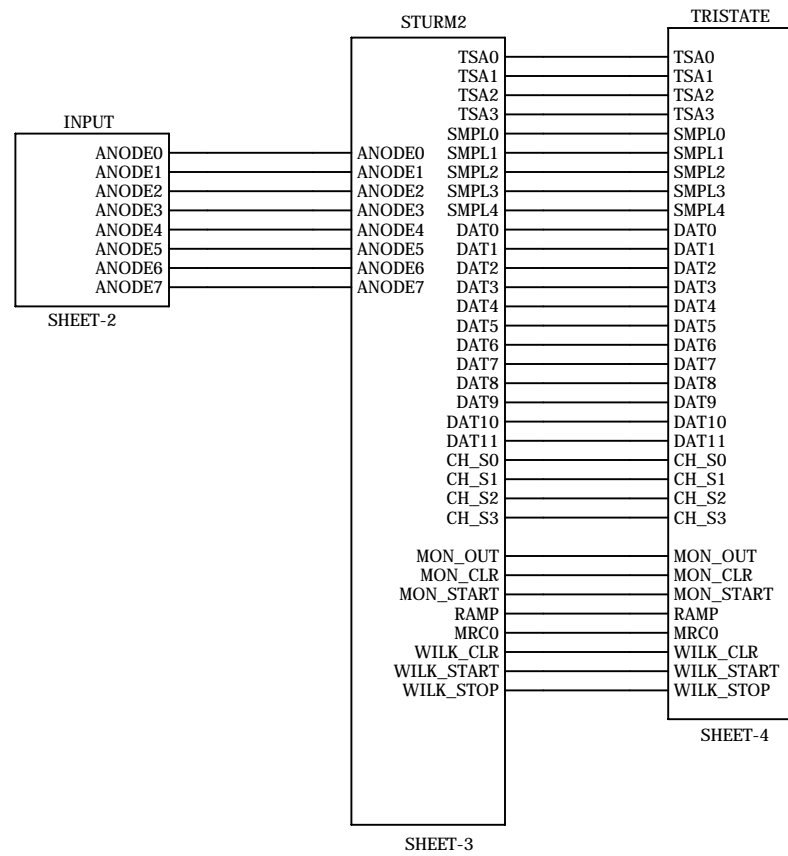
E

D

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institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	DC_STURM2
revision:	D
IDLAB design #:	IDL_13_035
circuit design:	JM
PCB design:	JM
sheet #:	1 of 4
sheet description:	TOP Block
date last modified:	13-AUG-2013

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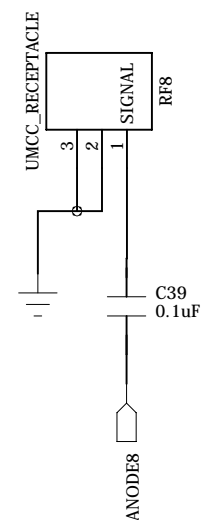
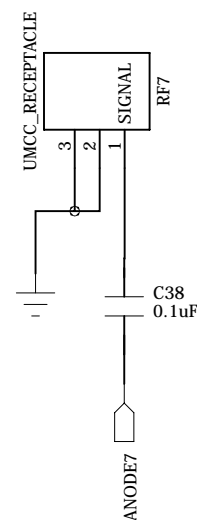
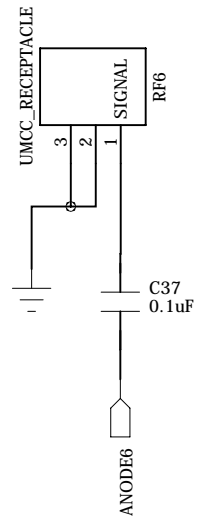
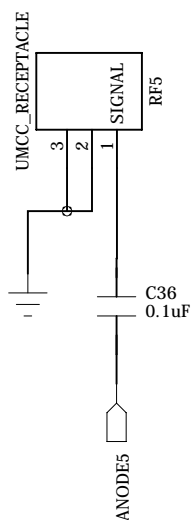
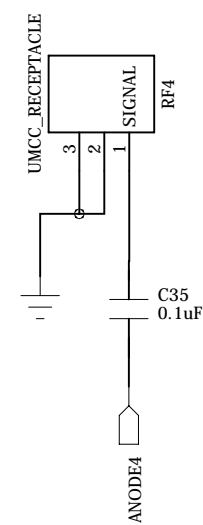
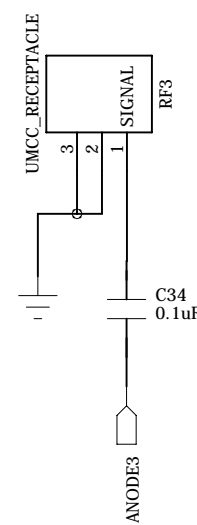
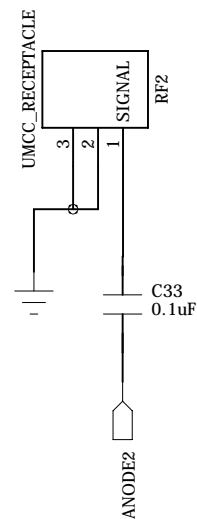
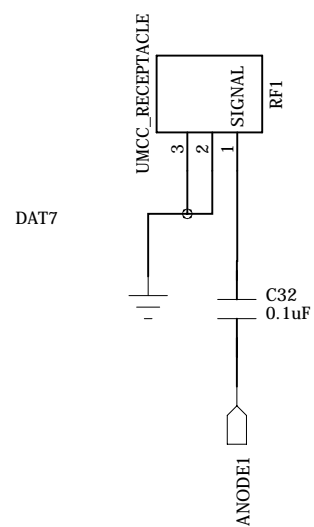
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Input capacitors 1.6 -2 pF



institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab

title: DC_STURM2
revision: D
IDLAB design #: IDL_13_035
circuit design: JM
PCB design: JM

sheet #: 2 of 4
sheet description: Signal input
date last modified: 13-AUG-2013

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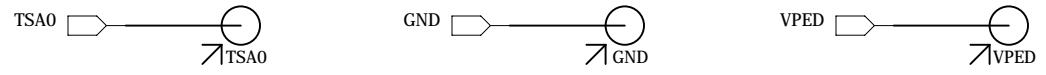
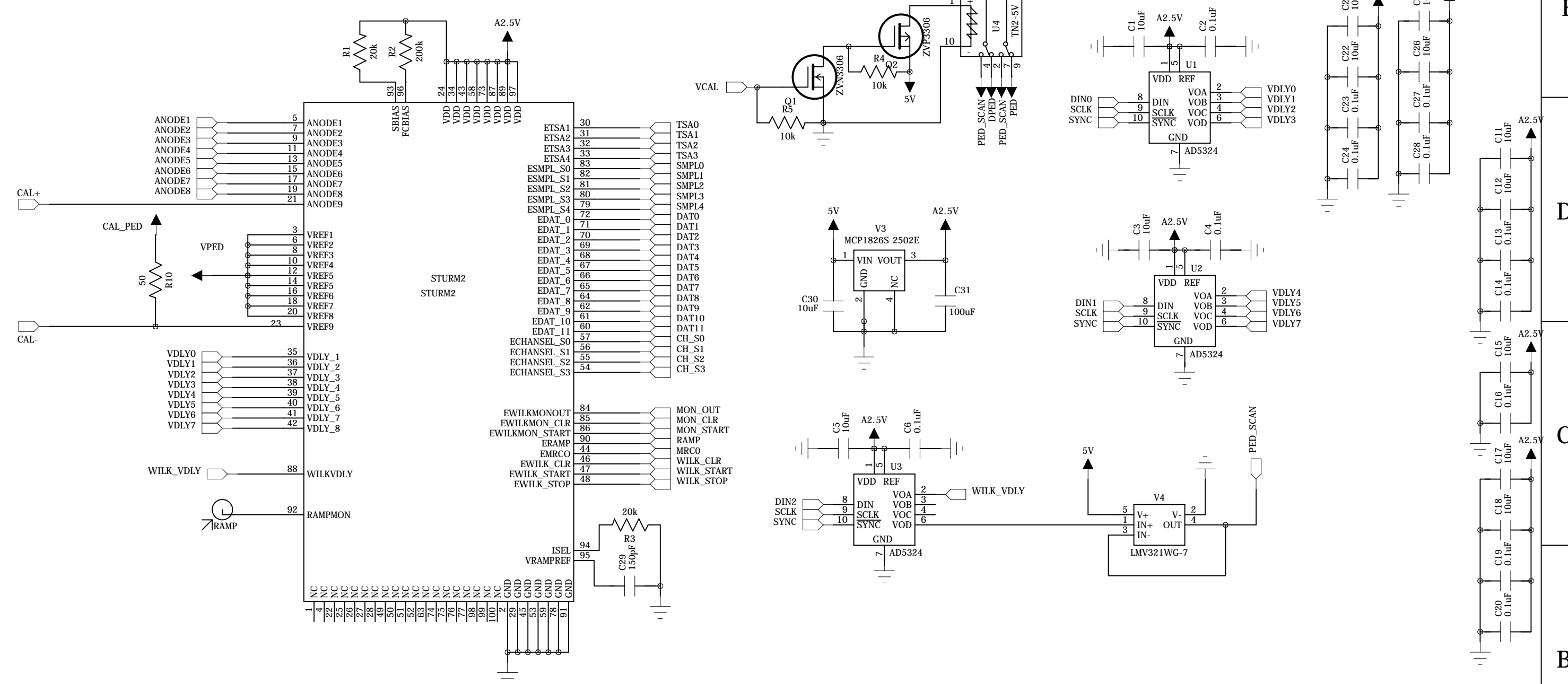
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VPED set to 1.24 Volts

$$VPED = 0.41 * (R9 + R10) / R10$$

 Keep R10 between 10k - 200k

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	DC_STURM2
revision:	D
IDLAB design #:	IDL_13_035
circuit design:	JM
PCB design:	JM
sheet #:	3 of 4
sheet description:	STURM2
date last modified:	13-AUG-2013

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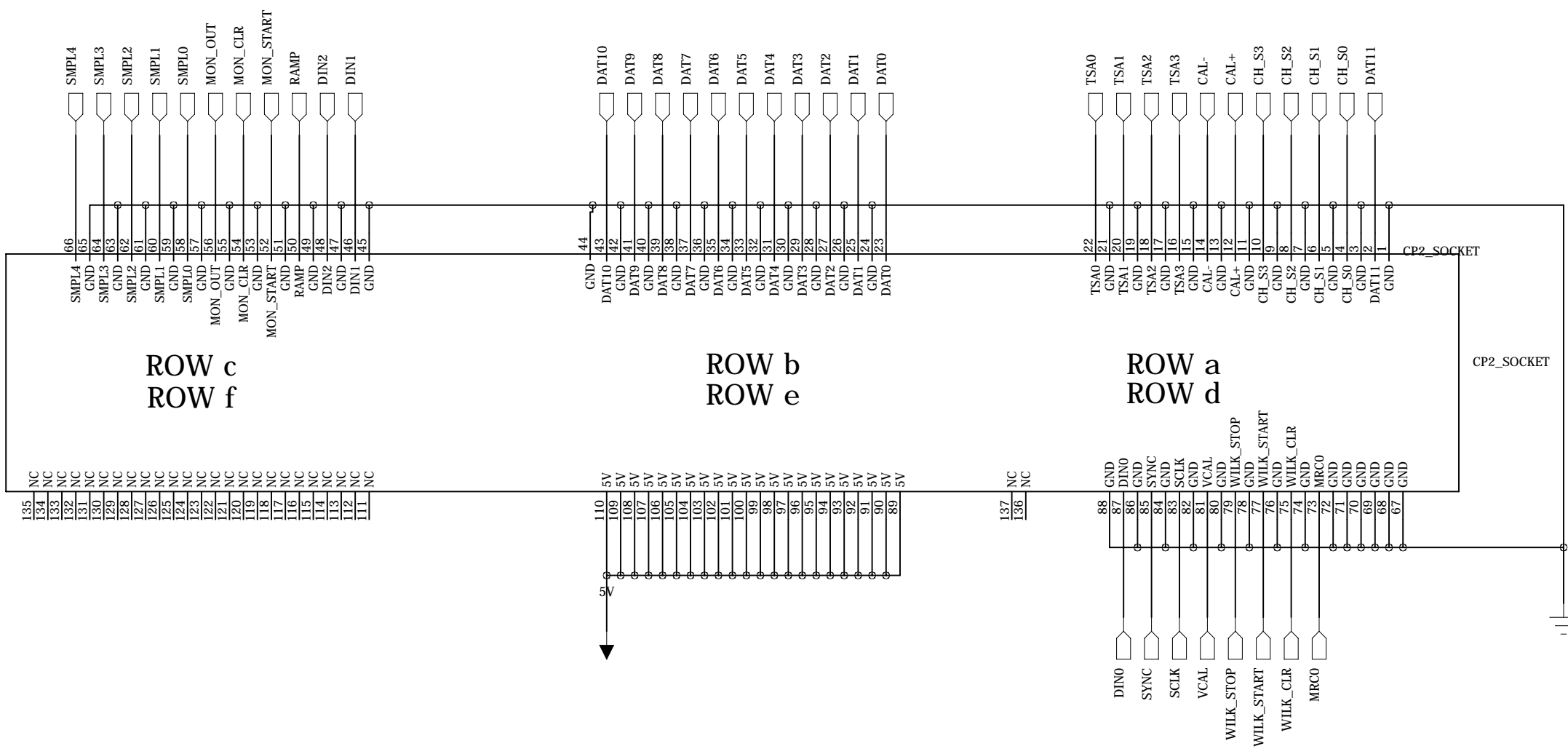
C

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institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	DC_STURM2
revision:	D
IDLAB design #:	IDL_13_035
circuit design:	JM
PCB design:	JM
sheet #:	4 of 4
sheet description:	SCROD connection
date last modified:	13-AUG-2013