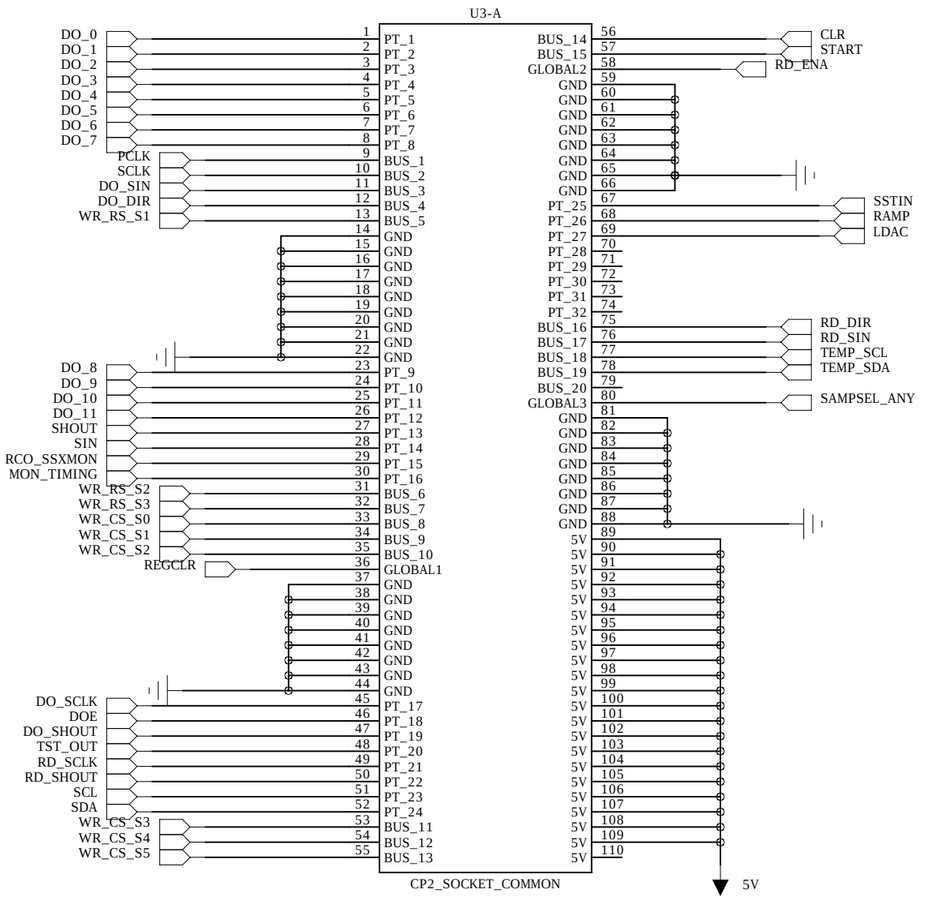
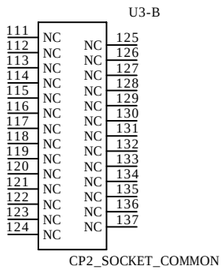
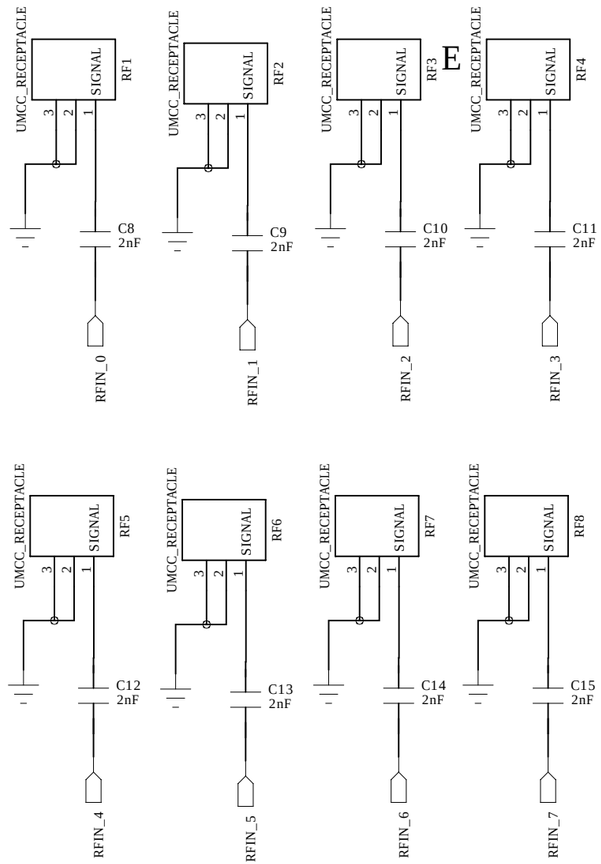
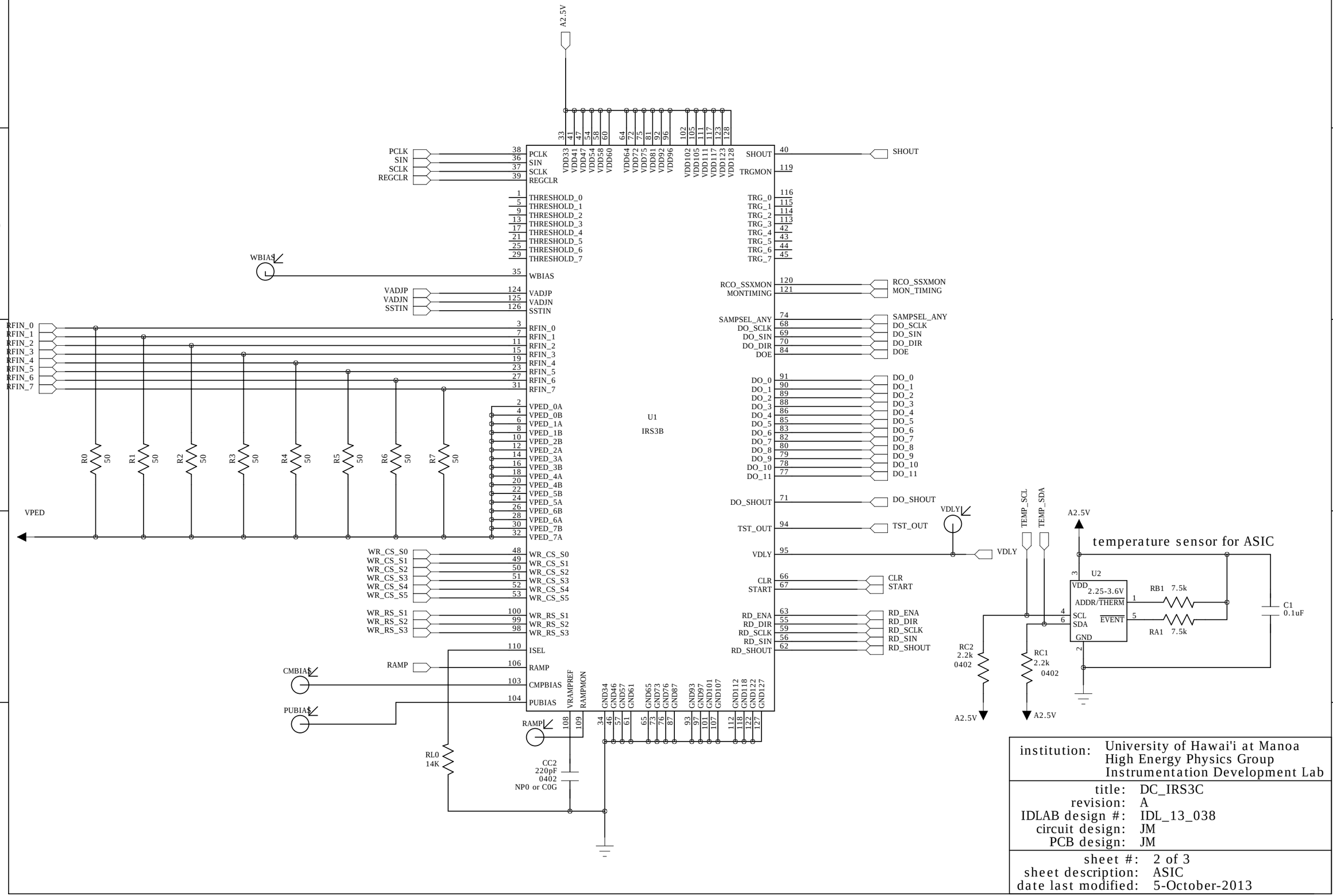




Input capacitors 1.6 -2 pF

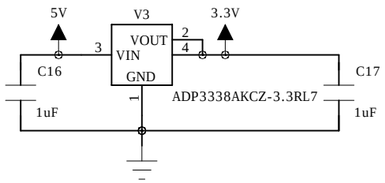


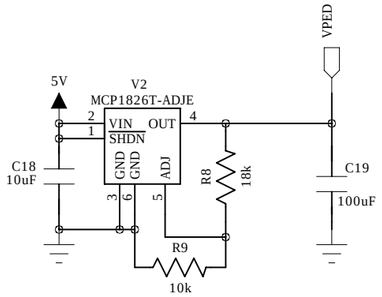
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	DC_IRS3C
revision:	A
IDLAB design #:	IDL_13_038
circuit design:	JM
PCB design:	JM
sheet #:	1 of 3
sheet description:	Input / SCROD connection
date last modified:	5-October-2013



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	DC_IRS3C
revision:	A
IDLAB design #:	IDL_13_038
circuit design:	JM
PCB design:	JM
sheet #:	2 of 3
sheet description:	ASIC
date last modified:	5-October-2013

Provides 3.3 volts to DAC





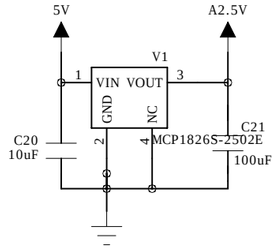
VPED set to 1.24 Volts

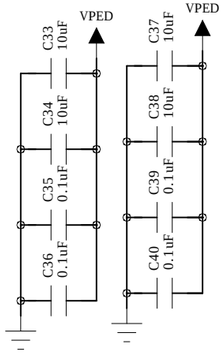
VPED = 0.41 * ((R9 +R10) / R10)

Keep R10 between 10k - 200k

provides pedestal voltage for ASIC

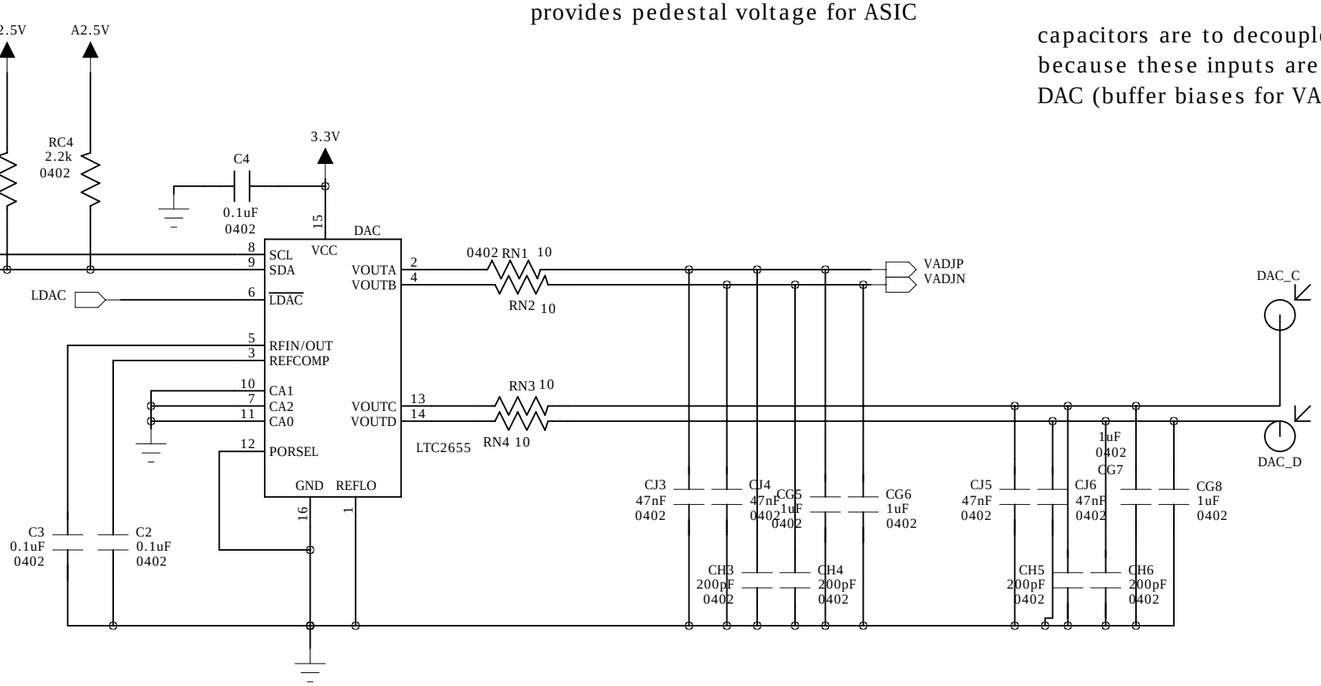
Provides 2.5 volts to ASIC

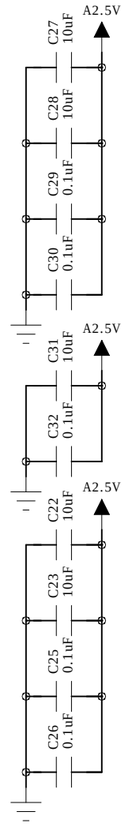




capacitors are to decouple noise from sensitive ASIC inputs
because these inputs are driven, be sure to disable ASIC internal
DAC (buffer biases for VADJP and VADJN are registers #43 and #45)

DACs to control ASIC sampling rate
i2c address = 0010000





institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	DC_IRS3C
revision:	A
IDLAB design #:	IDL_13_038
circuit design:	JM
PCB design:	JM
sheet #:	3 of 3
sheet description:	Power
date last modified:	5-October-2013