

UNIVERSITY
of HAWAI'I®
MĀNOA

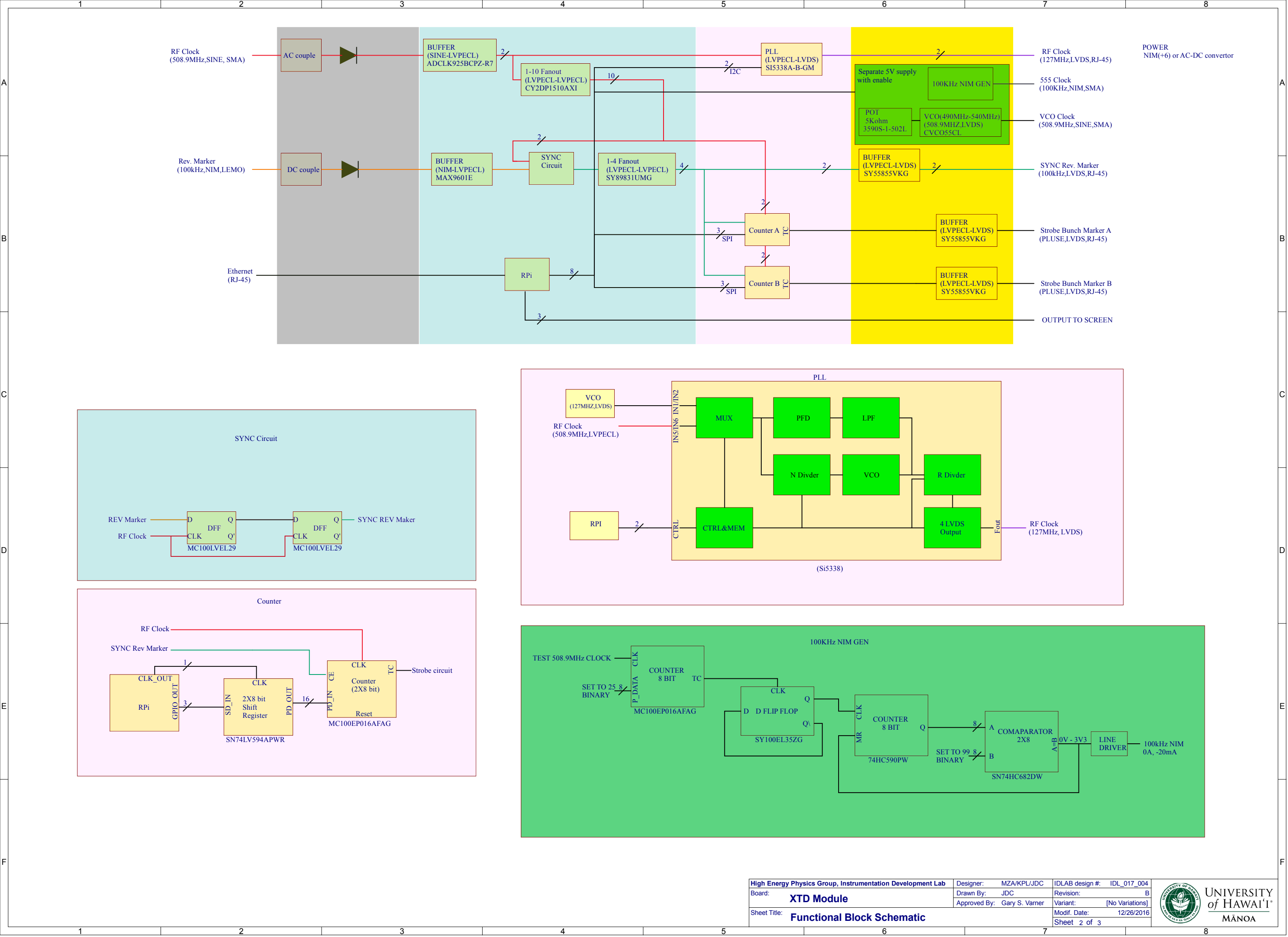
High Energy Physics Group
Instrumentation Development Laboratory
2505 Correa Road, Honolulu, HI 96822

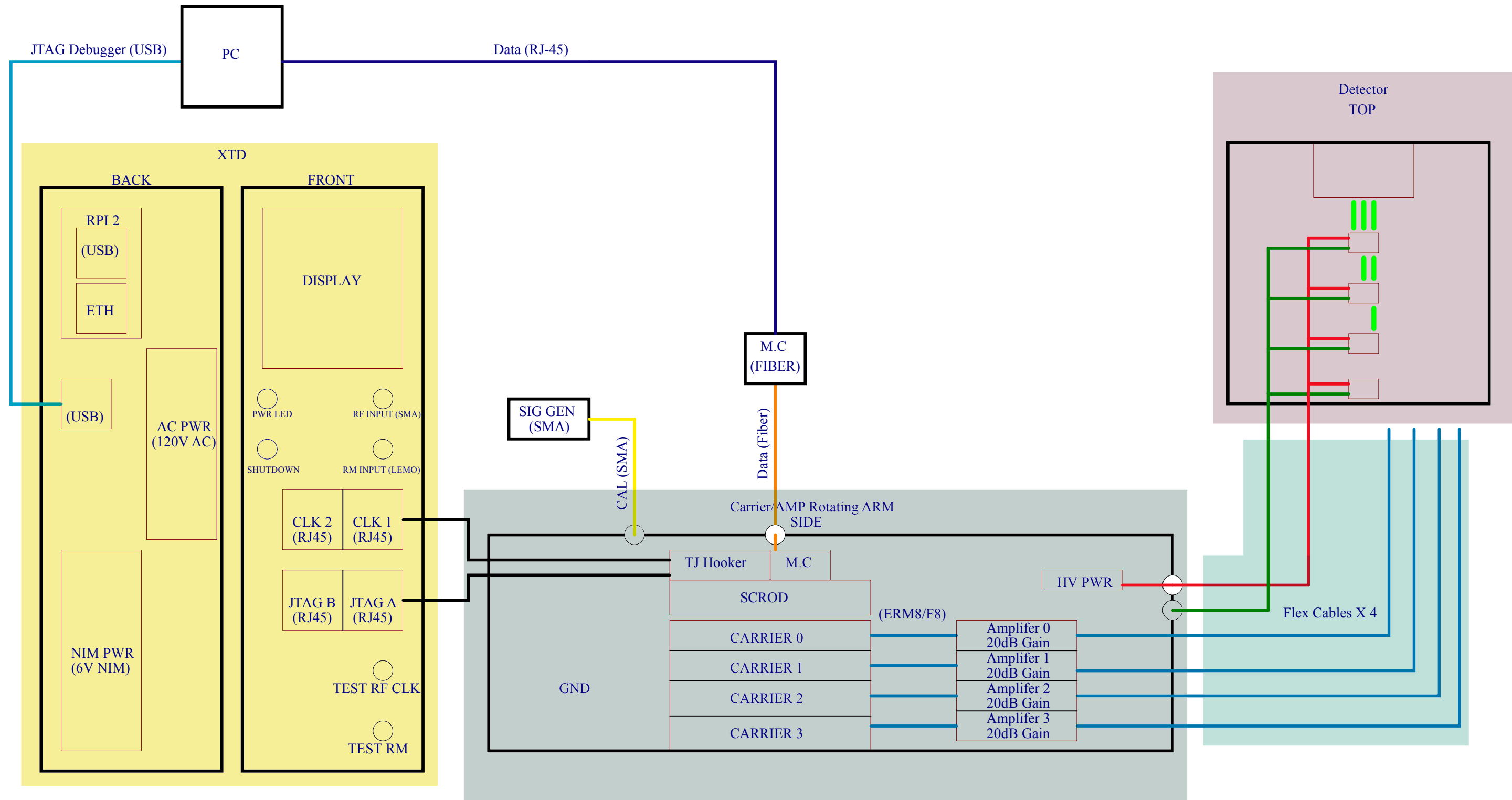
Cannot open file C:\Users\khanhle\Desktop\2017-01-24 12_58_52-Altium Designer (15.1) - C__Users_khanhle_Desktop_XTD_RevB_XTD_RevB_XTD__REVB_ID.png

Production Documentation for:

Project Name: *XTD Module*
Board Name: *XTD Module*
IDL num: *IDL_017_004*
Revision: *B*
Variant: *[No Variations]*

Designer: *MZA/KPL/JDC*
Drawn by: *JDC*
Approved by: *Gary S. Varner*



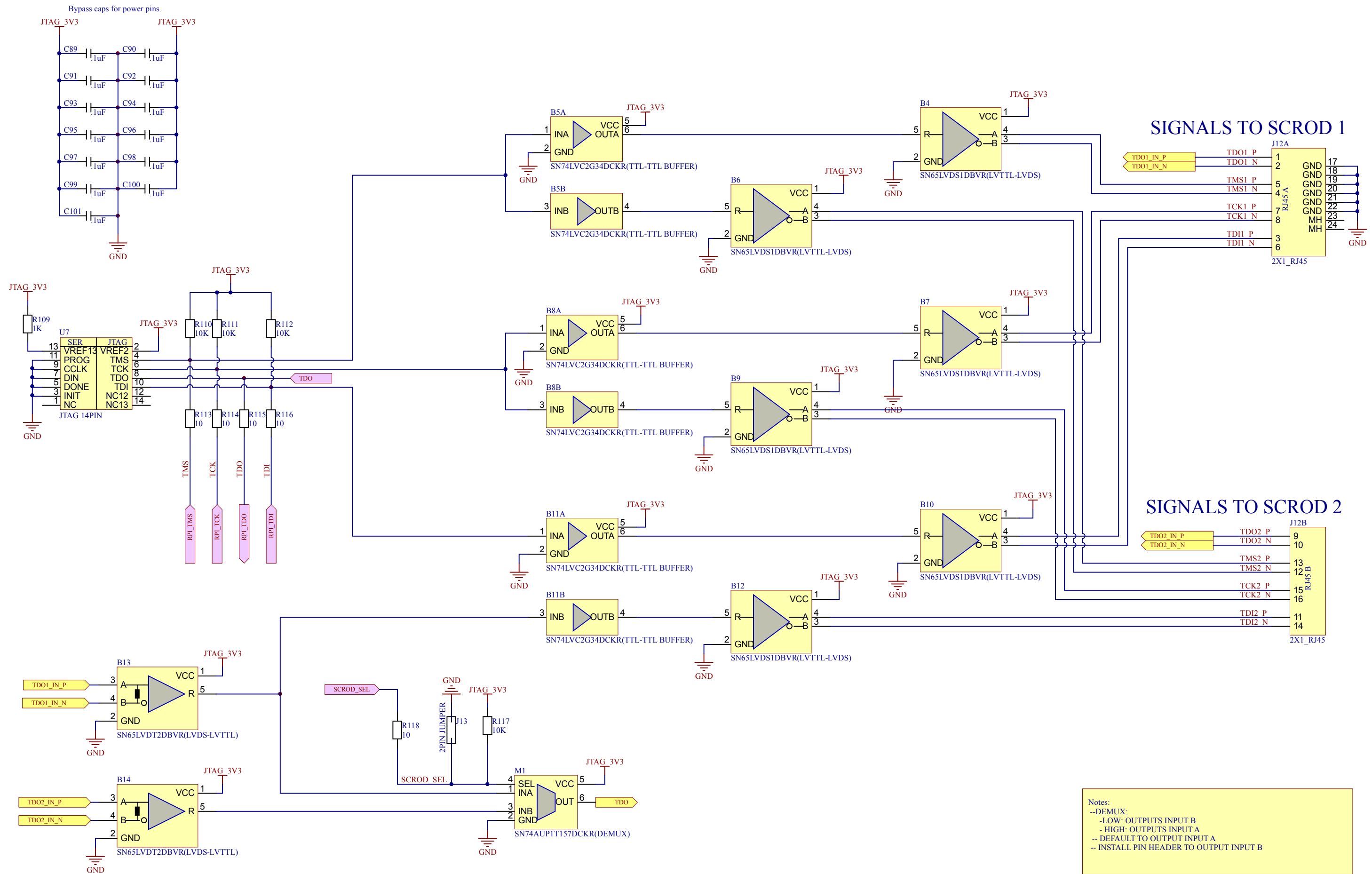


XTD NOTES:

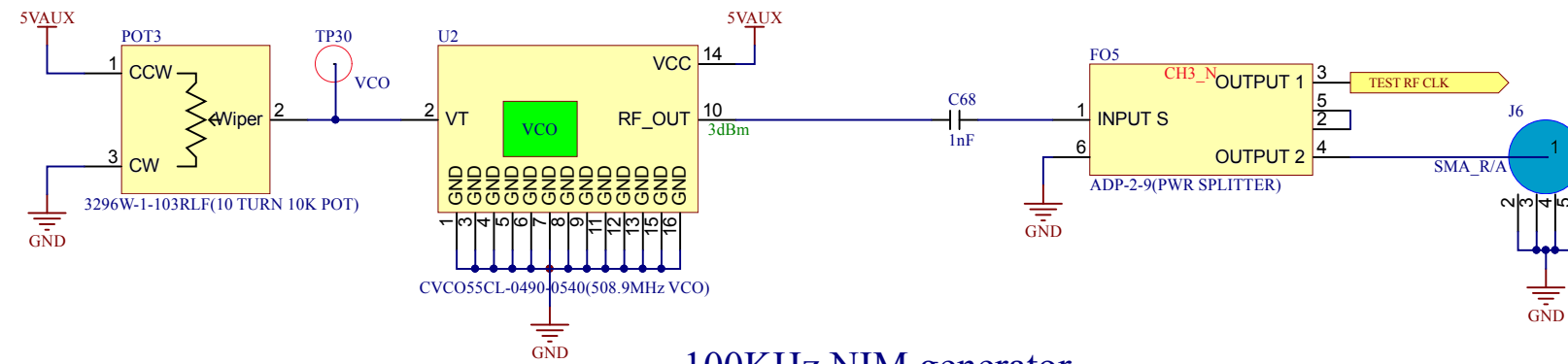
1. JTAG A IS DEFAULT
2. CLK OUTPUT PIN CONFIG
 - 127MHz (7 & 8)
 - REV MARKER (3 & 6)
 - BENCH MARKER A (5 & 4)
 - BENCH MARKER B (1 & 2)
3. JTAG OUTPUT PIN CONFIG
 - TCK (7 & 8)
 - TDI (3 & 6)
 - TMS (5 & 4)
 - TDO (1 & 2)

CARRIER/DETECTOR NOTES:

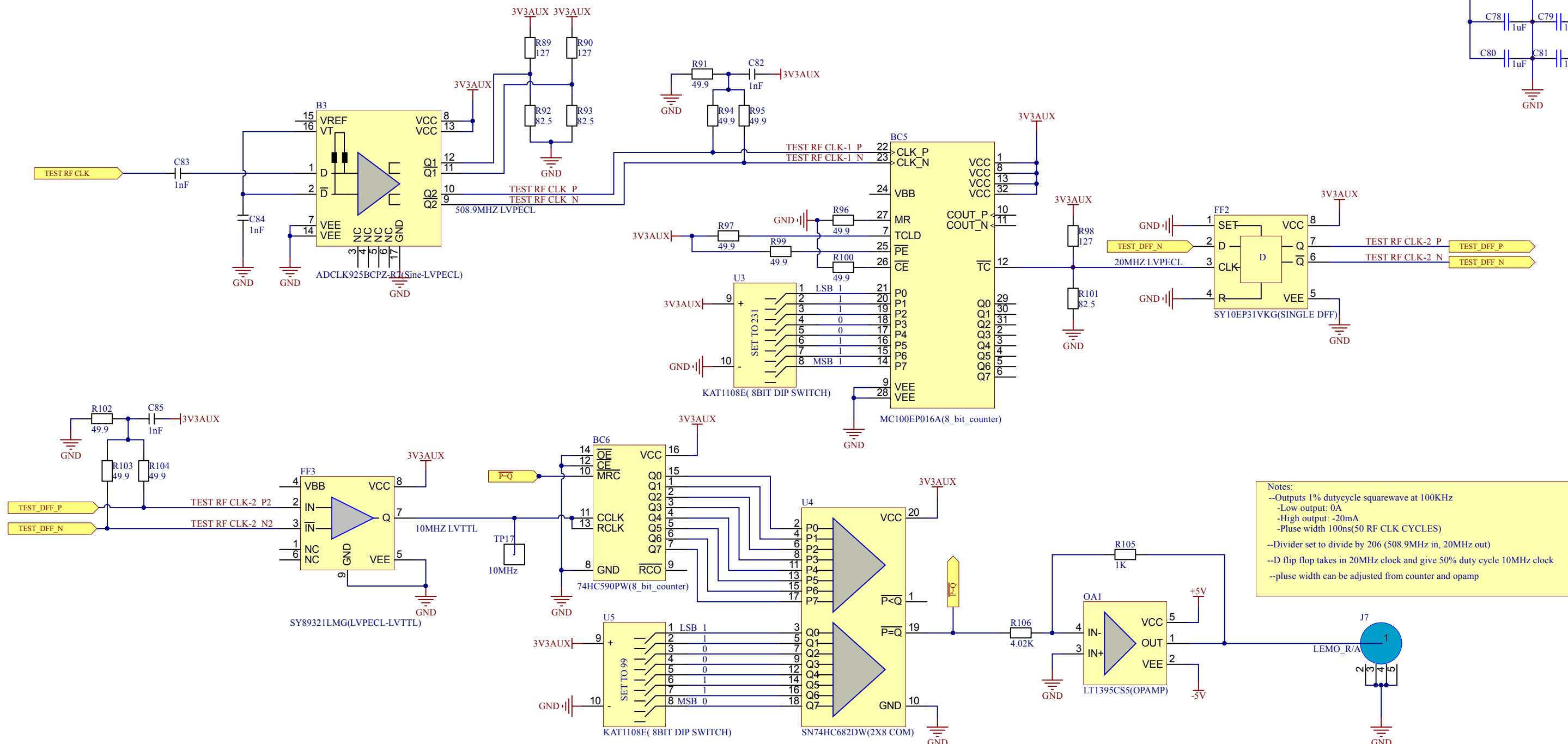
1. USE PROVIDED CABLE FOR DETECTOR 5V & GND



508.9MHz sine wave generator

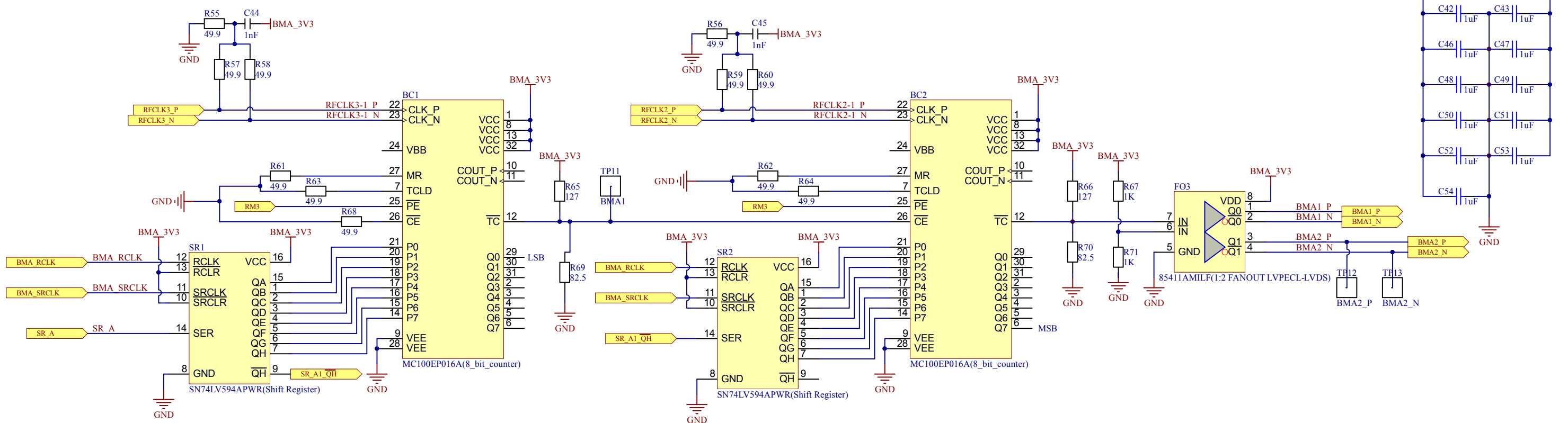


100KHz NIM generator

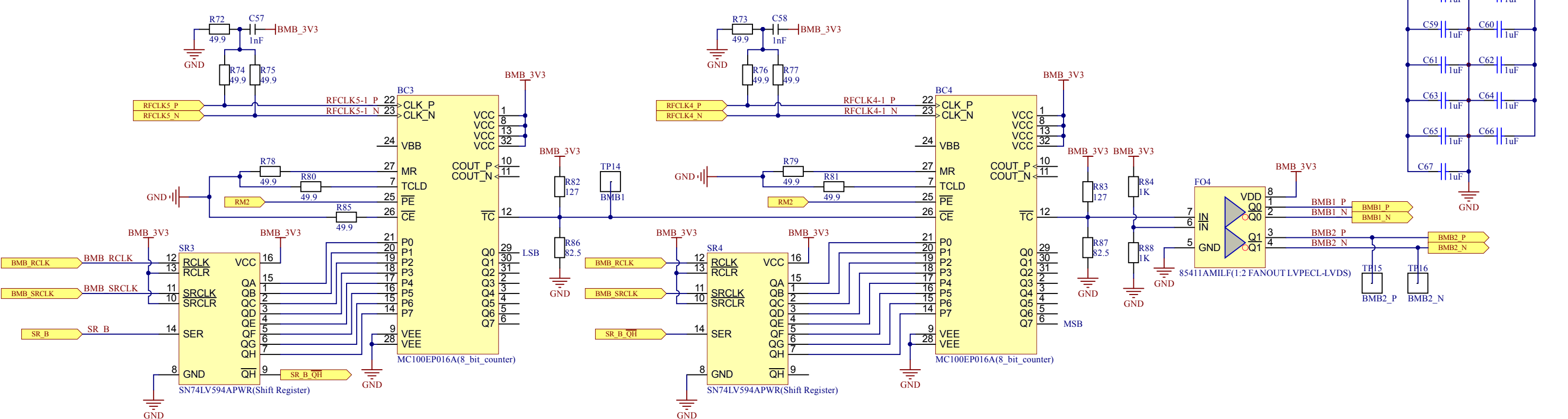


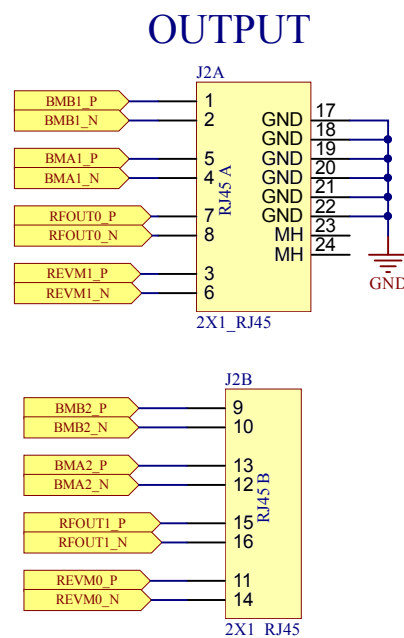
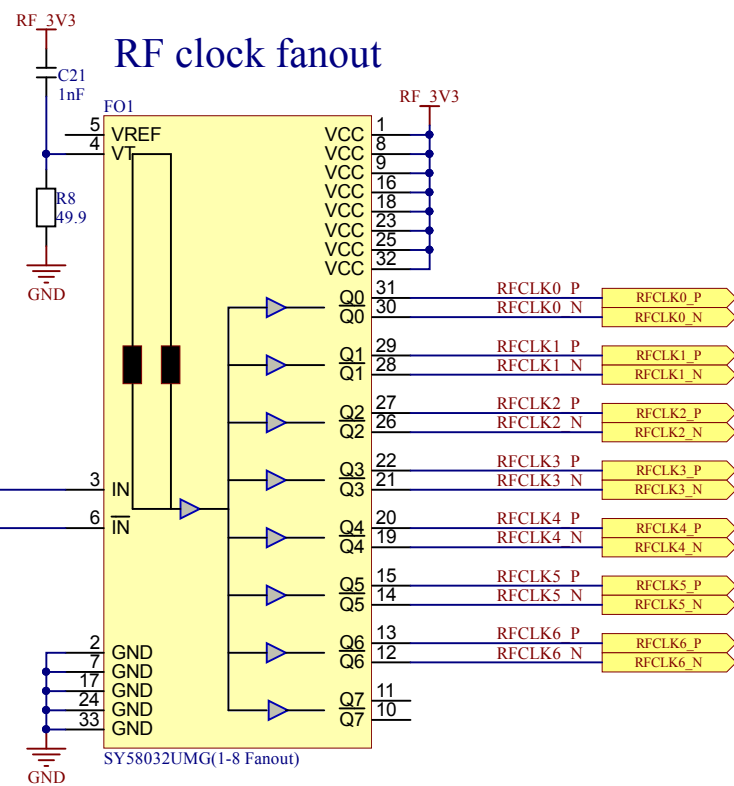
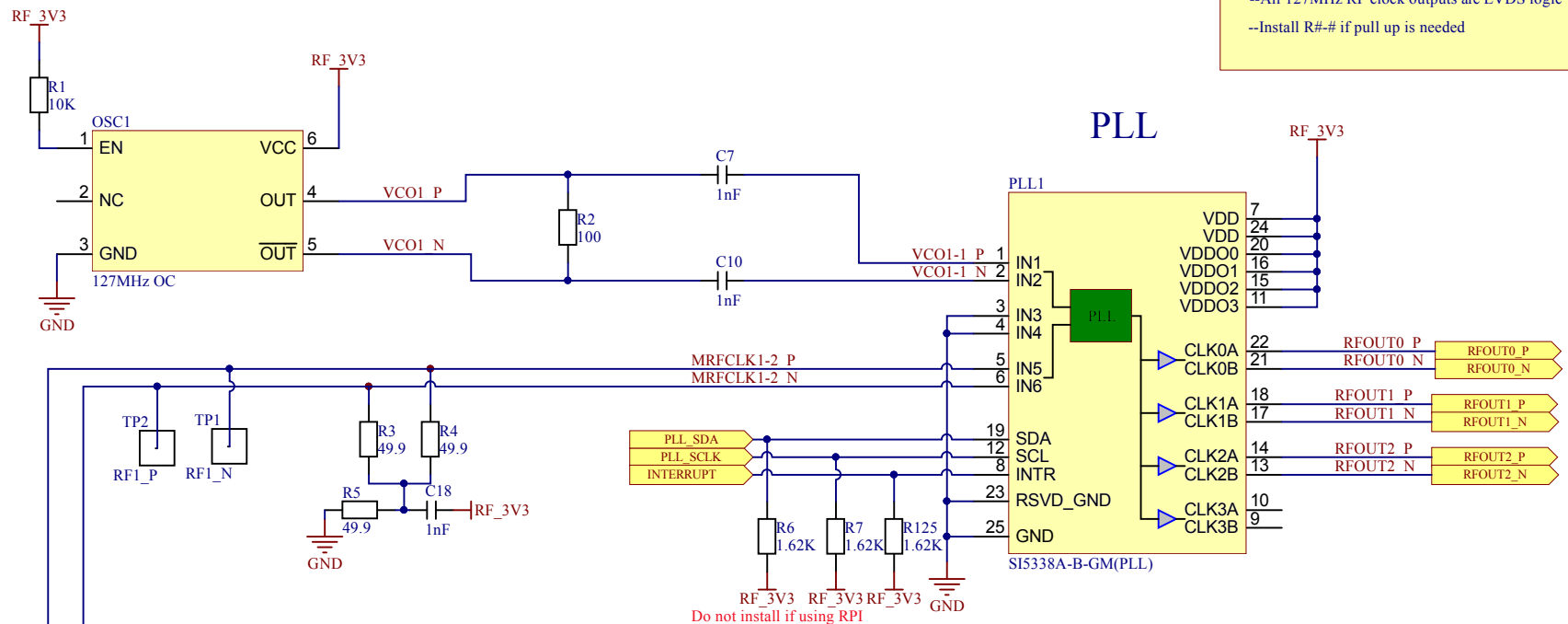
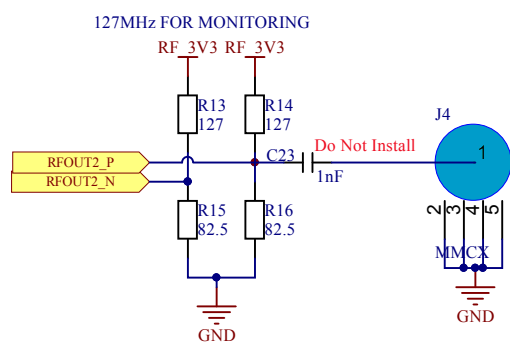
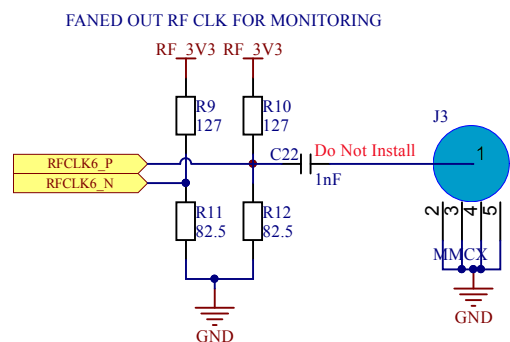
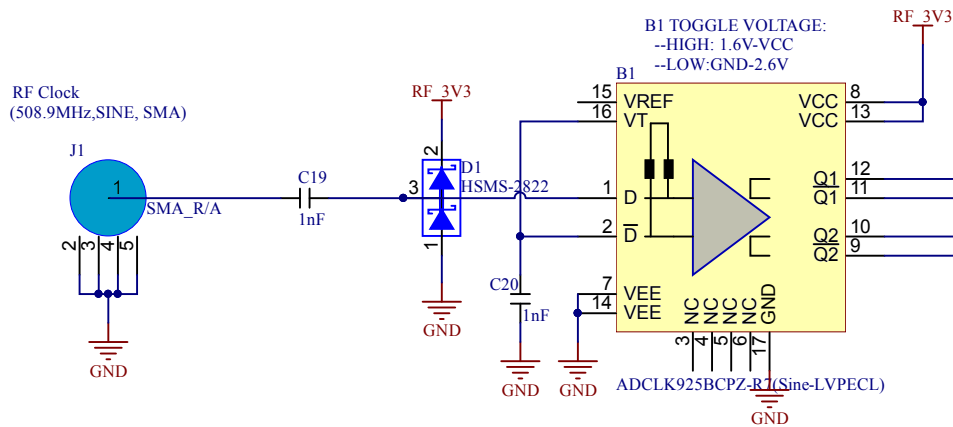
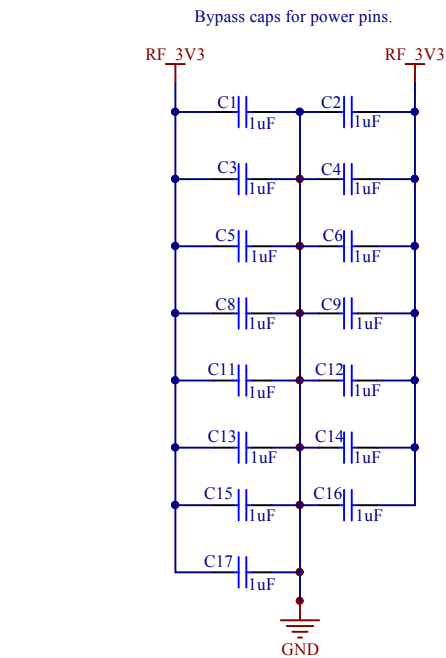
Notes:
 --Outputs 1% dutycycle squarewave at 100KHz
 --Low output: 0A
 --High output: -20mA
 --Pluse width 100ns(50 RF CLK CYCLES)
 --Divider set to divide by 206 (508.9MHz in, 20MHz out)
 --D flip flop takes in 20MHz clock and give 50% duty cycle 10MHz clock
 --pluse width can be adjusted from counter and opamp

Counter circuit for bench marker A

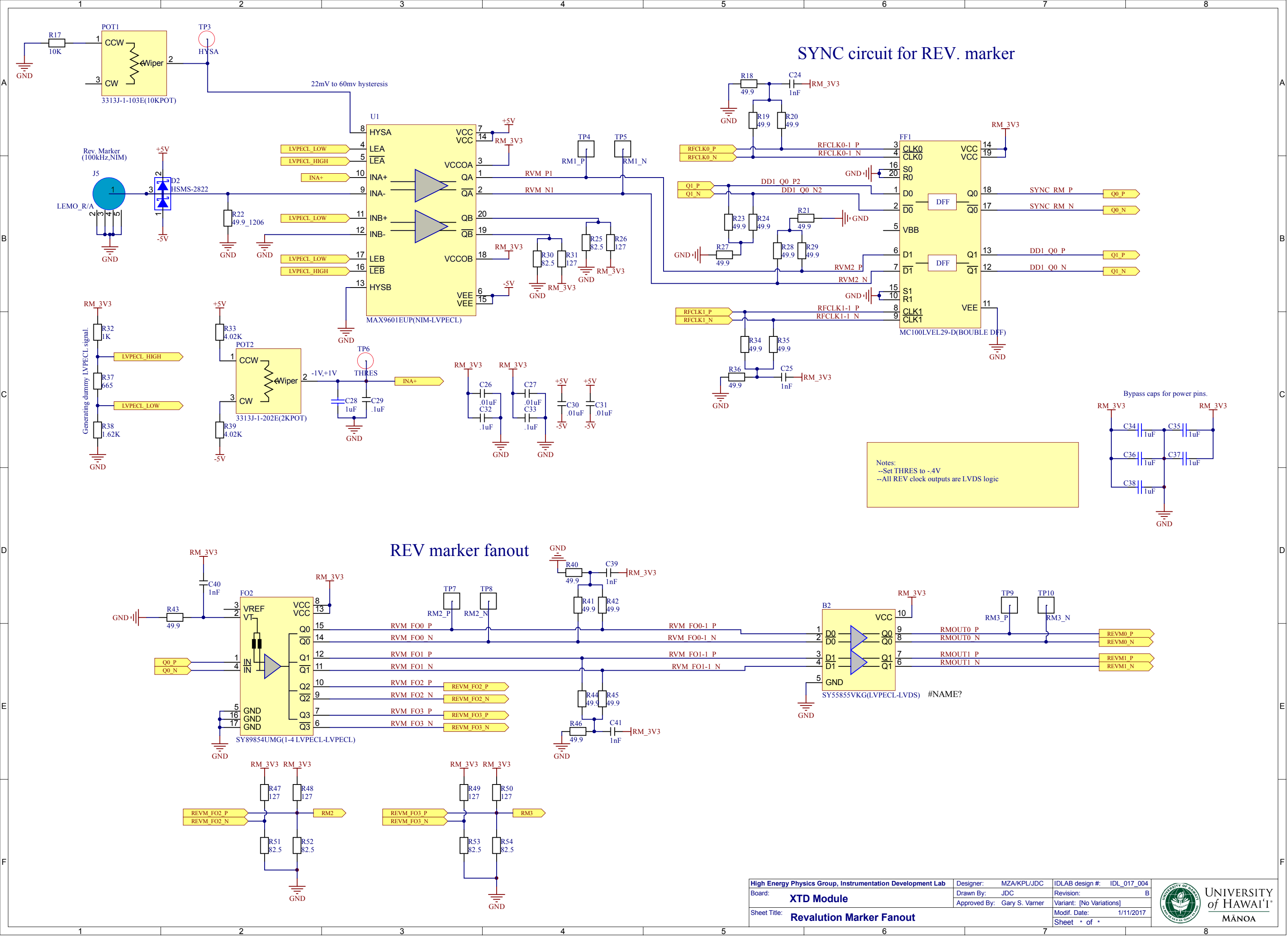


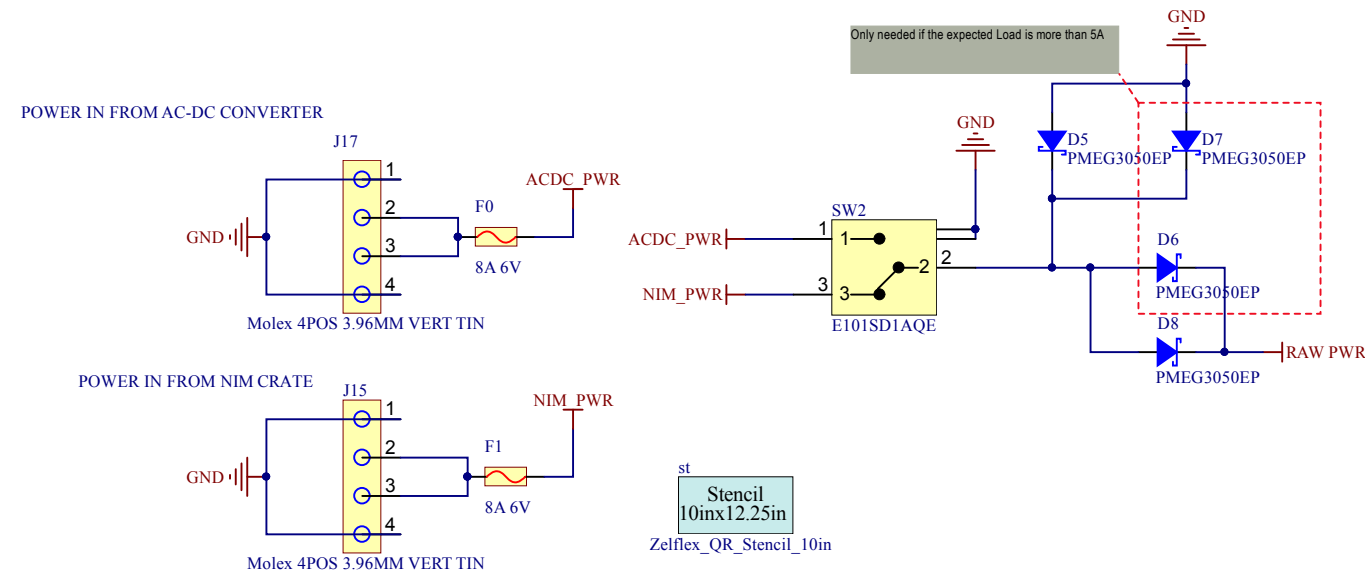
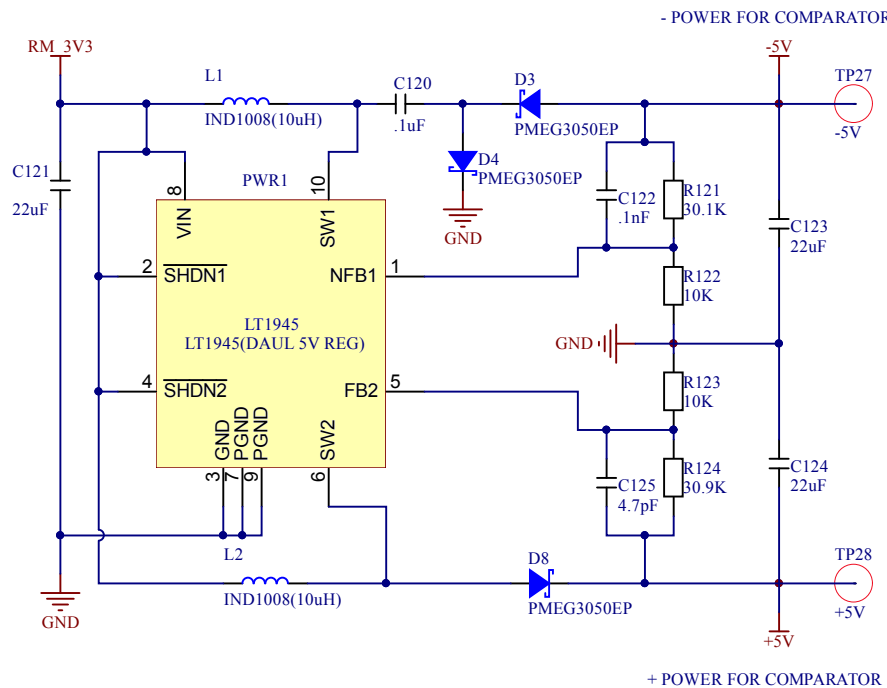
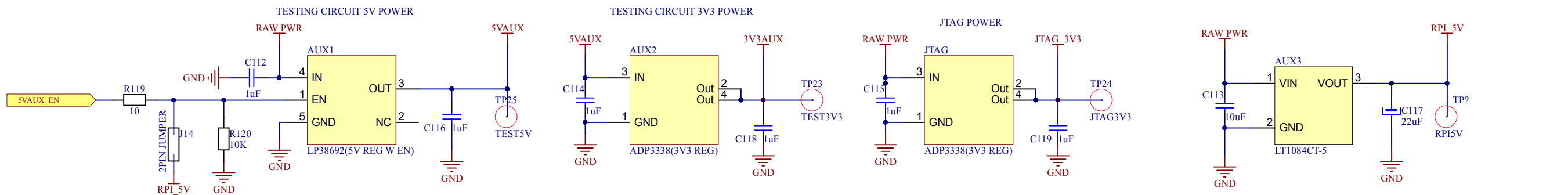
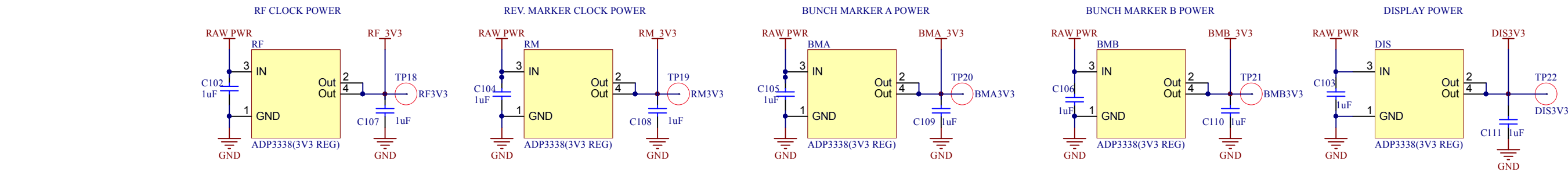
Counter circuit for bench marker B

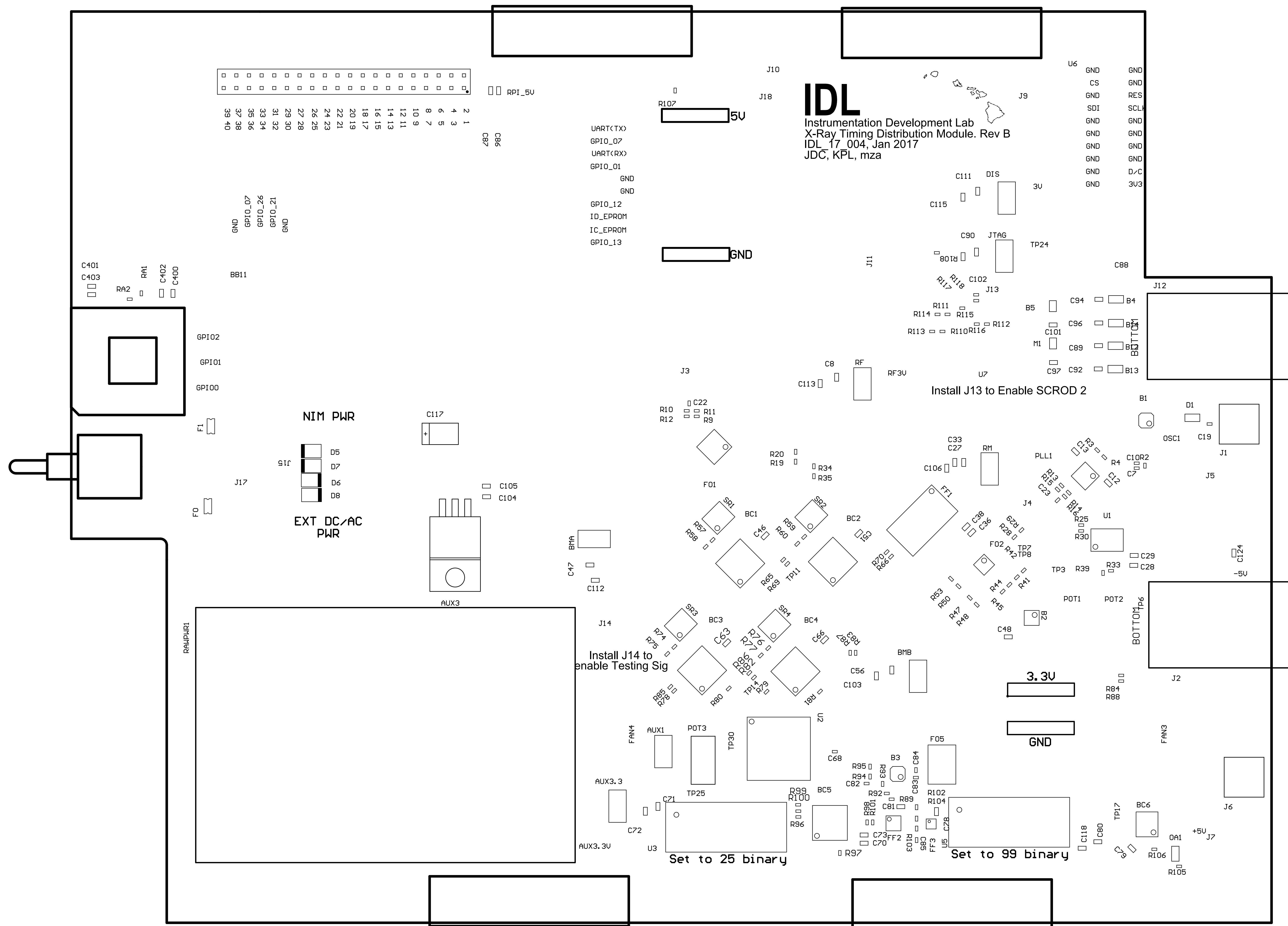




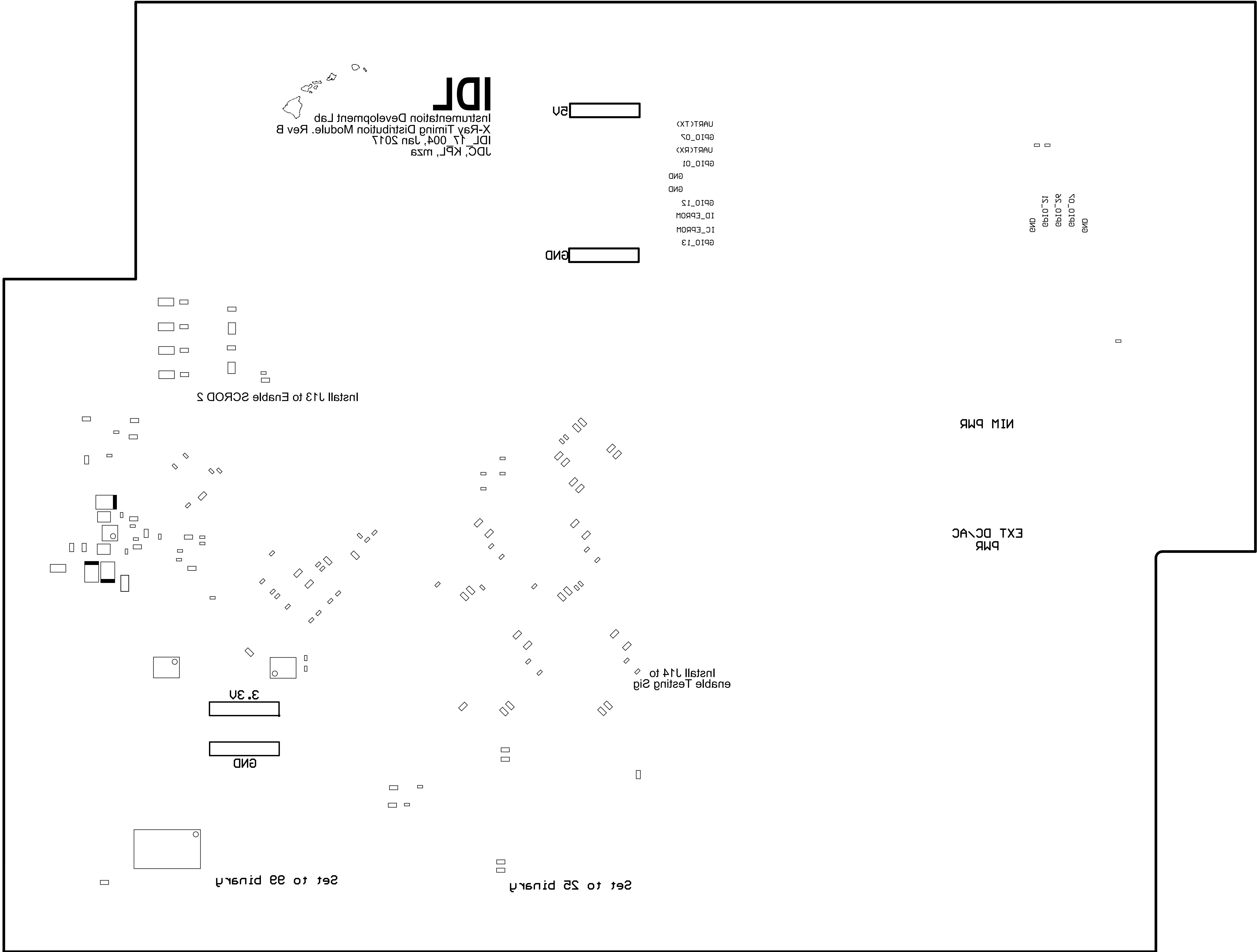
Notes:
 --All 508.9MHz RF clock inside module are LVPECL logic
 --All 127MHz RF clock outputs are LVDS logic
 --Install R#-# if pull up is needed

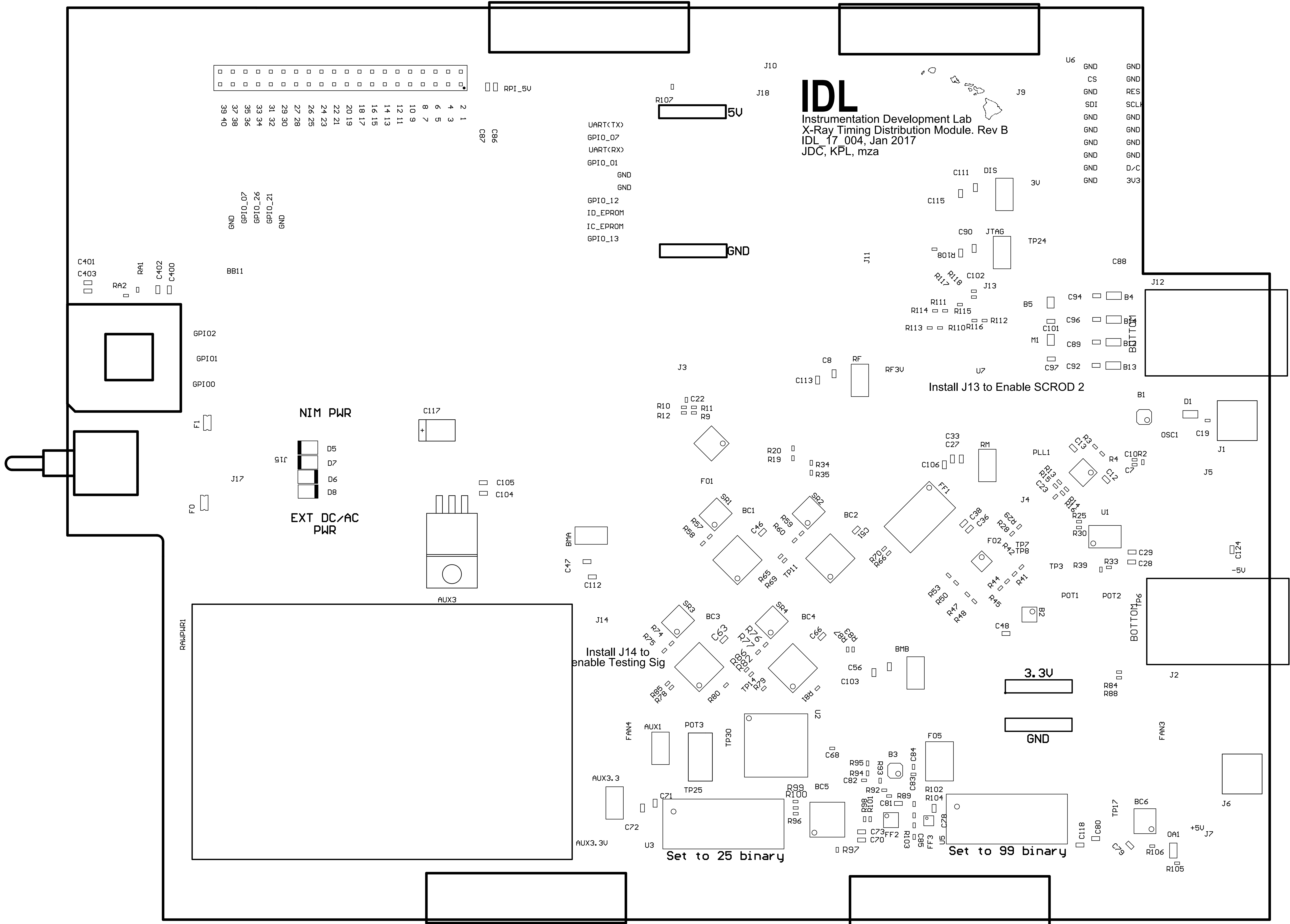


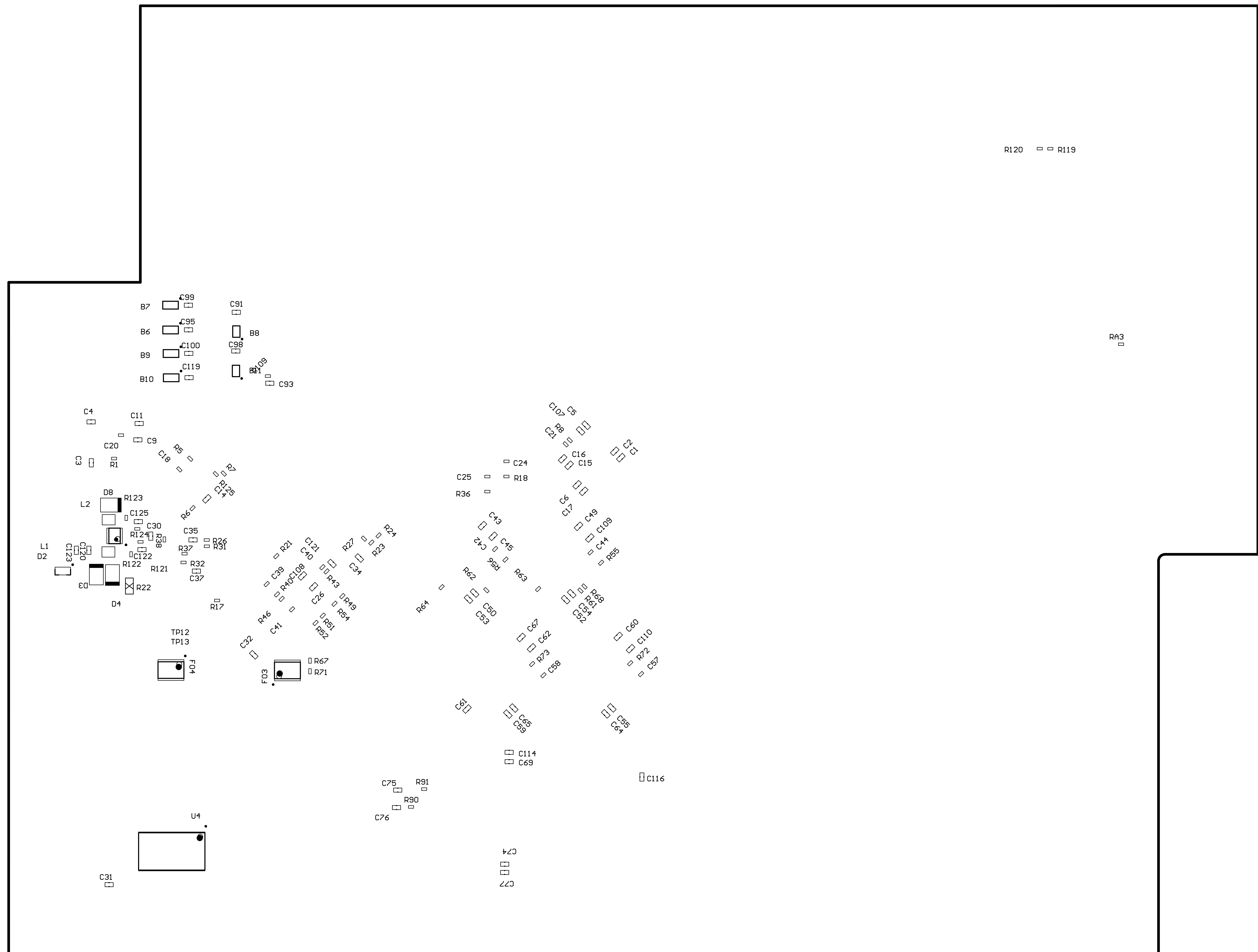




Designer: KHANH LE	Revision: REV B	File: idl_17_001_A9	Sheet 1 of 1	Code: IDL_017_004
Drawn By: JULIEN C	Modif. Date: Date	Variant: [No Variations]	ASSEMBLY	
Approved By: Gary S. Varner	Print Date: 2/6/2017	Gary S. Varner	Size: A3 H	ID: XTD Module
Title: XTD MODULE				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory







- Notes:
- Board shall be fabricated - performance class II as per IPC-6011 and IPC6012
 - PCB manufacturer logo, P/N, revision and/or date code of manufacturing shall be printed in top solder mask (not over pcb traces, allowed over copper plane). The date code shall be in the format: "WWYY" where WW=week and YY= year, max height 0.15 inches
 - Silkscreen on both sides
 - Material: high temperature FR4 class epoxy glass rated UL94V-0. UL symbol and rating shall be marked farside
35um copper for external layers and 18um for all internal layers
Must be RoHS compliant and survive a lead-free assembly max reflow of 260 deg C (5 passes)
Td rating: >340 deg C
Tg = 150 deg C (min)
 - Solder mask: SMOBC per IPC-SM-840C, class T must be Rohs compliant, 0.001" max measured over bare copper plating, must clear all lands as indicated on gerber solder mask layers, color= GREEN
 - Finish: electro-less nickel immersion gold (ENIG), 0.05-0.125 mil Au over 3-6 mil Ni - over bare copper only
 - Solderability test: Category 2 of J-STD-003
 - Finished boards shall not have nicks, scratches, voids, exposed copper, poor plating or misdrilled holes
 - All holes sizes are after plating
 - PCB manufacturer may add copper thieving as needed to improve manufacturability, thieving to be 0.030" round pads at 0.050" spacing.
Thieving will have a minimum of 0.100" clearance from existing copper and should not be placed under surface mounted devices

- PCB manufacturer may use tear drops to improve annular rings as long as DRC rules are followed
- All via connections to power and ground planes are solid
- All unconnected pads on inner signal layers are removed
- All finished boards are to be 100% electrically tested
- Unless otherwise indicated, all linear toleracnes shall be XX.X +/-0.2mm and XX.XX +/- 0.1mm
- Gerber file GM1 shows board outline (milling line)
- Table 1 shows Layer stack details
- Layer 2, 3, 4, 5 are in negative image

Additional notes:

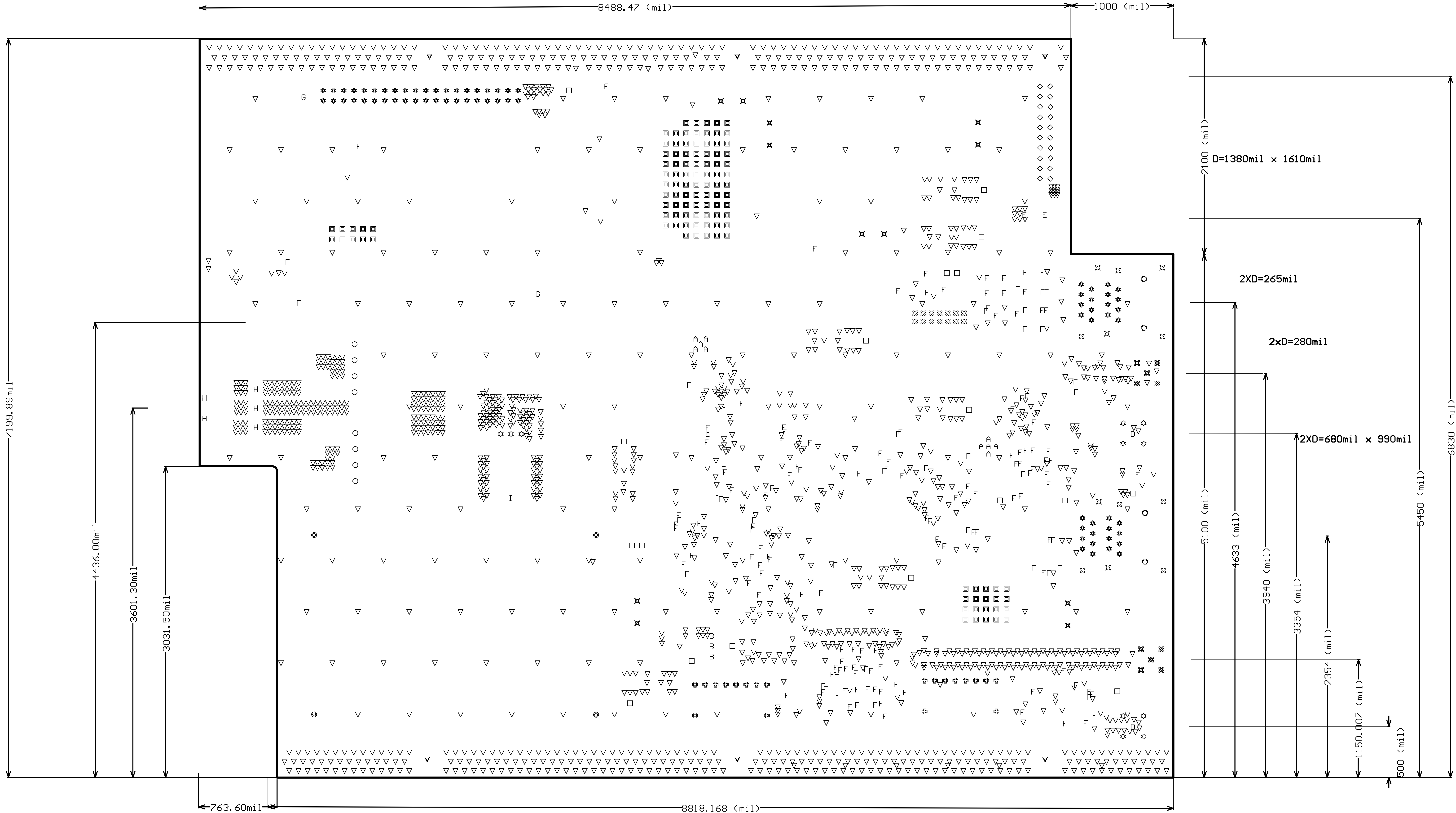
A1. Finished board thickness = 62mils +/- 10%; measured over top/bottom copper and solder mask

Table 1a: Layer Stack Details for IDL_15_039 Rev.A (Imperial Units)

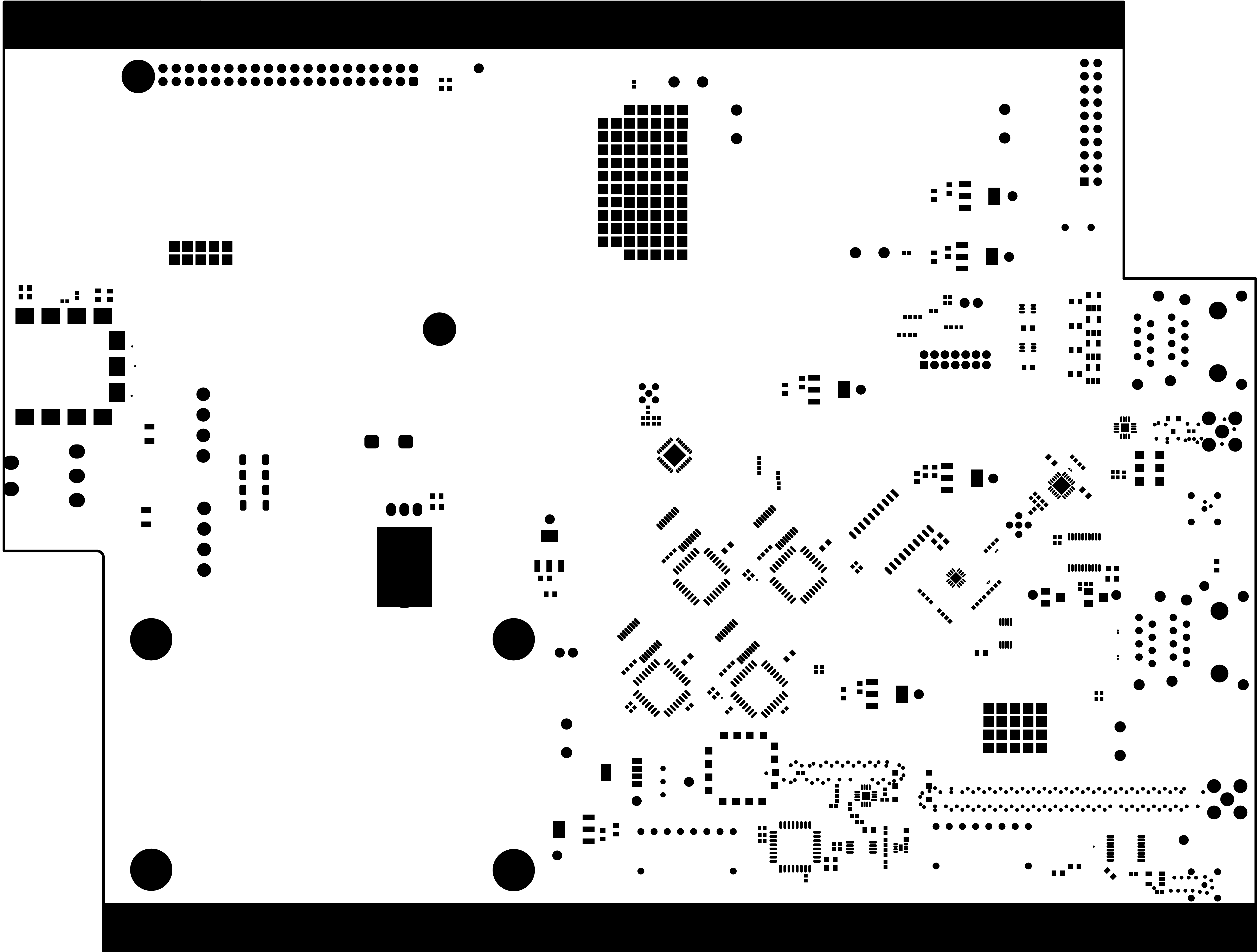
Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack
1	Top Overlay					
2	Top Solder	Solder Resist	0.40mil	3.5		
3	Top Layer - SI61	Copper	1.38mil			
4	Dielectric 1	FR-4	9.00mil	4.6		
5	Layer 2 - GND1	Copper	0.71mil			
6	Dielectric 2	FR-4	14.00mil	4.6		
7	Layer 3 - PWR1	Copper	0.71mil			
8	Dielectric 3	FR-4	9.00mil	4.2		
9	Layer 4 - PWR2	Copper	0.71mil			
10	Dielectric 4	FR-4	14.00mil	4.6		
11	Layer 5 - GND2	Copper	0.71mil			
12	Dielectric 5	FR-4	9.00mil	4.6		
13	Bottom Layer - SI62	Copper	1.38mil			
14	Bottom Solder	Solder Resist	0.40mil	3.5		
15	Bottom Overlay					

Table 2: NC Drill Details for IDL_15_039 Rev.A

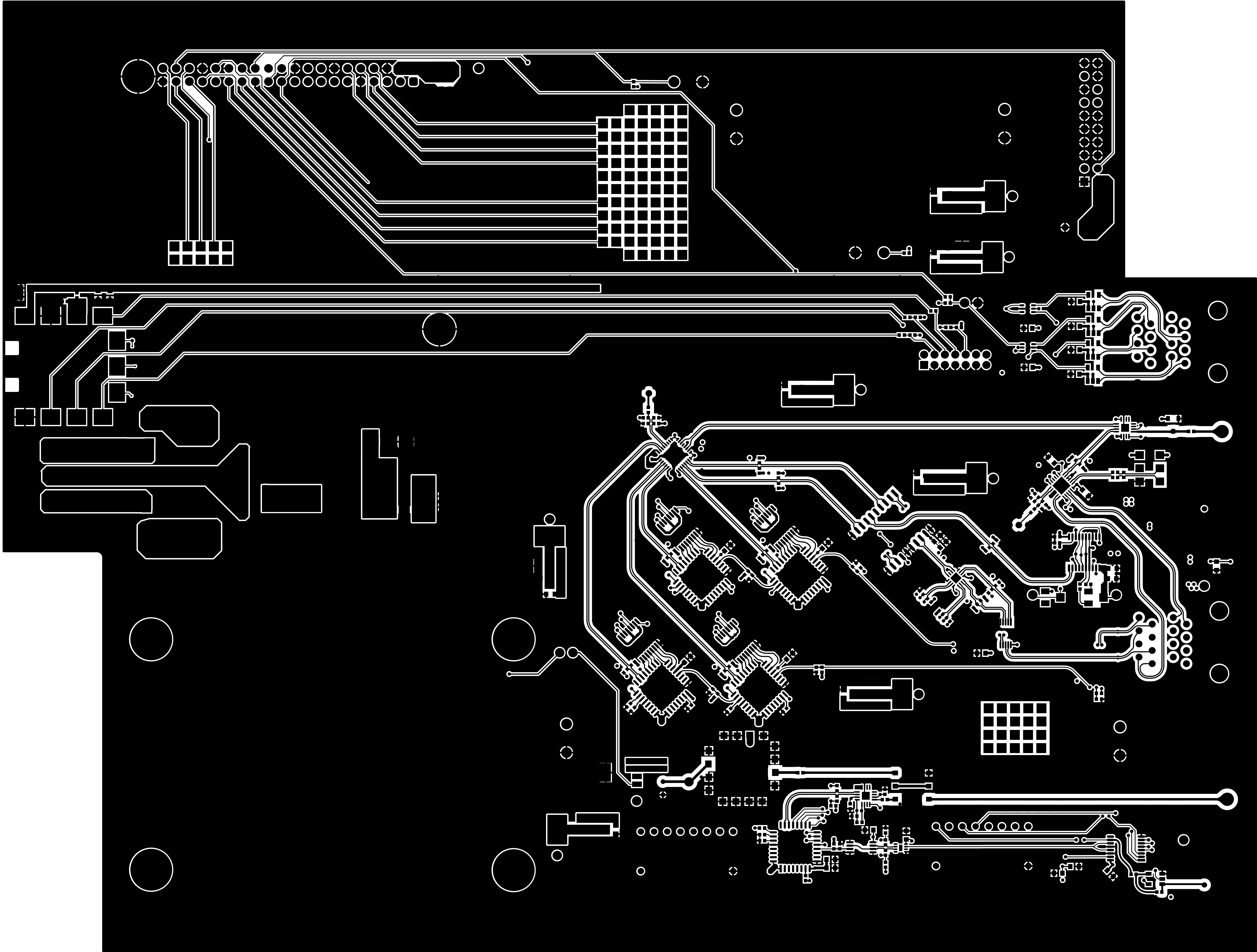
Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
I	1	125.98mil (3.200mm)	PTH	Round
D	2	27.56mil (0.700mm)	PTH	Round
E	2	28.00mil (0.711mm)	PTH	Round
G	2	108.27mil (2.750mm)	PTH	Round
B	3	25.00mil (0.635mm)	PTH	Round
⊕	4	130.00mil (3.302mm)	NPTH	Round
⊙	4	157.48mil (4.000mm)	PTH	Round
H	5	72.83mil (1.850mm)	PTH	Round
▽	6	152.00mil (3.861mm)	PTH	Round
○	8	70.87mil (1.800mm)	PTH	Round
A	10	33.07mil (0.840mm)	PTH	Round
⊗	10	70.00mil (1.778mm)	PTH	Round
☆	11	39.37mil (1.000mm)	PTH	Round
✕	12	60.00mil (1.524mm)	PTH	Round
⊗	12	66.93mil (1.700mm)	PTH	Round
⊗	14	33.00mil (0.838mm)	PTH	Round
□	18	50.00mil (1.270mm)	PTH	Round
⊕	20	31.50mil (0.800mm)	PTH	Round
◇	20	41.00mil (1.041mm)	PTH	Round
★	72	35.43mil (0.900mm)	PTH	Round
▣	110	40.00mil (1.016mm)	PTH	Round
F	163	11.81mil (0.300mm)	PTH	Round
▽	1686	12.00mil (0.305mm)	PTH	Round
	2195 Total			



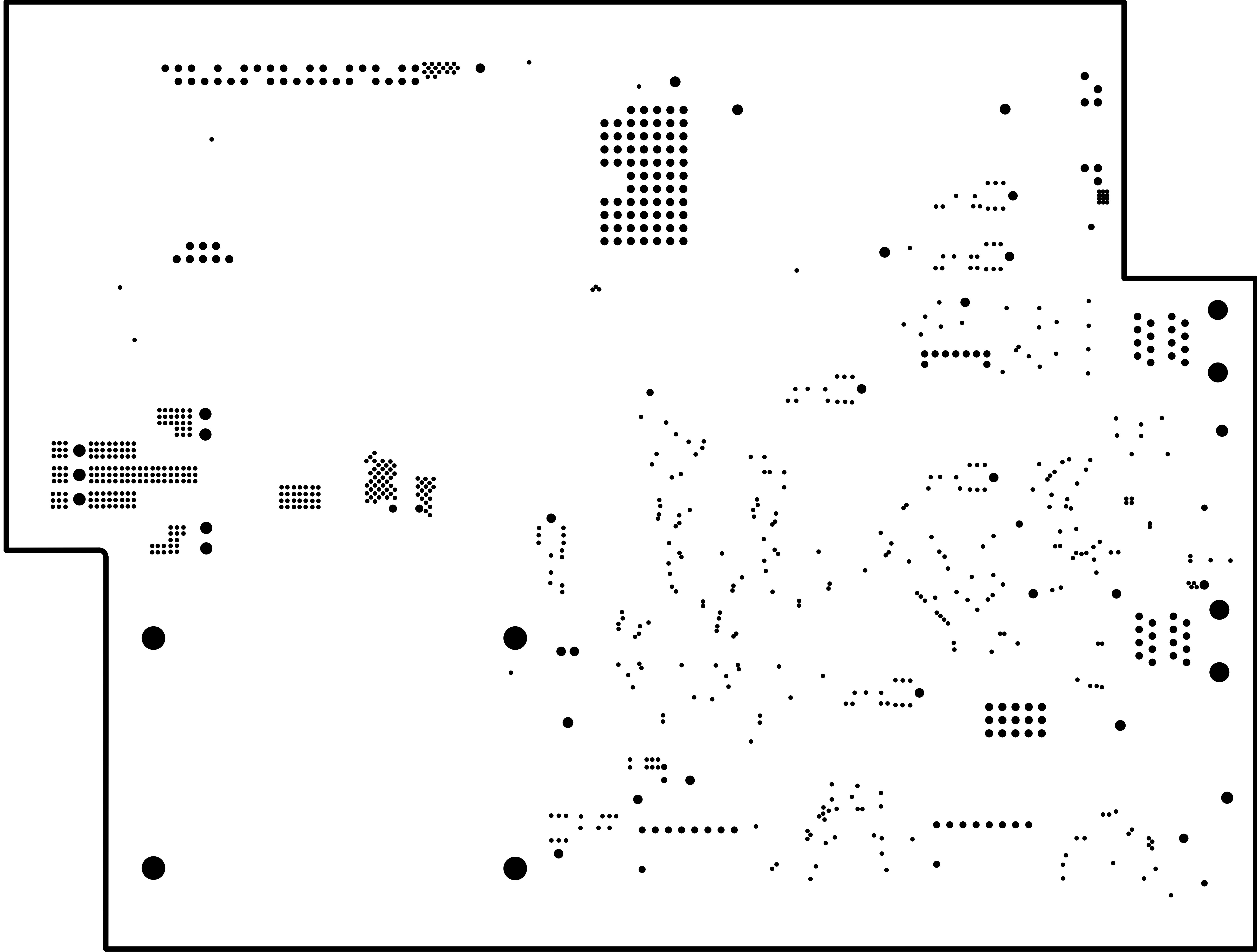
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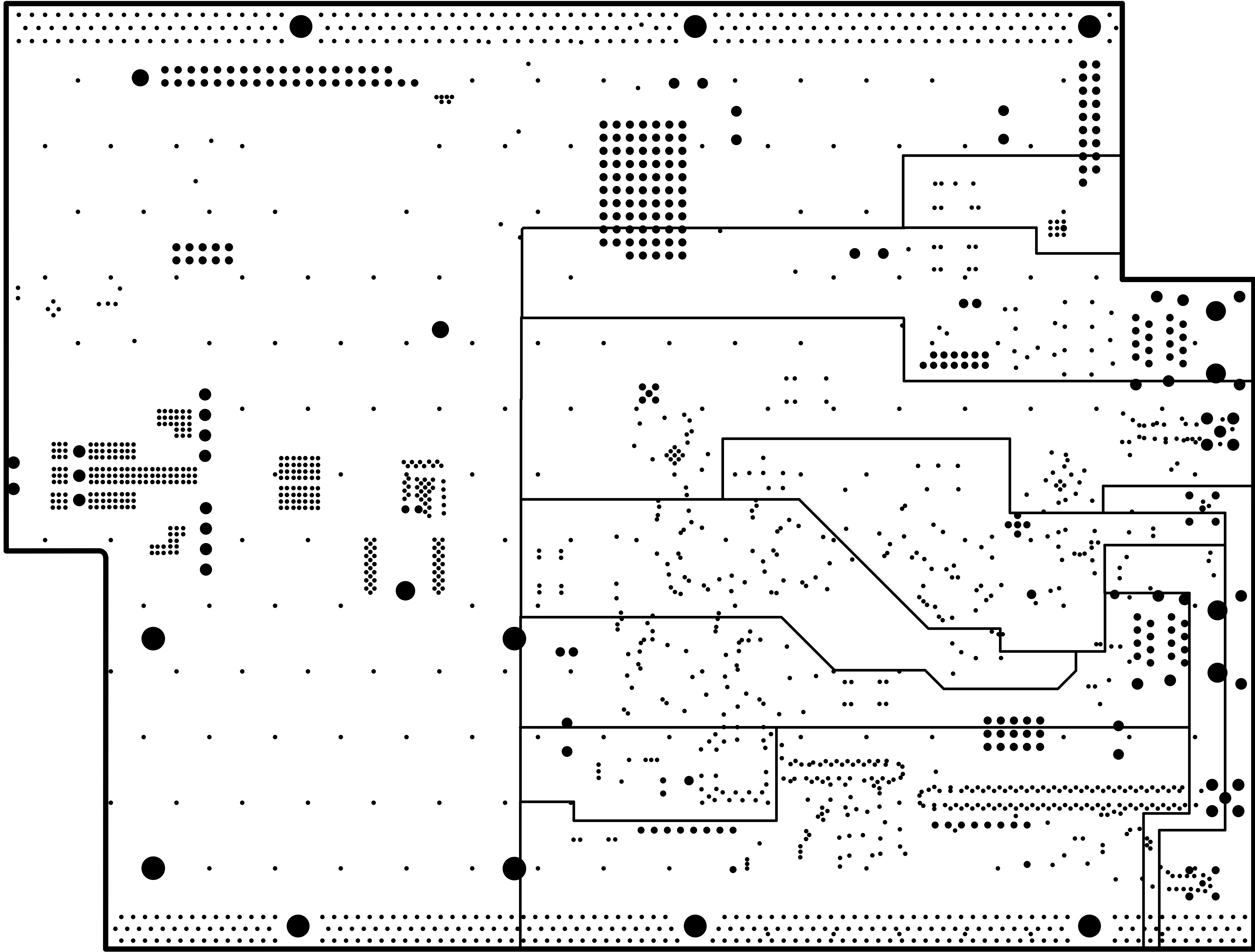
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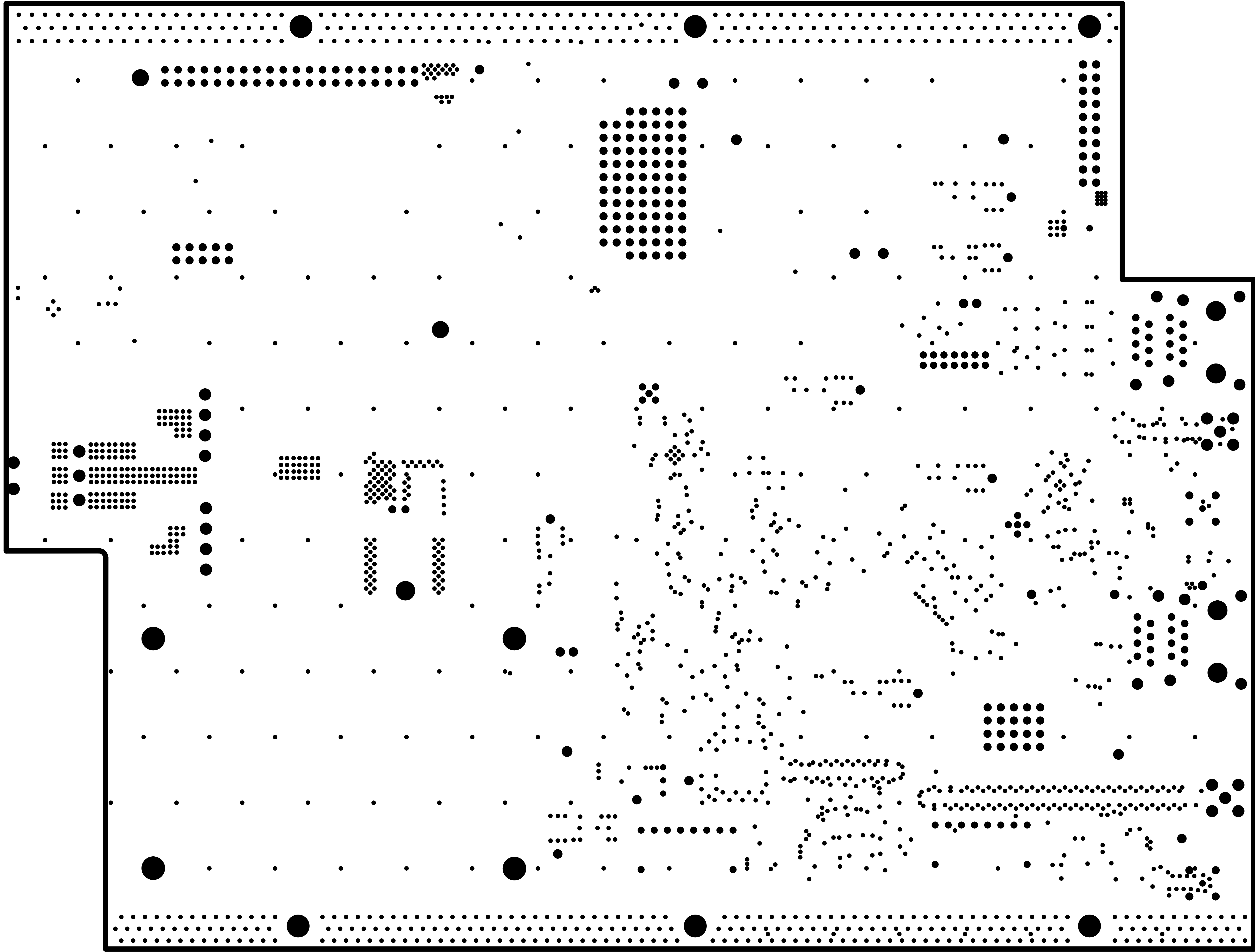
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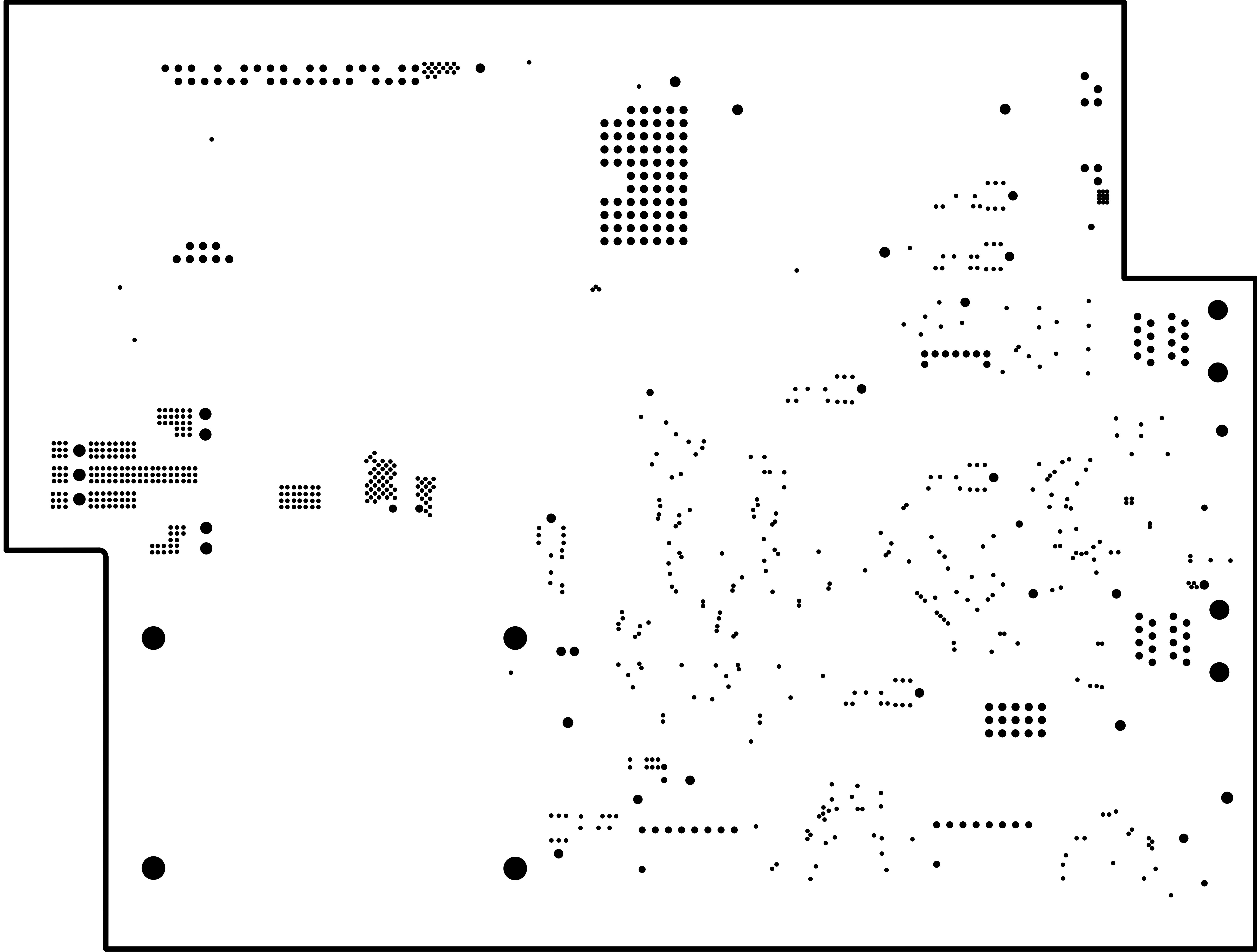
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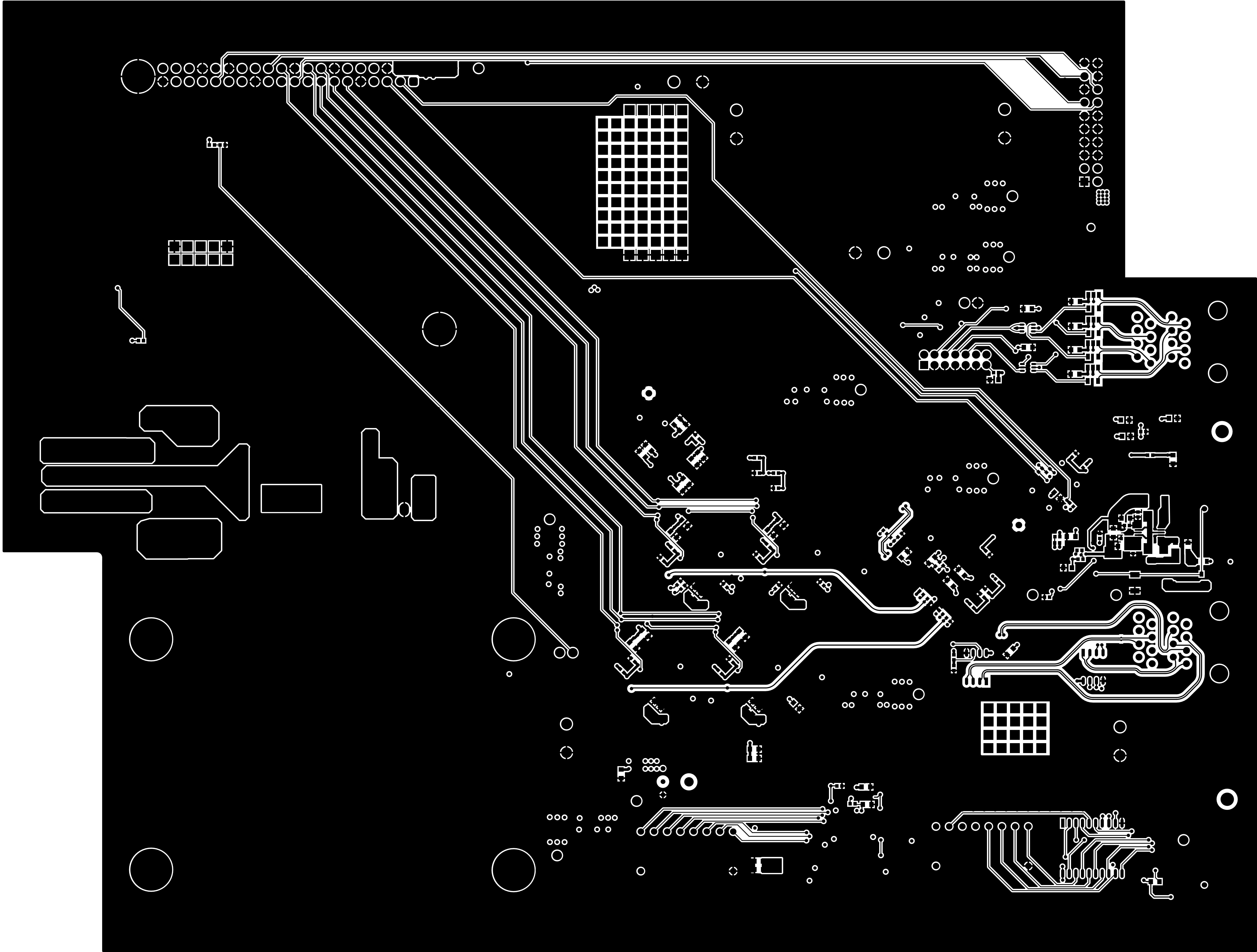
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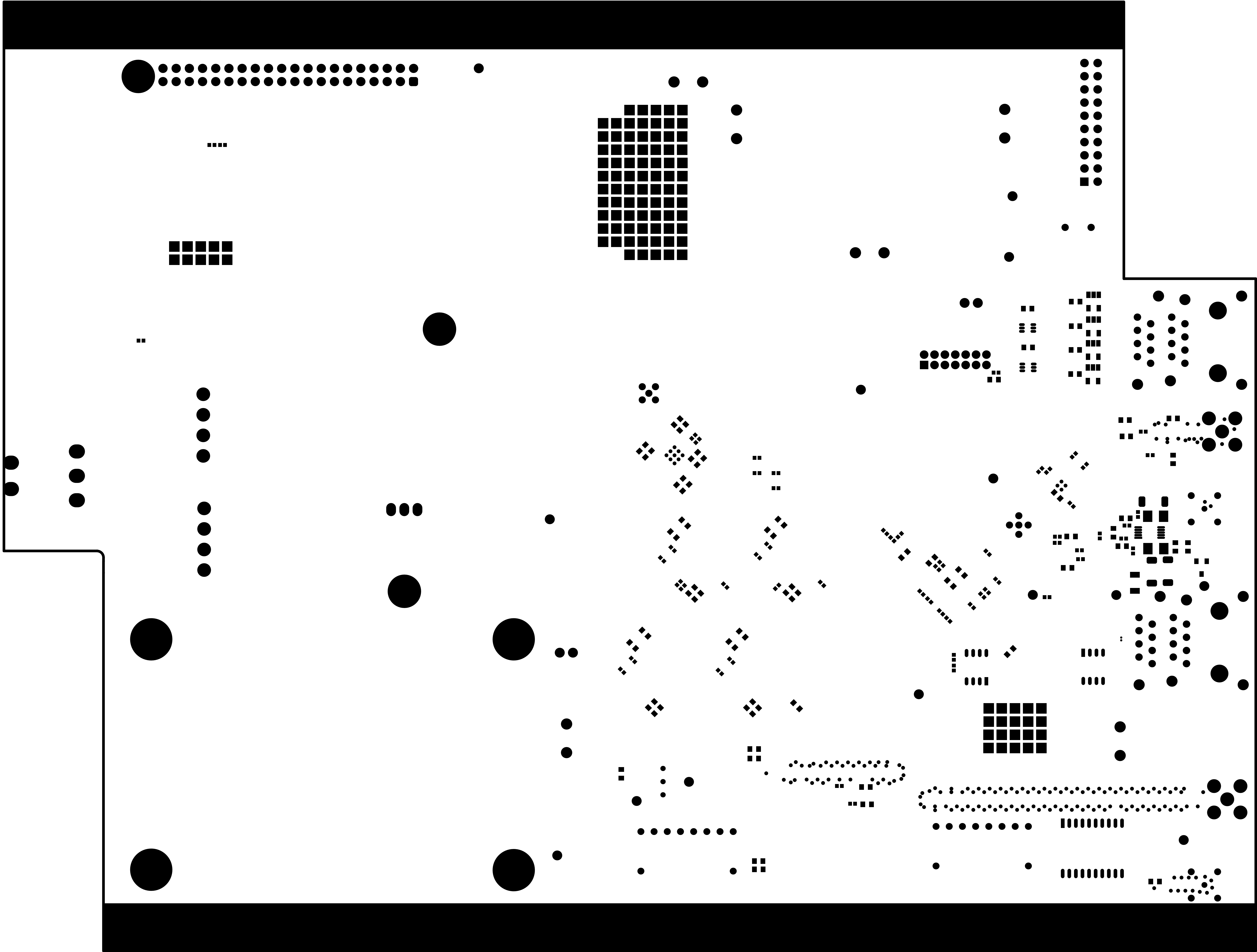
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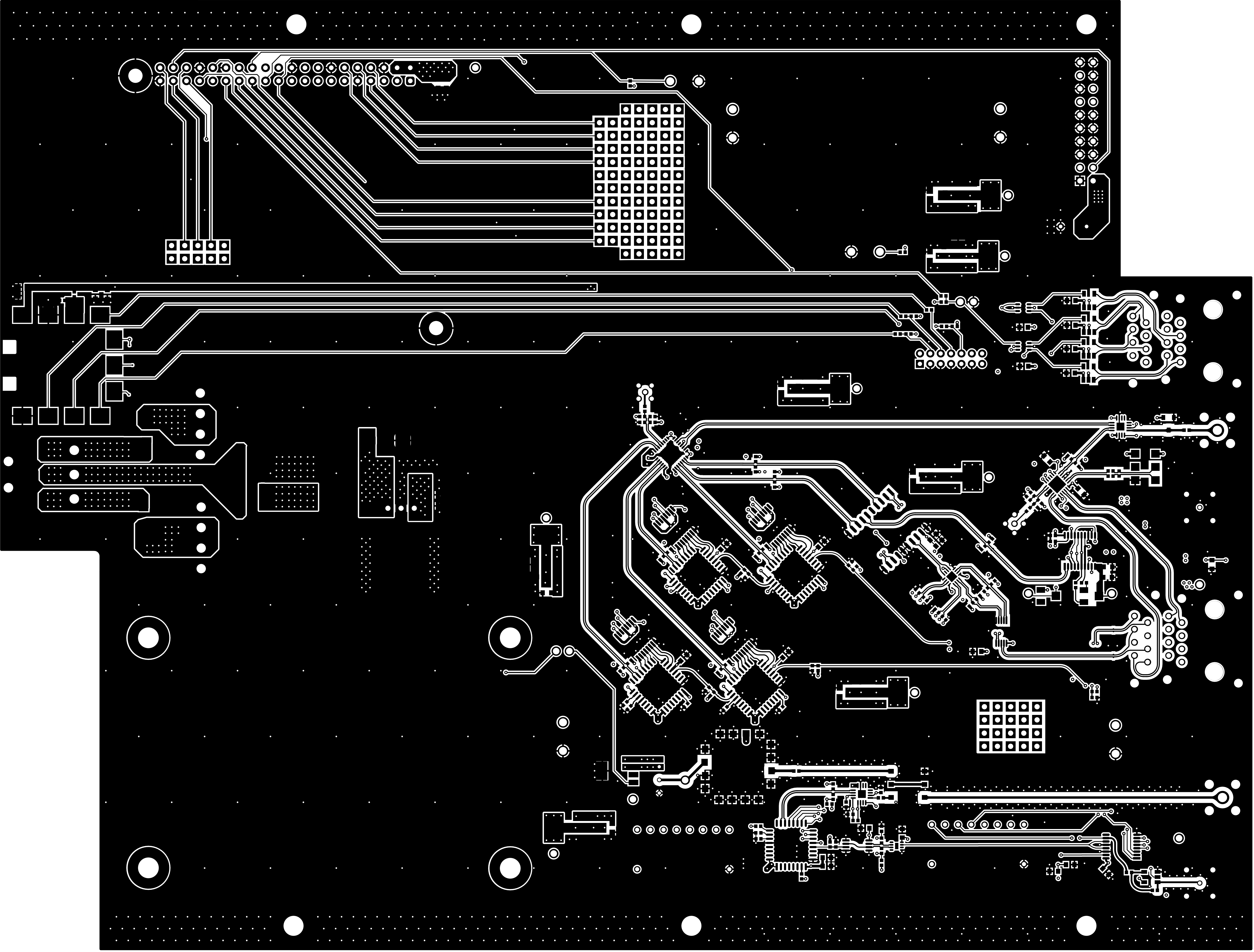
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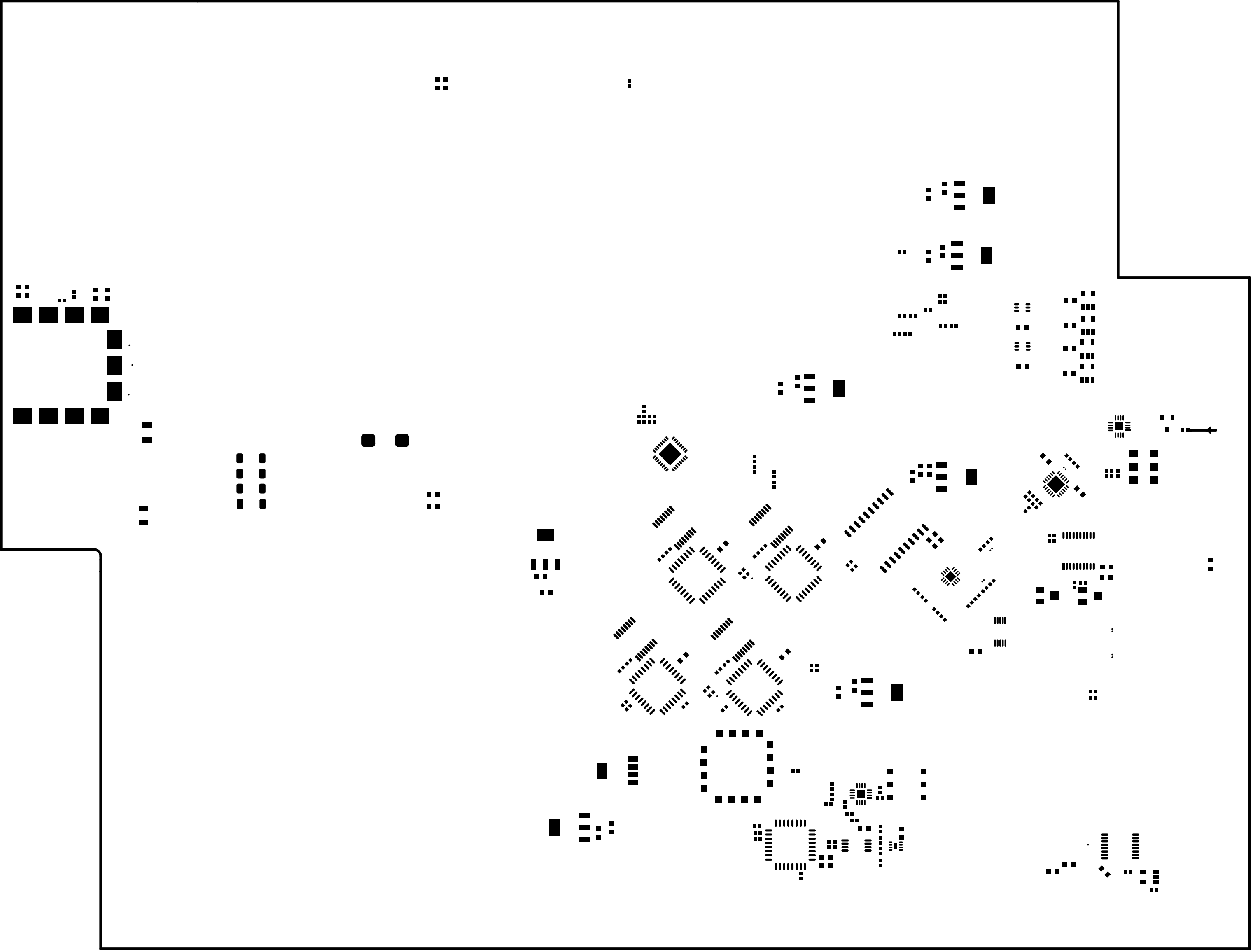


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