

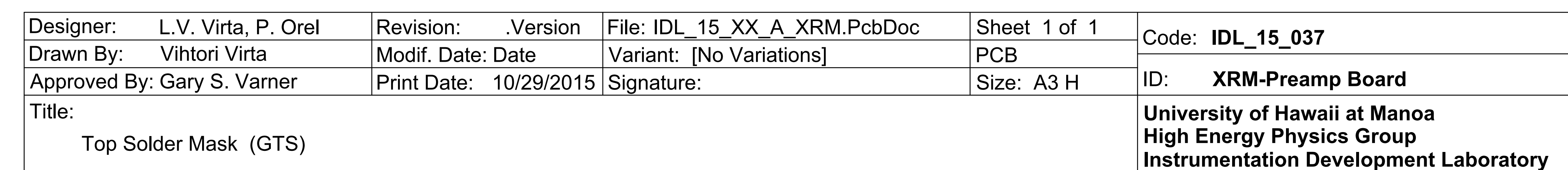
- Notes:
- Board shall be fabricated - performace class II as per IPC-6011 and IPC6012
  - PCB manufacturer logo, P/N, revision and/or date code of manufacturing shall be printed in top solder mask (not over pcb traces, allowed over copper plane). The date code shall be in the format: "WWYY" where WW=week and YY= year, max height 0.15 inches
  - Silkscreen printed on both sides
  - Material: high temperature FR4 class epoxy glass rated UL94V-0. UL symbol and rating shall be marked farside  
35um copper for external and internal layers  
Must be RoHS compliant and survive a lead-free assembly max reflow of 260 deg C (5 passes)  
Td rating: >340 deg C  
Tg = 150 deg C (min)
  - Solder mask: SMOBC per IPC-SM-840C, class T must be Rohs compliant, 0.001" max measured over bare copper plating, must clear all lands as indicated on gerber solder mask layers, color= GREEN
  - Finish: electro-less nickel immersion gold (ENIG), 0.05-0.125um Au over 3-6um Ni - over bare copper only
  - Solderability test: Category 2 of J-STD-003
  - Finished boards shall not have nicks, scratches, voids, exposed copper, poor plating or misdrilled holes
  - All holes sizes are after plating
  - PCB manufacturer may add copper thieving as needed to improve manufacturability, thieving to be 0.030" round pads at 0.050" spacing. Thieving will have a minimum of 0.100" clearance from existing copper and should not be placed under surface mounted devices
  - PCB manufacturer may use tear drops to improve annular rings as long as DRC rules are followed
  - All via connections to power and ground planes are solid
  - All unconnected pads on inner signal layers are removed
  - All finished boards are to be 100% electrically tested
  - Unless otherwise indicated, all linear toleracnes shall be XX.X +/-0.2mm and XX.XX +/- 0.1mm
  - Gerber file GM1 shows board outline (milling line)
  - Table 1 shows Layer stack details

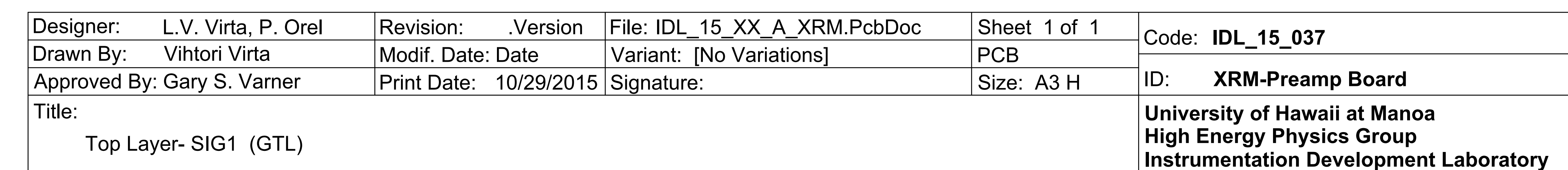
Additional notes:  
A1. Finished board thickness = 1.6mm +/- 0.1mm; measured over top/bottom copper and solder mask

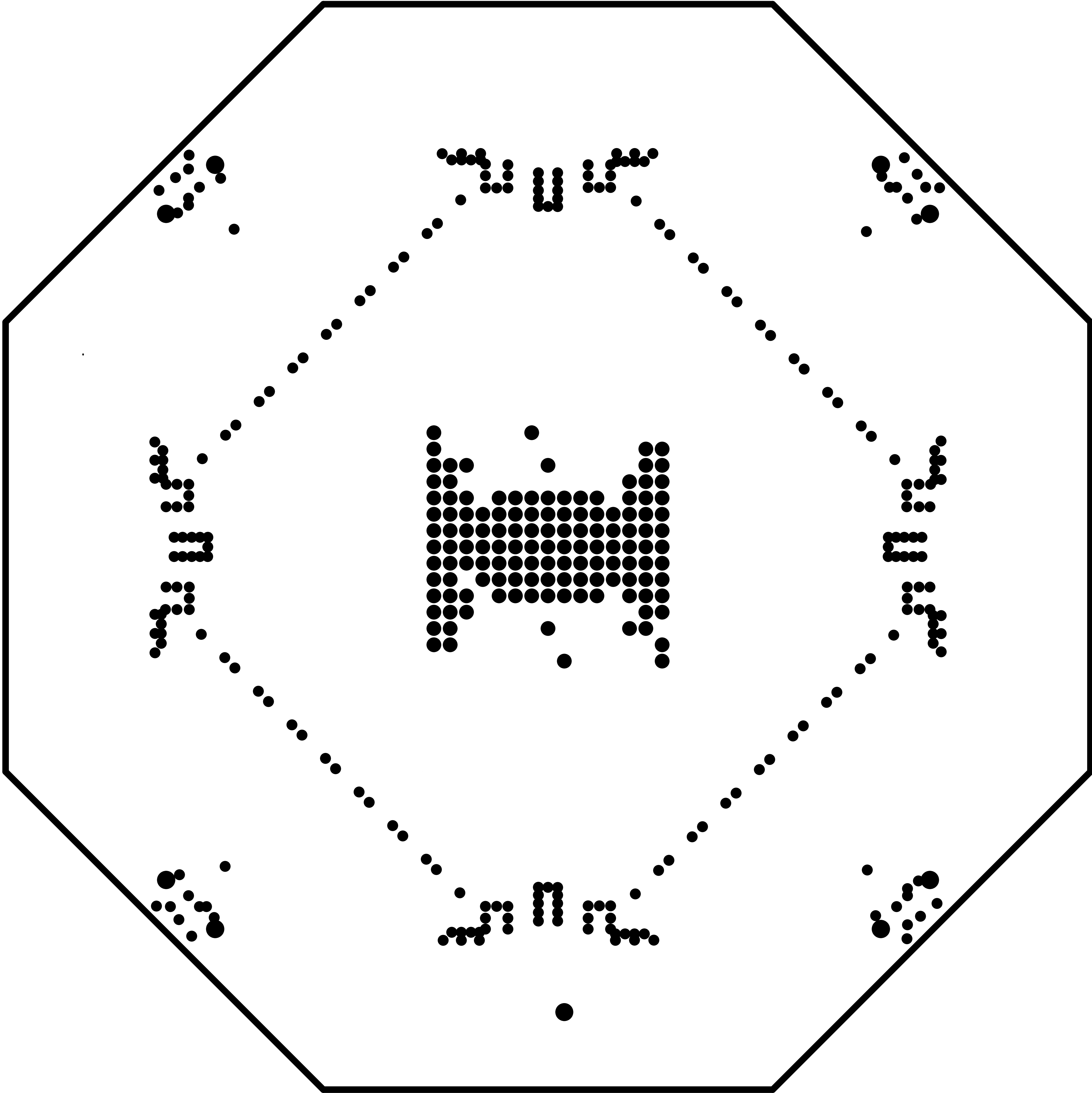
Table 1a: Layer Stack Details for IDL\_15\_37 Rev.A (Metric Units)

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack
1	Top Overlay					
2	Top Solder	Solder Resist	0.010mm	3.5		
3	Top Layer - SIG1	Copper	0.035mm			
4	Dielectric 1	FR-4	0.150mm	4.65		
5	Layer 2 - GND1	Copper	0.035mm			
6	Dielectric 3	FR-4	0.430mm	4.65		
7	Layer 3 - PWR	Copper	0.035mm			
8	Dielectric 6	FR-4	0.150mm	4.65		
9	Layer 4 - PWR	Copper	0.035mm			
10	Dielectric 5	FR-4	0.430mm	4.65		
11	Layer 5 - GND2	Copper	0.035mm			
12	Dielectric 4	FR-4	0.150mm	4.65		
13	Bottom Layer - SIG4	Copper	0.035mm			
14	Bottom Solder	Solder Resist	0.010mm	3.5		
15	Bottom Overlay					

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Technology
○	2	1.400mm (55.12mil)	PTH	Round	Top Layer - SIG1 - Bottom Layer - SIG4	Pad	*	Drilled
✕	8	0.830mm (32.68mil)	PTH	Round	Top Layer - SIG1 - Bottom Layer - SIG4	Pad	Rounded	Drilled
✱	8	1.450mm (57.09mil)	NPTH	Round	Top Layer - SIG1 - Bottom Layer - SIG4	Pad	Rounded	Drilled
⊠	8	3.300mm (129.92mil)	PTH	Round	Top Layer - SIG1 - Bottom Layer - SIG4	Pad	Rounded	Drilled
□	225	0.900mm (35.43mil)	PTH	Round	Top Layer - SIG1 - Bottom Layer - SIG4	Pad	Rounded	Drilled
▽	392	0.300mm (11.81mil)	PTH	Round	Top Layer - SIG1 - Bottom Layer - SIG4	Via	Rounded	Drilled
	643 Total							

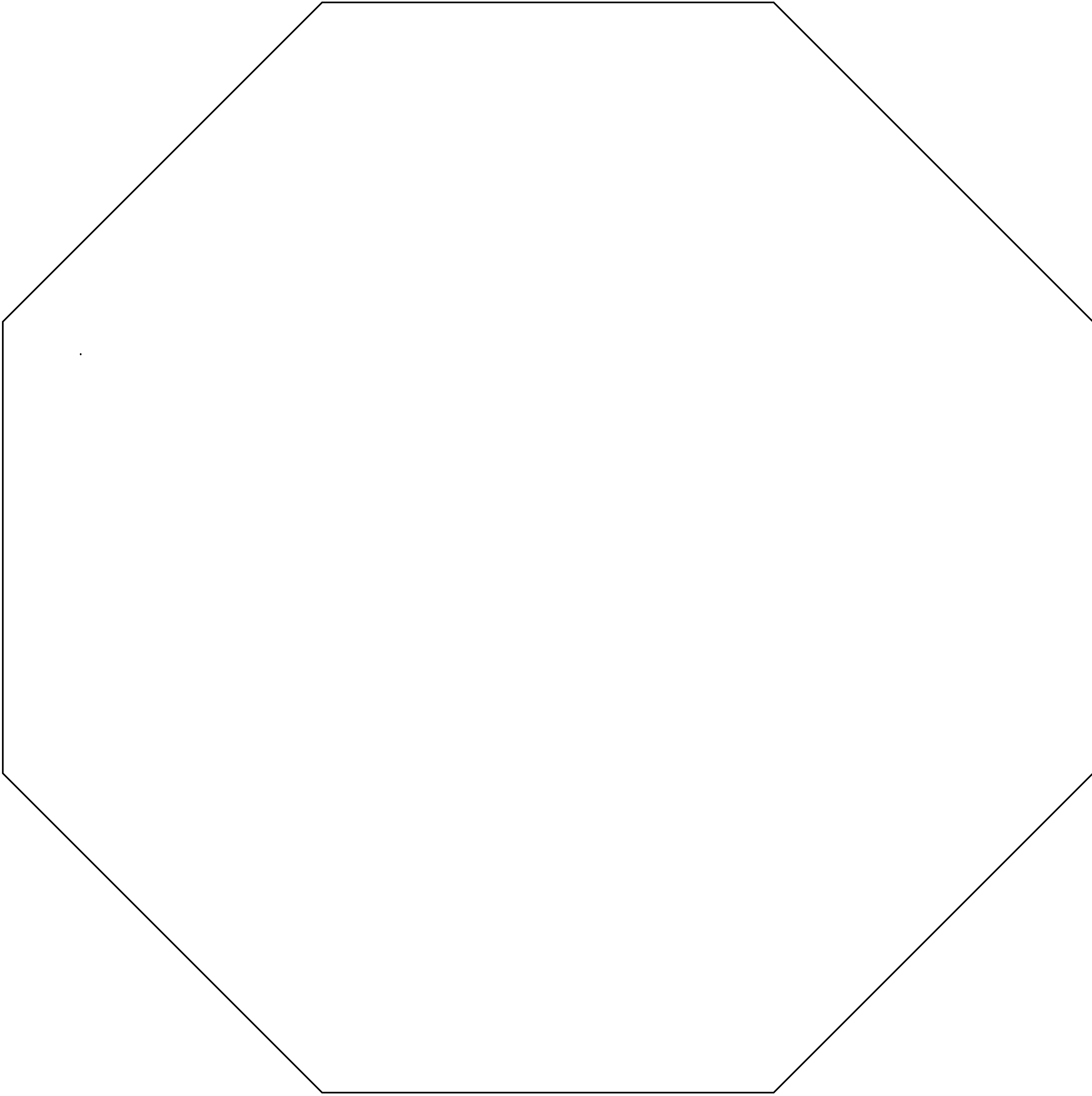




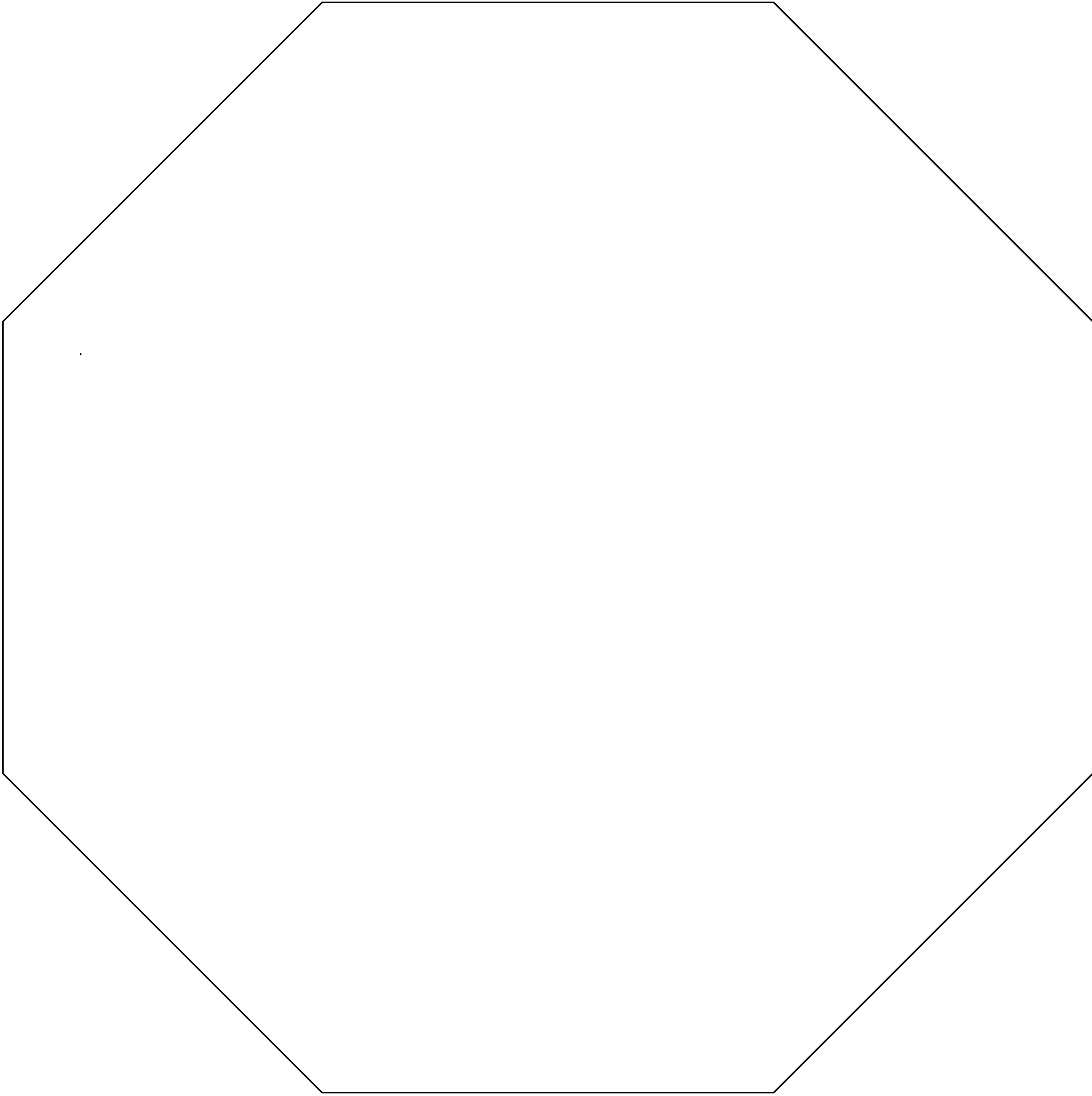


Designer:	L.V. Virta, P. Orel	Revision:	.Version	File:	IDL_15_XX_A_XRM.PcbDoc	Sheet	1 of 1	Code:	IDL_15_037
Drawn By:	Vihtori Virta	Modif. Date:	Date	Variant:	[No Variations]	PCB			
Approved By:	Gary S. Varner	Print Date:	10/29/2015	Signature:		Size:	A3 H	ID:	XRM-Preamp Board
Title: Layer 2 - GND1 (GP1)									University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory

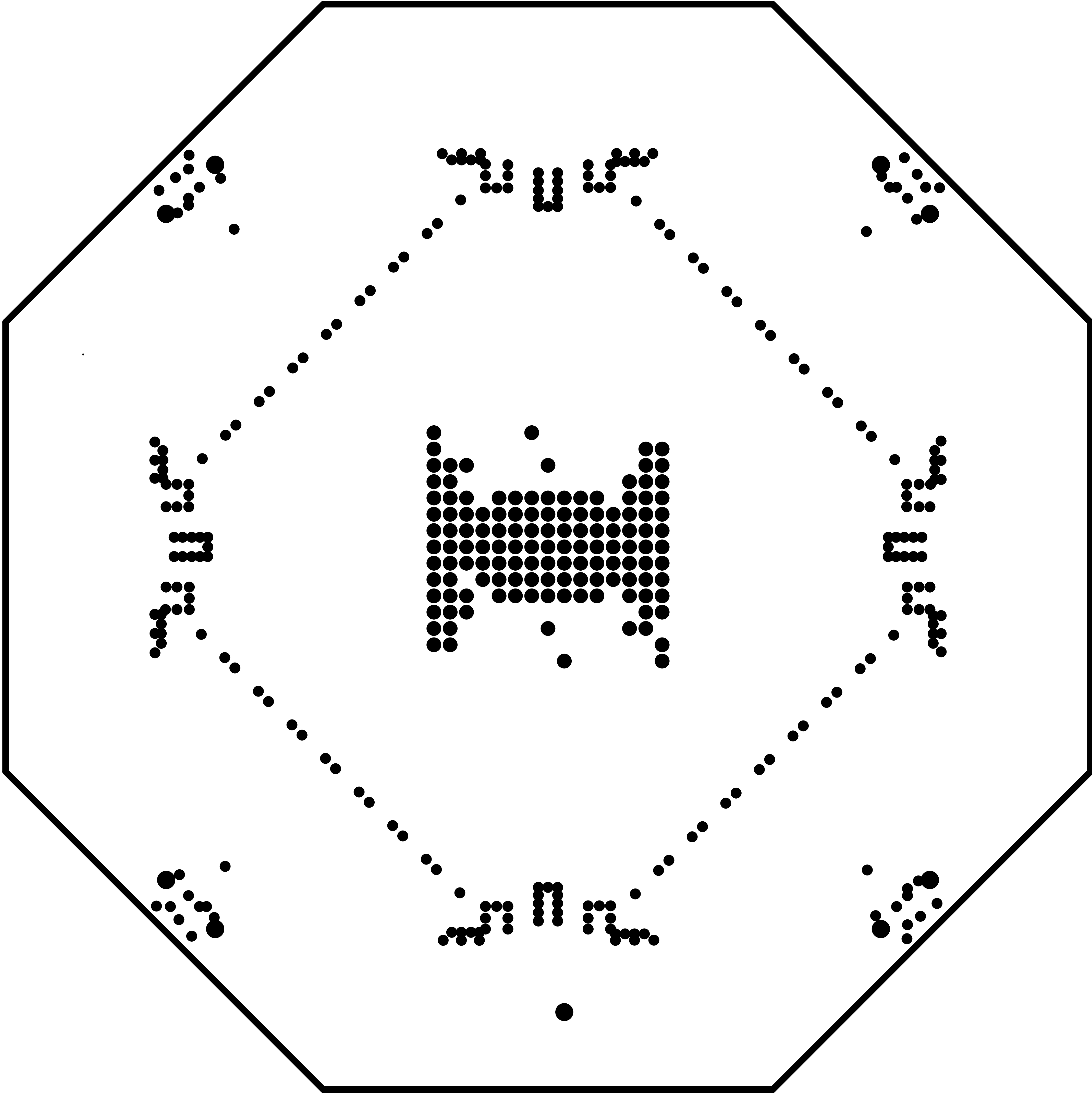


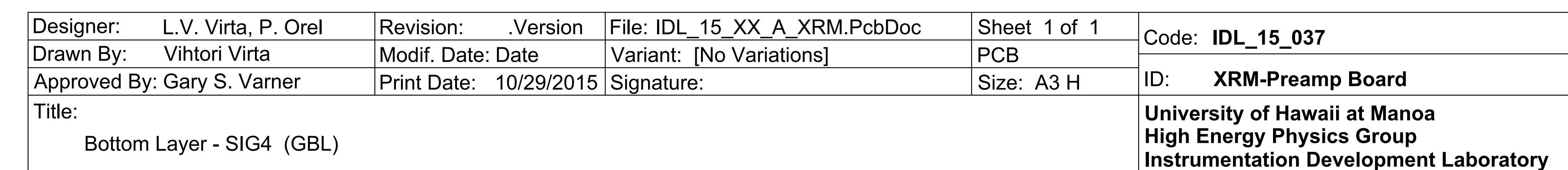


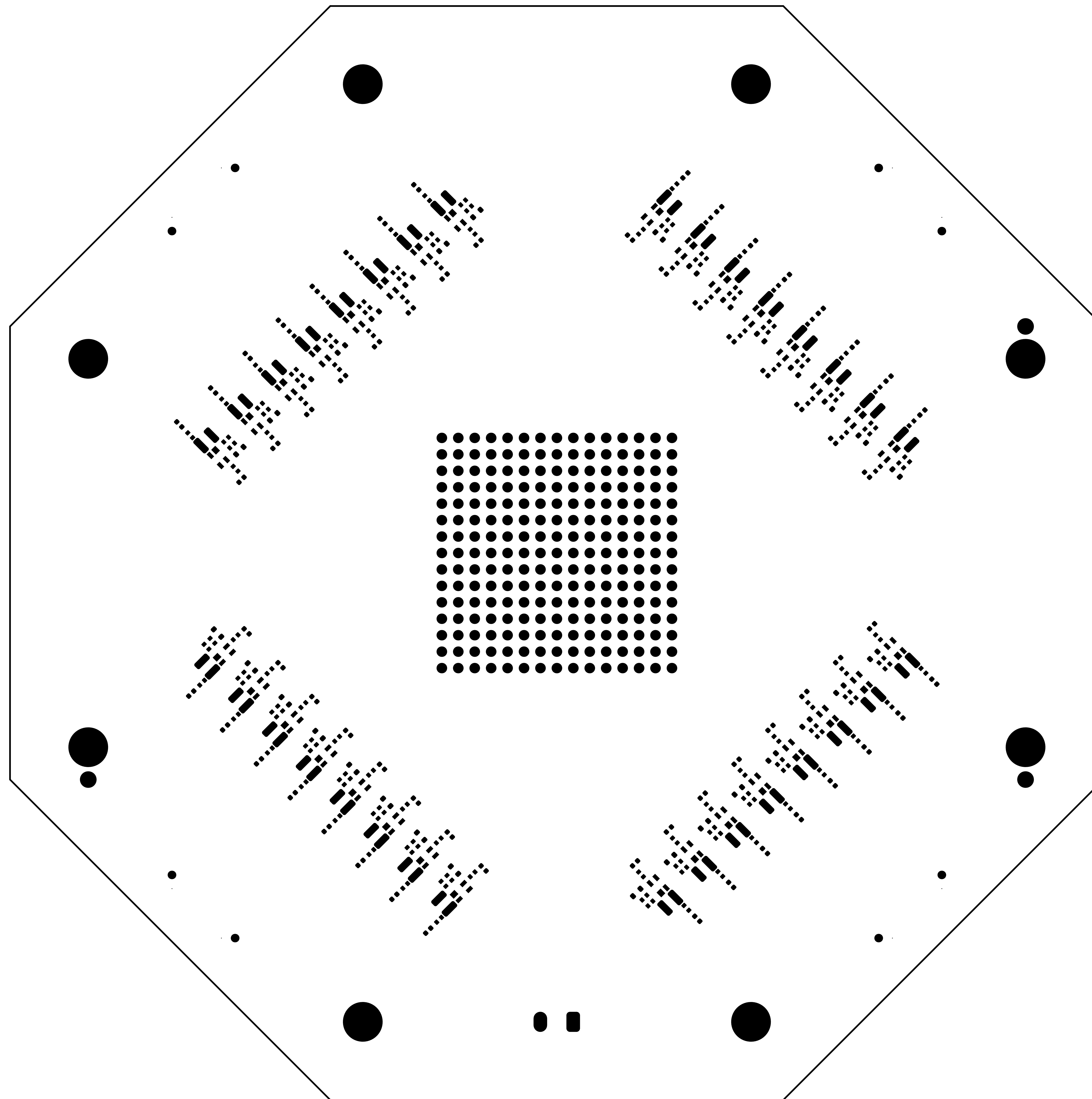
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Approved By:	Gary S. Varner	Print Date:	10/29/2015	Signature:		Size:	A3 H	ID:	XRM-Preamp Board
Title: Layer 3 - SIG2 (G1)								University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory	



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Approved By:	Gary S. Varner	Print Date:	10/29/2015	Signature:		Size:	A3 H	ID:	XRM-Preamp Board
Title: Layer 4 - SIG2 (G2)								University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory	







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Drawn By: Vihtori Virta	Modif. Date: Date	Variant: [No Variations]	PCB	
Approved By: Gary S. Varner	Print Date: 10/29/2015	Signature:	Size: A3 H	
Title: Bottom Solder Mask (GBS)				<b>ID: XRM-Preamp Board</b> <b>University of Hawaii at Manoa</b> <b>High Energy Physics Group</b> <b>Instrumentation Development Laboratory</b>