10/02

CLK_FANOUT:

Changed layer stack:

* Top, 5V, 3.3V, 2.5V power planes
* GND 1 (Solid)
* LVDS 1 (Routing)
* GND 2 (Solid)
* LVDS 2 (Routing)
* Bottom, GND, Solid

- removed 1 to 4 clock fanout
- rearrenged the buffers to clean the routing

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CLK_FANOUT:

- Added 2 layers,

* Top
* GND1
* LVDS
* Power
* GND2
* Bottom

Motherboard:

- Added more clearance around mounting holes
- Added adjustable regulators to provide VPED and Downbonds to fermionics sensor box

Carrier:

- All signal planes flooded with copper
- added another 5 volt power plane

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CLK_FANOUT:

- 127 MHZ fanout to:
    * Clock divider ==> SSTIN
    * SCROD
    * Buffer ==> FPGA's

Carrier:

- CLOCK_TO_ASICS_ON_CARRIER removed. replaced with 127 MHZ clock
- copy of SSTIN to FPGA
- SCROD_TO_CARRIER / CARRIER_TO_SCROD moved to general IO pins

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09/18

CLK_FANOUT:

- Added 3 new LVDS inputs and fanout buffer for each
    * Reset
    * Bunch0
    * Bunch0 offset

- Added clock divider, 127 MHZ input clock divided by 5

Carrier:

- Reset, Bunch0, Bunch0 offset connected to ARTIX

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CLK Fanout:

- RF-45 clock input pins 1-6 not tied to ground
- RJ-45 input/output markings more clear, as well as power connector markings
- clock input traces to differential pair, optimized few other traces
- moved few traces further away from mounting holes
- Silkscreen adjusted, no overlapping markings

Carrier:

- added pullup & pulldown to M0 - m2. resistor grouped together, easy to change if needed
- Silkscreen adjusted, no overlapping markings

Motherboard

- Removed 2.5V, 3.3V and 4V regulators and power planes
- Added copper ares around power and ground input input connectors
- added mounting holes
- added 2 ground testpoints to opposing sides of the boards
- moved carrier power connectors so they align with the connectors on carriers, same thing with clk fanout.
- moved power connectors for the fans
- moved SMA input, so it wont be on the way of the clock cables to carriers
- Silkscreen adjusted, no overlapping markings