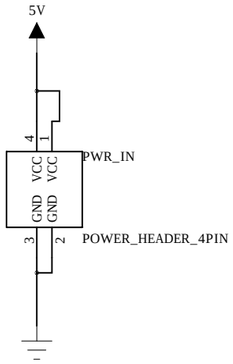
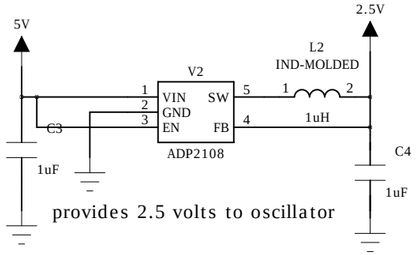
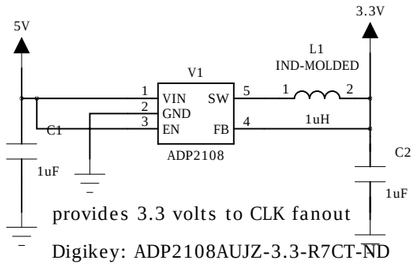




provides 2.5 volts to oscillator

Digikey: ADP2108AUJZ-2.5-R7CT-ND

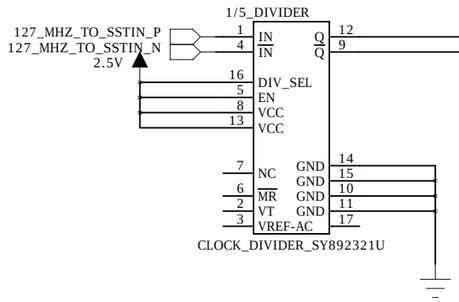


provides 3.3 volts to CLK fanout

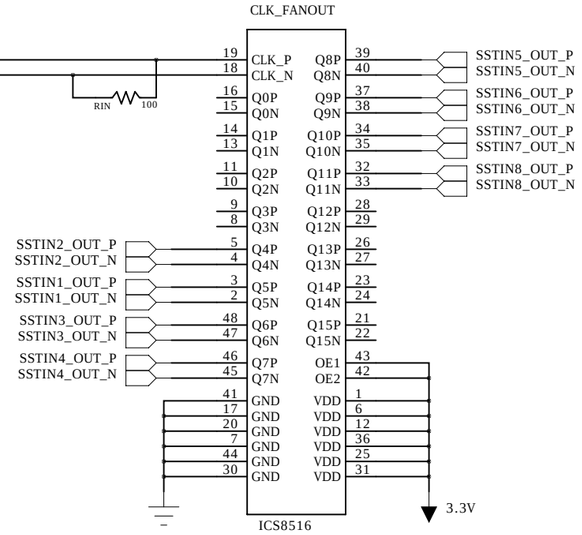
Digikey: ADP2108AUJZ-3.3-R7CT-ND

Clock Divider. 127 MHZ divided by 5

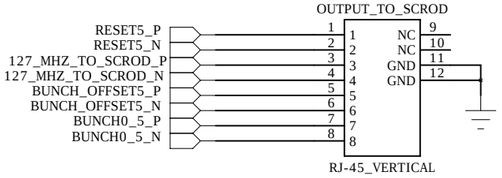
Digikey: 576-2965-5-ND



Clock Fanout circuit

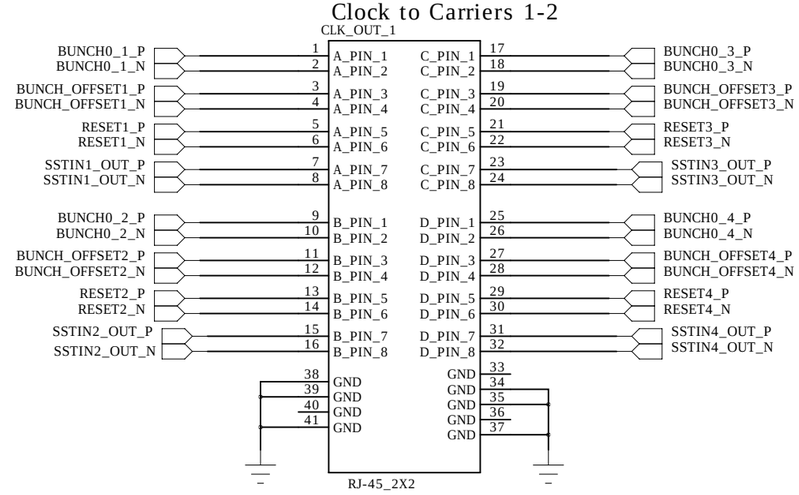


Clock to SCROD

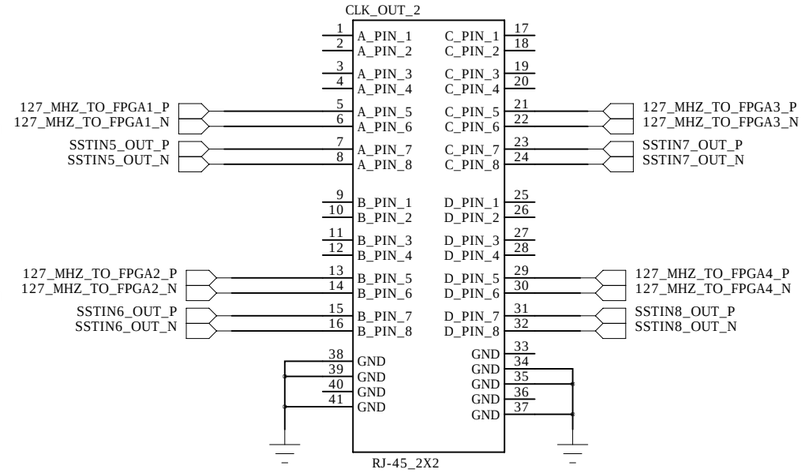


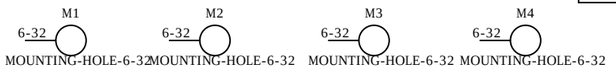
Digikey: 609-4633-ND

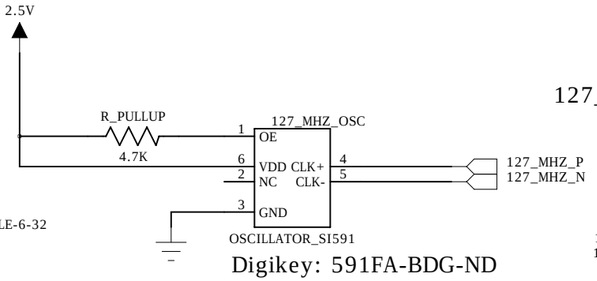
Clock to Carriers 1-2



Clock to Carriers 3-4

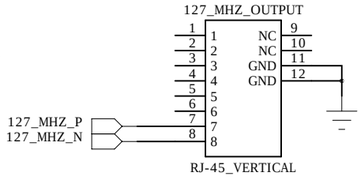






Digikey: 591FA-BDG-ND

127_MHZ_output from oscillator



Institution	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
Title	XRM_CLOCK_FANOUT
Revision	A
IDLAB Design #	IDL_14_024
Circuit Design	JM
PCB Design	JM
Sheet #	1 of 2
Description	Input, Clock Divider, Power
Last Modified	2-October-2014

Clock input

RJ-45_VERTICAL

CLOCK_INPUT

OFFSET_BUF

BUFFER_SN65LVDS108

127MHZ_BUF

BUFFER_SN65LVDS108

RESET_BUF

Digikey: 296-2346-5-ND

BUFFER_SN65LVDS108

BUNCH0_BUF

BUFFER_SN65LVDS108

Institution	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
Title	XRM_CLOCK_FANOUT
Revision	A
IDLAB Design #	IDL_14_024
Circuit Design	JM
PCB Design	JM
Sheet #	2 of 2
Description	Output buffers, output
Last Modified	2-October-2014