5mil trace; outer layer trace spacing=5; inner layer spacing=8
dielectric layer thickness: 5 mil(microstrip) and 9 mil(stripline)
will work for both symmetry and asymmetry layer stackup.

JUMPERS

A - Enalbe/disable local 127MHz clock

B - LVDS clock fanout
installed: will fanout only remote RCLK clock.
removed: fanout both RCLK and local clock

C - installed: shutdown 2.5V and 1.2V VRs

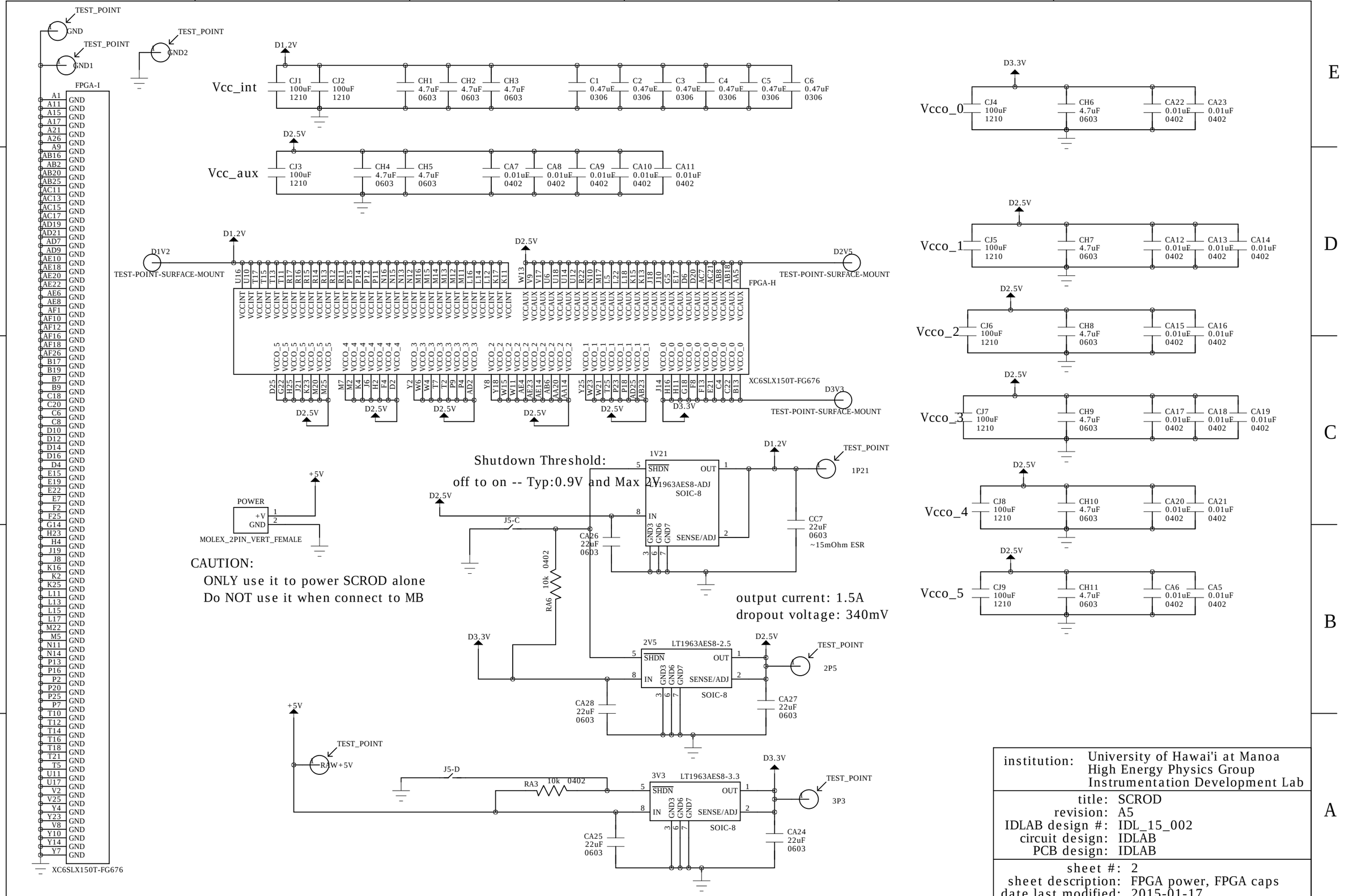
D - installed: shutdown 3.3V VR

2015-01-20
fixed RJ45 pinout error for remote JTAG.

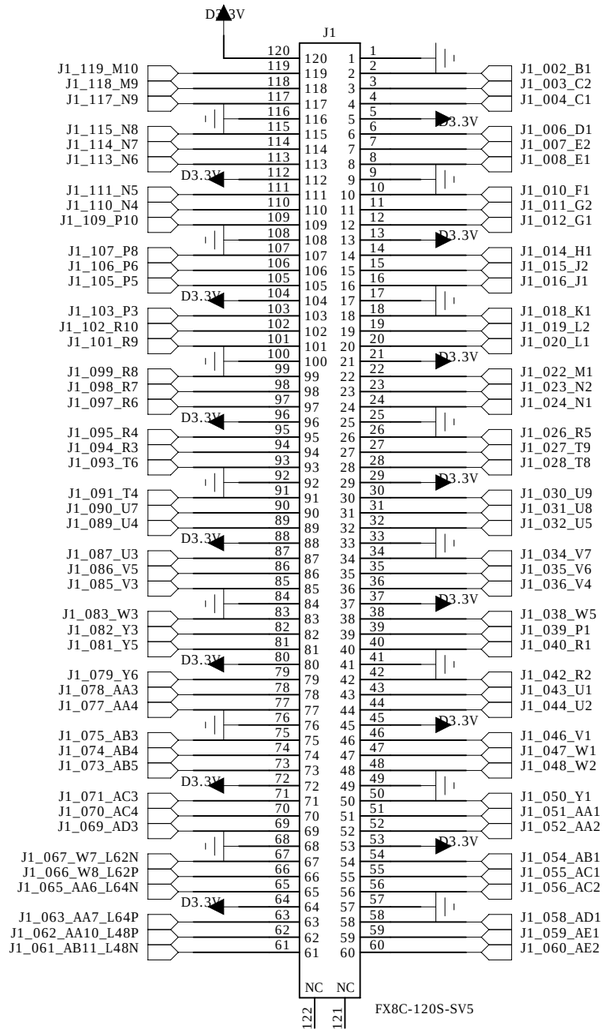
2013-10-09
pcb: changed 2 pin molex connector to use bigger holes

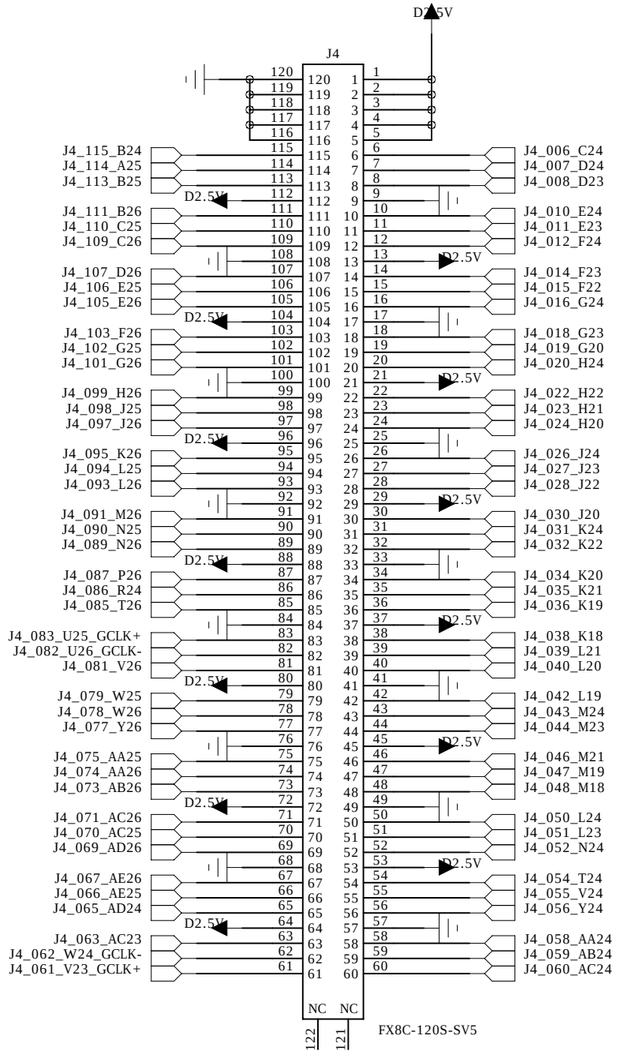
2013-10-10
sch: changed thermal wall holes to be the skinny type

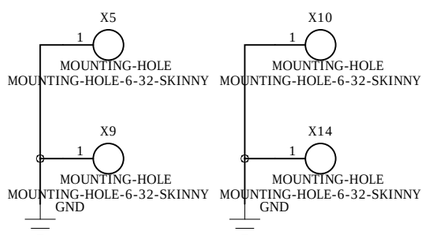
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A5
IDLAB design #:	IDL_15_002
circuit design:	IDLAB
PCB design:	IDLAB
sheet #:	1
sheet description:	block diagram
date last modified:	2015-01-17



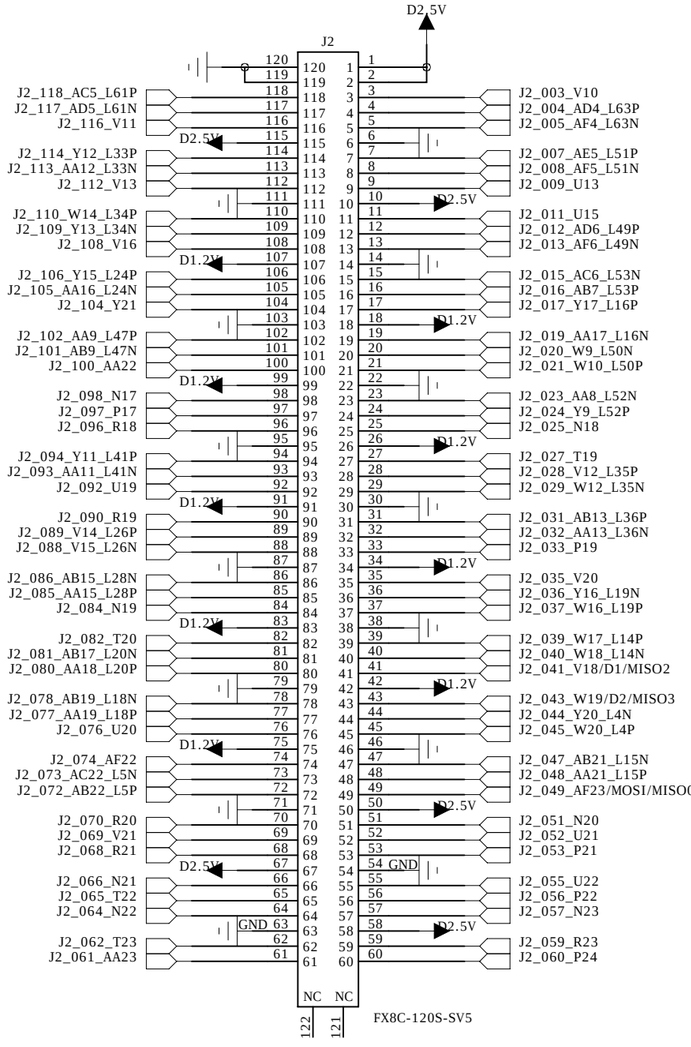
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A5
IDLAB design #:	IDL_15_002
circuit design:	IDLAB
PCB design:	IDLAB
sheet #:	2
sheet description:	FPGA power, FPGA caps
date last modified:	2015-01-17

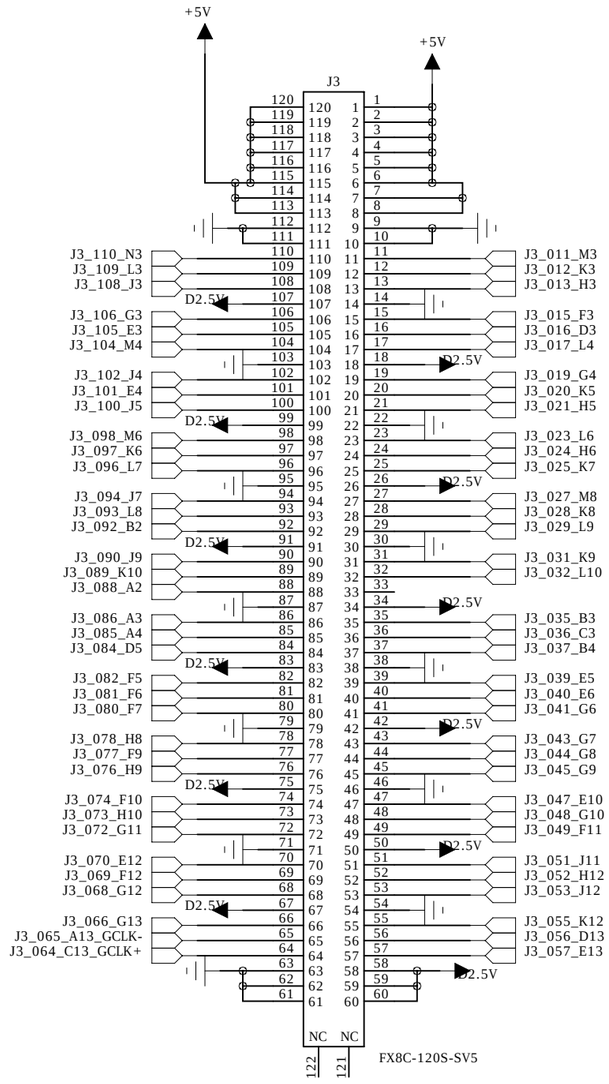




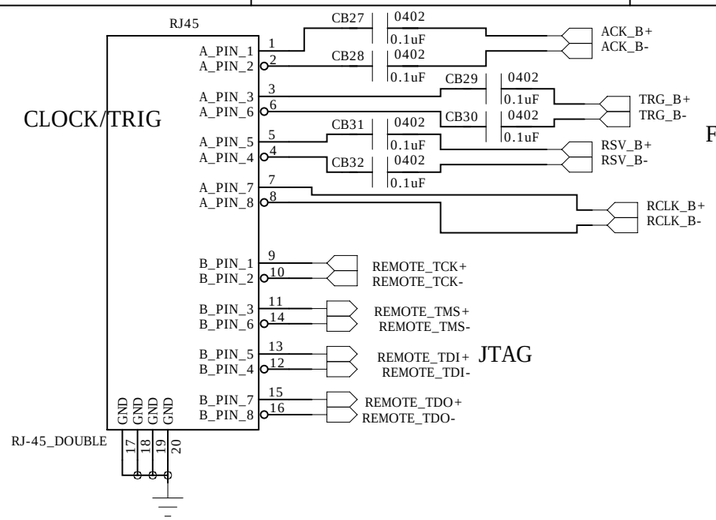


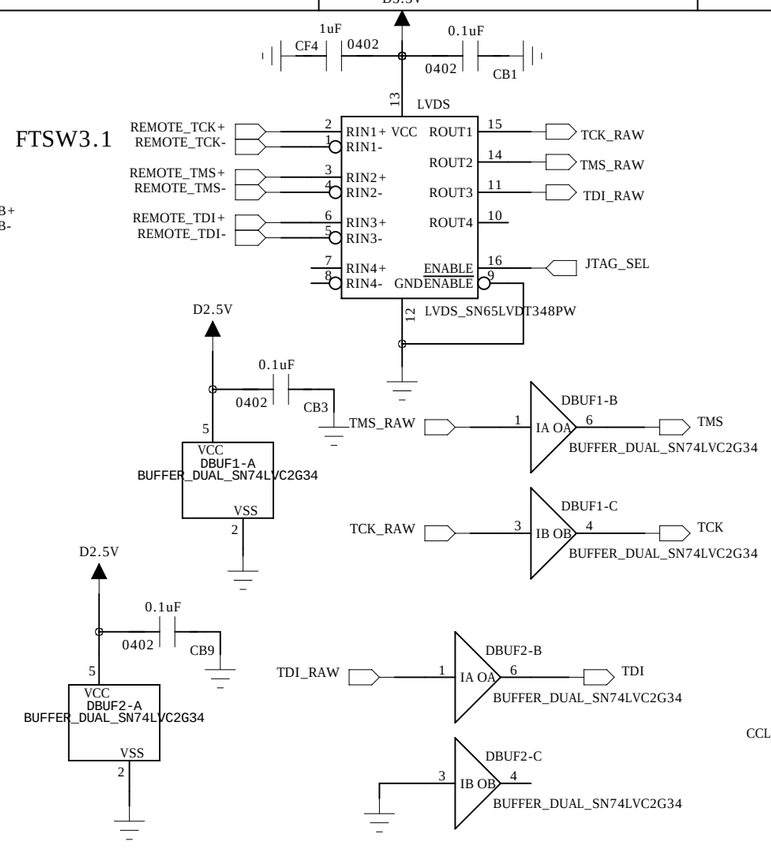
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A5
IDLAB design #:	IDL_15_002
circuit design:	IDLAB
PCB design:	IDLAB
sheet #:	3
sheet description:	board-to-board interconnects
date last modified:	2015-01-17

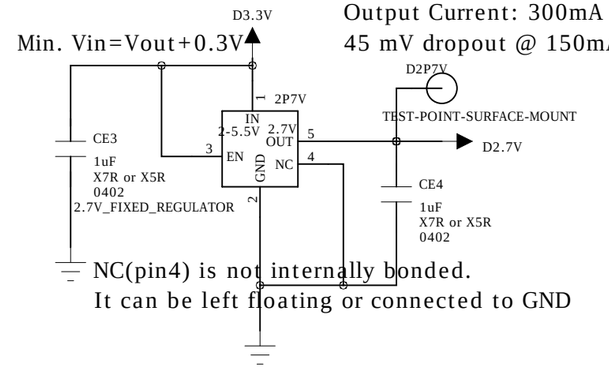




institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A5
IDLAB design #:	IDL_15_002
circuit design:	IDLAB
PCB design:	IDLAB
sheet #:	4
sheet description:	board-to-board interconnects
date last modified:	2015-01-17

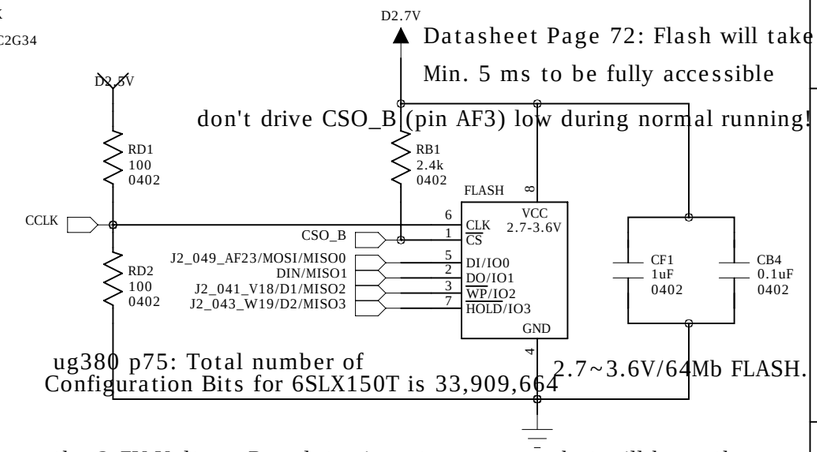




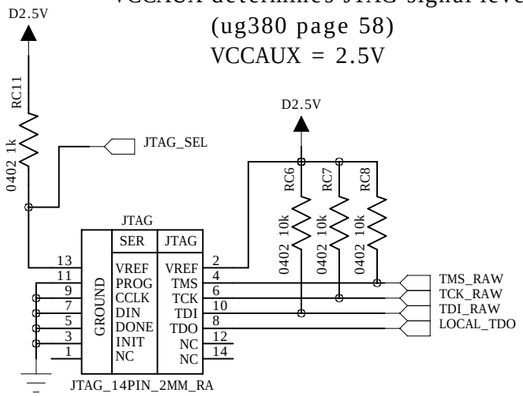


Min. Input High Voltage:2.7V * 0.7 = 1.89V

change D3.3V TO D2.7V Max. Current Chip Erase: 25 mA

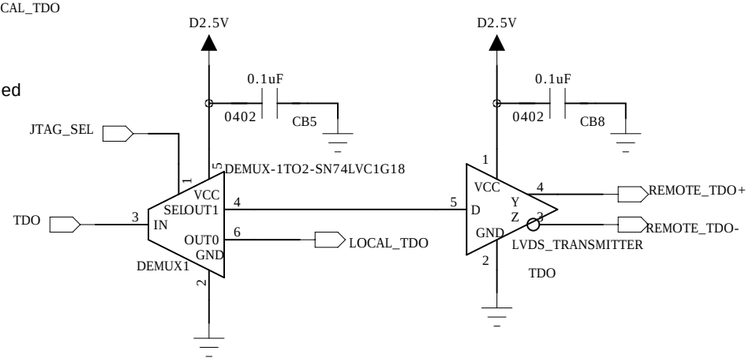


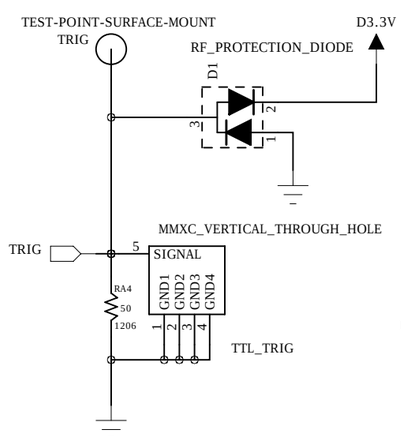
the 2.7V Voltage Regulator is not necessary, but will keep them anyway.

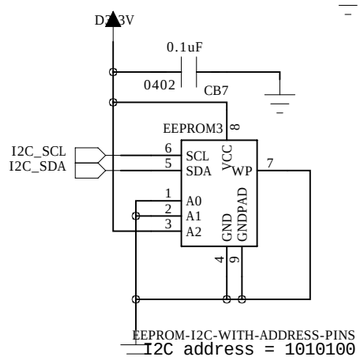


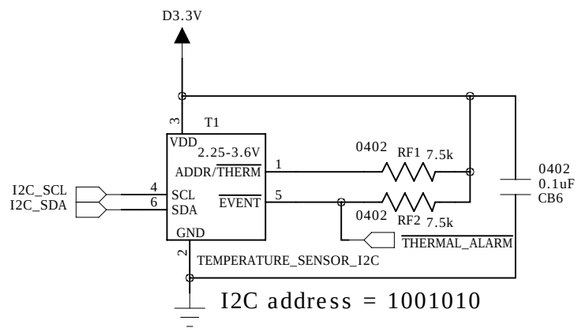
VCCAUX determines JTAG signal level
(ug380 page 58)
VCCAUX = 2.5V

JTAG_SEL must be LVDS when 14 pin header not connected
ds593 page 16 suggests this hookup
copy from SCROD RevB
automatically select between local and remote JTAG

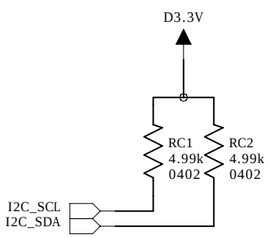




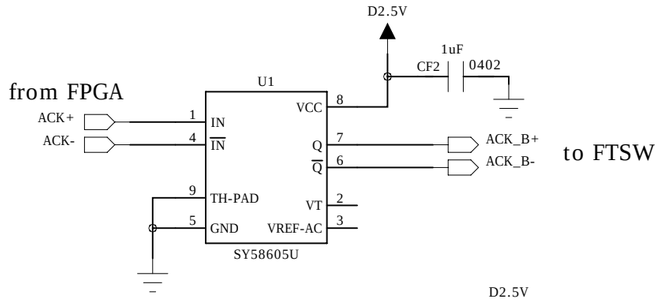




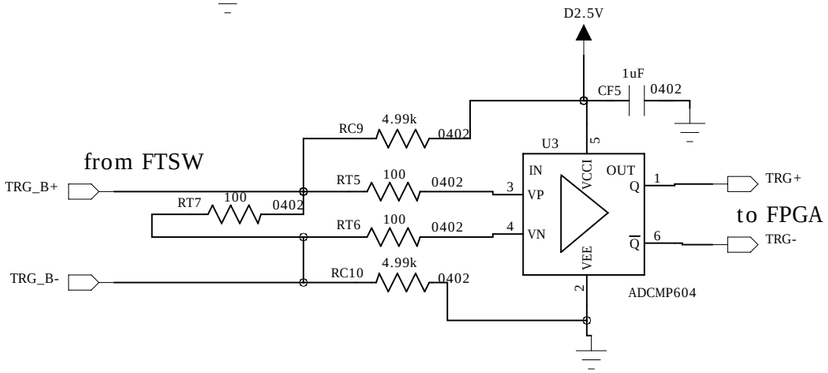
I2C address = 1001010



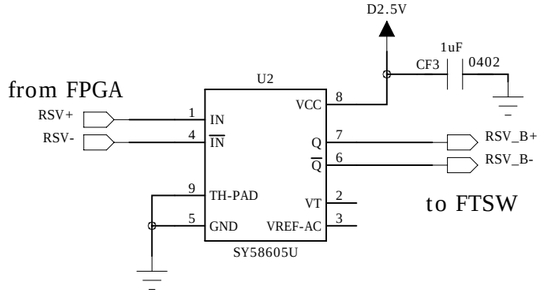
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A5
IDLAB design #:	IDL_15_002
circuit design:	IDLAB
PCB design:	IDLAB
sheet #:	5
sheet description:	JTAG, CLOCK, LEDs, PROM
date last modified:	2015-01-17



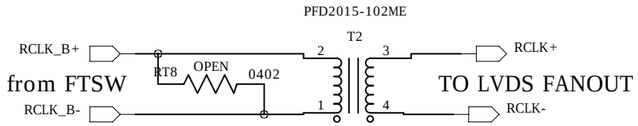
to FTSW

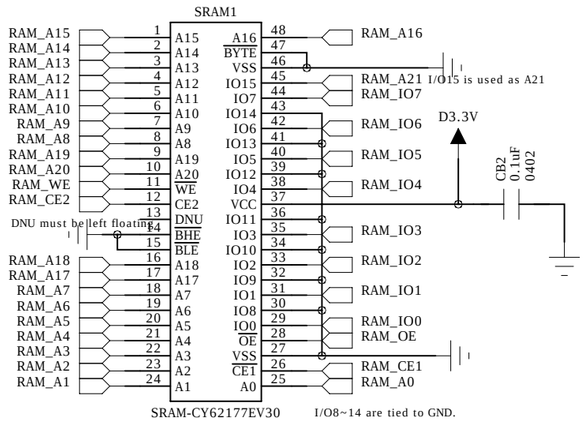


to FPGA

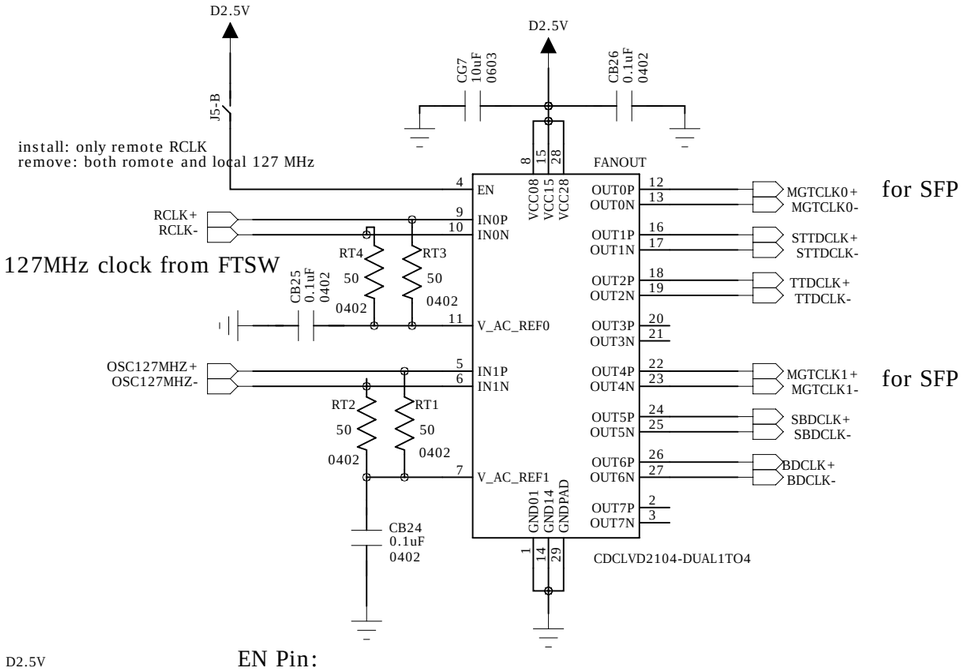


to FTSW





RAM uses 34 FPGA I/O Pins(3.3V bank).

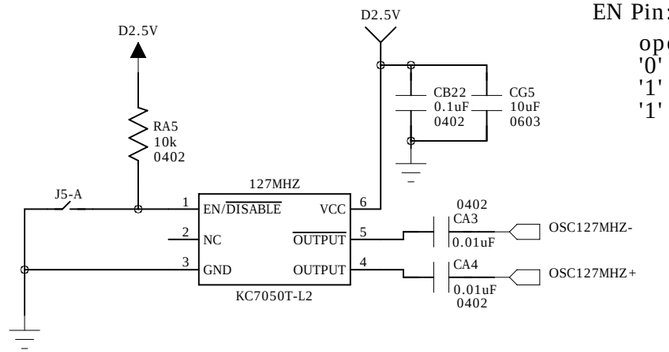


for SFP

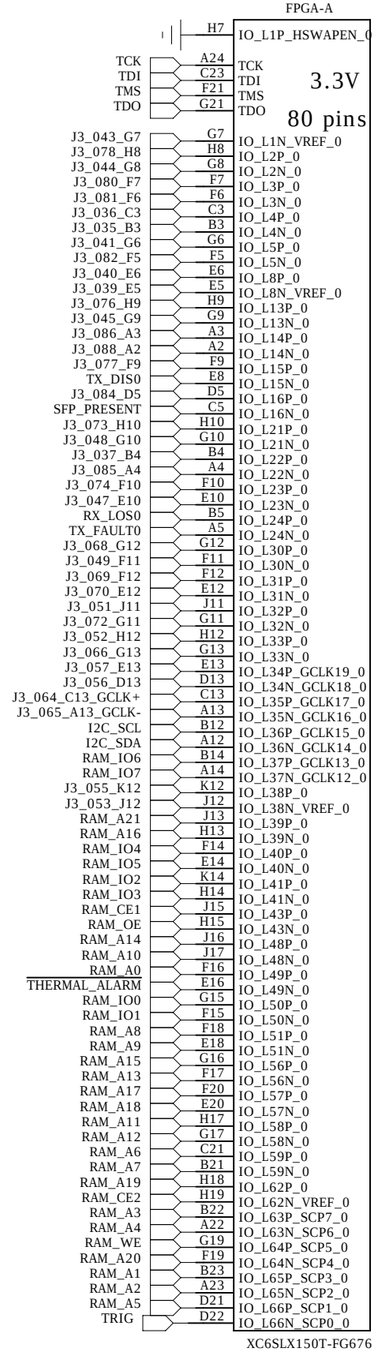
for SFP

EN Pin:

open -> two buffers with all outputs are enabled.
'0' -> two buffers with all outputs are disabled.
'1' -> one buffers enabled and one disabled.
'1' -> OUT0, OUT3 enabled and OUT4, OUT7 disabled

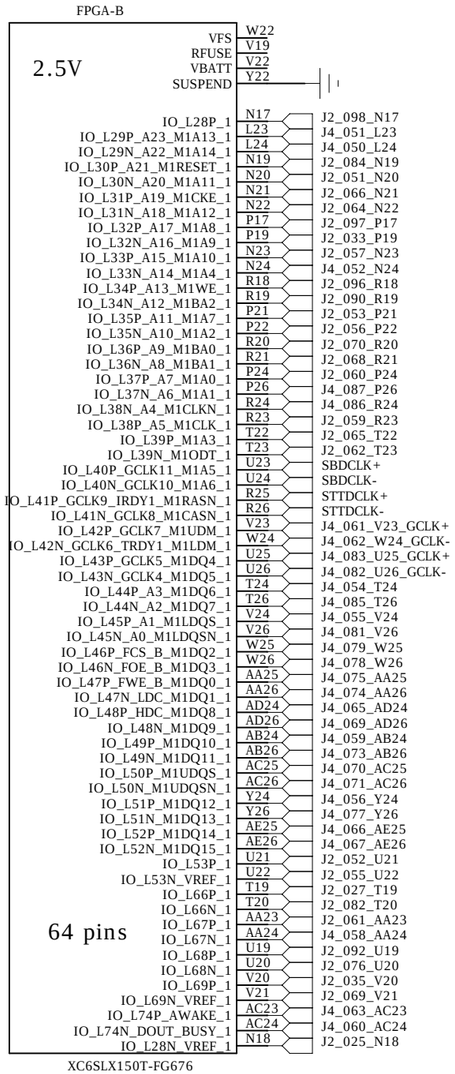


institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A5
IDLAB design #:	IDL_15_002
circuit design:	IDLAB
PCB design:	IDLAB
sheet #:	6
sheet description:	block diagram
date last modified:	2015-01-17

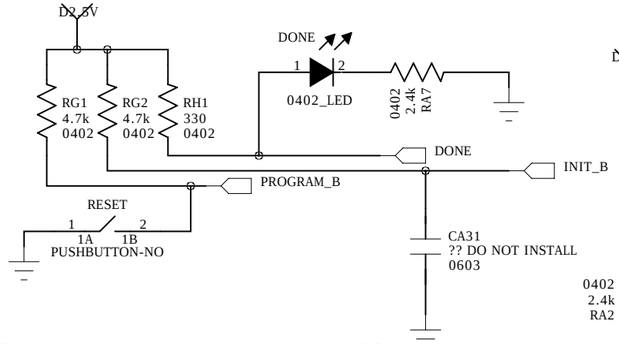


added bank pin counts

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A5
IDLAB design #:	IDL_15_002
circuit design:	IDLAB
PCB design:	IDLAB
sheet #:	7
sheet description:	FPGA banks 0-5
date last modified:	2015-01-17

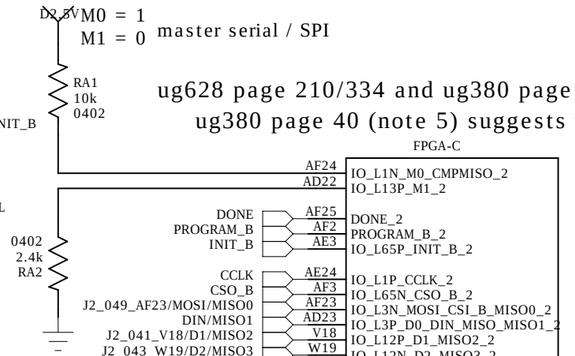


institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A5
IDLAB design #:	IDL_15_002
circuit design:	IDLAB
PCB design:	IDLAB
sheet #:	8
sheet description:	FPGA banks 0-5
date last modified:	2015-01-17

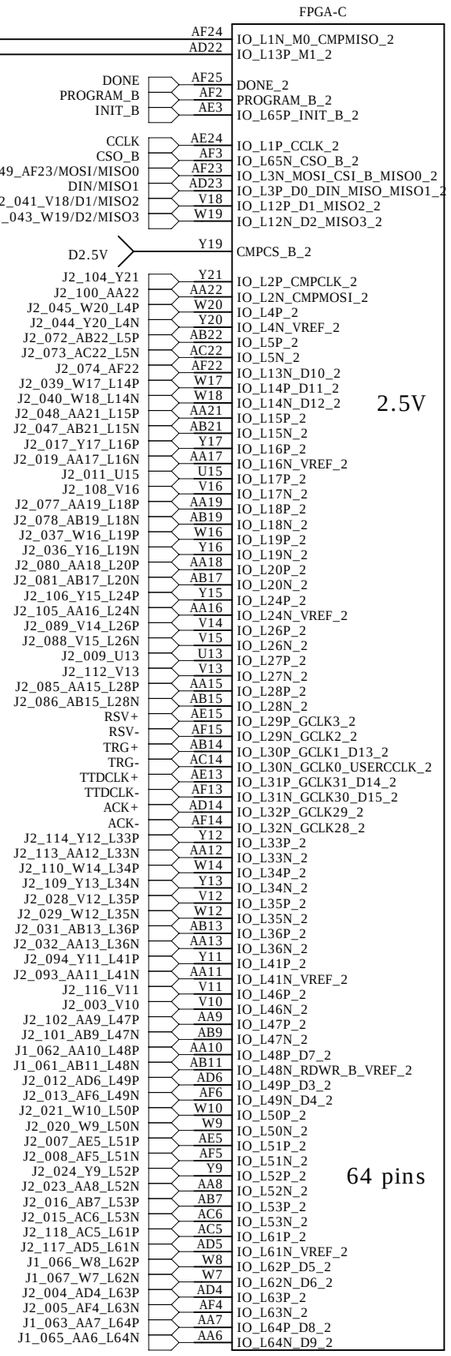


datasheet ug380 says on page 41, Table 2-6

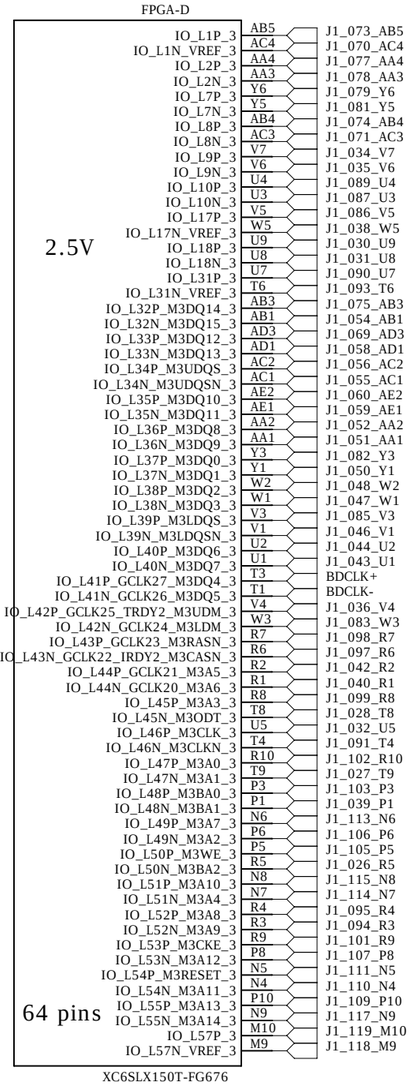
Tests show that the SPI Flash(W25Q64FVSSIG) works



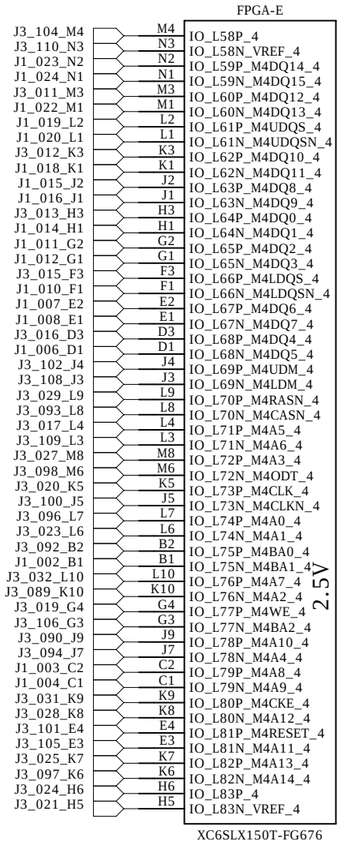
ug628 page 210/334 and ug380 page 42/66 says we don't need a pullup on done, program_b nor init_b
ug380 page 40 (note 5) suggests we need a 2.5V Vcc on the SPI flash



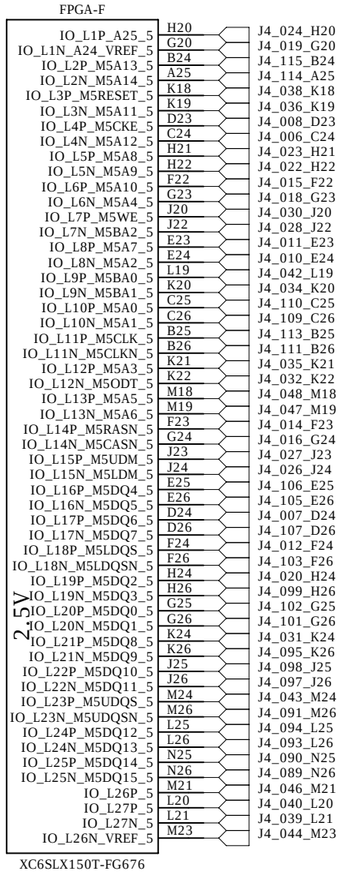
institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A5
IDLAB design #:	IDL_15_002
circuit design:	IDLAB
PCB design:	IDLAB
sheet #:	9
sheet description:	FPGA banks 0-5
date last modified:	2015-01-17



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A5
IDLAB design #:	IDL_15_002
circuit design:	IDLAB
PCB design:	IDLAB
sheet #:	10
sheet description:	FPGA banks 0-5
date last modified:	2015-01-17

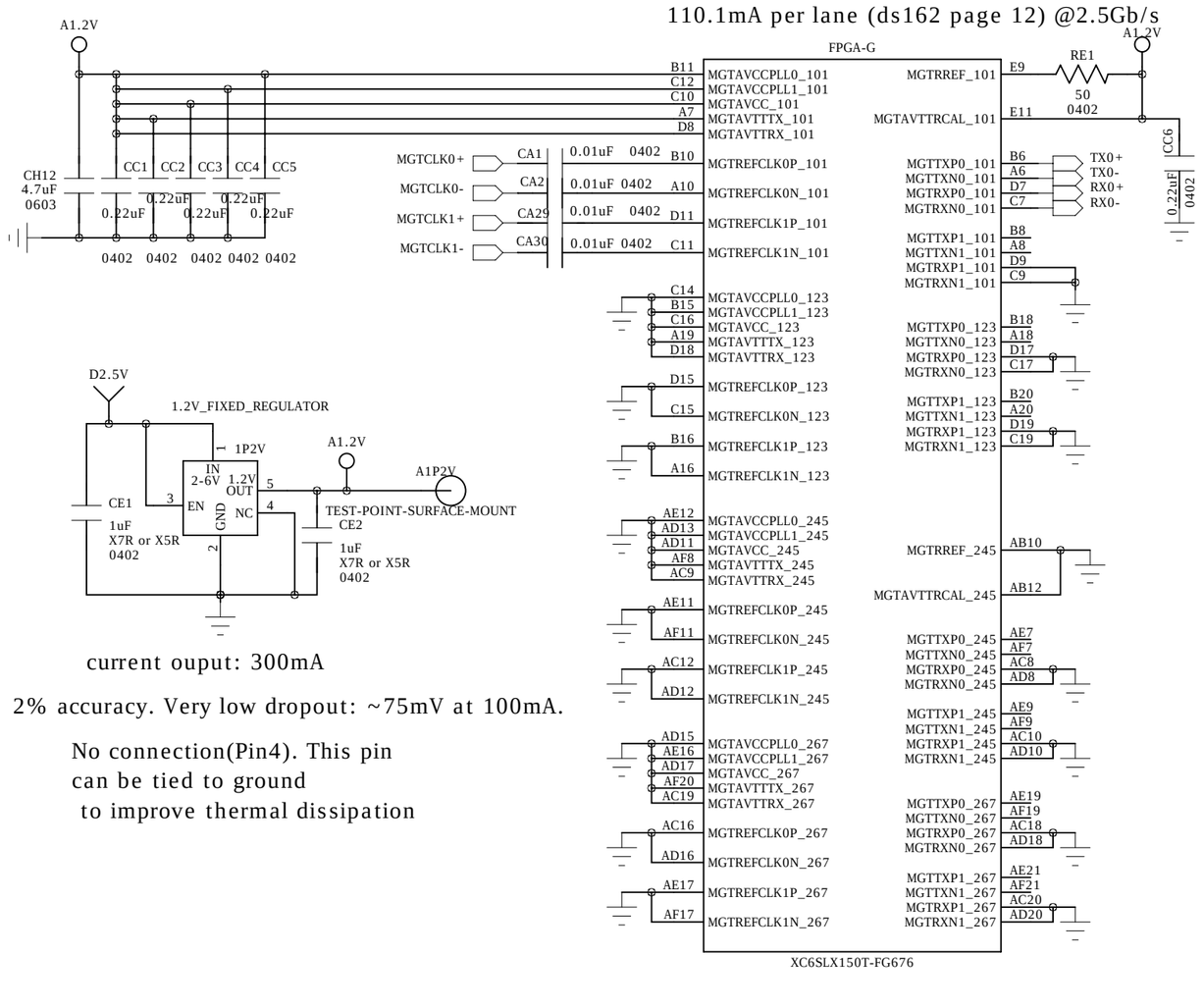


institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A5
IDLAB design #:	IDL_15_002
circuit design:	IDLAB
PCB design:	IDLAB
sheet #:	11
sheet description:	FPGA banks 0-5
date last modified:	2015-01-17



50 pins

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A5
IDLAB design #:	IDL_15_002
circuit design:	IDLAB
PCB design:	IDLAB
sheet #:	12
sheet description:	FPGA banks 0-5
date last modified:	2015-01-17



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	SCROD
revision:	A5
IDLAB design #:	IDL_15_002
circuit design:	IDLAB
PCB design:	IDLAB
sheet #:	13
sheet description:	fiber transceiver, fiber clock
date last modified:	2015-01-17