

6

5

4

3

2

1

E

5mil trace; outer layer trace spacing=5; inner layer spacing=8
dielectric layer thickness: 5 mil(microstrip) and 9 mil(stripline)
will work for both symmetry and asymmetry layer stackup.

E

JUMPERS

A - Enable/disable local 127MHz clock

B - LVDS clock fanout
installed: will fanout only remote RCLK clock.
removed: fanout both RCLK and local clock

C - installed: shutdown 2.5V and 1.2V VRs

D - installed: shutdown 3.3V VR

D

D

2015-01-20
fixed RJ45 pinout error for remote JTAG.

2013-10-09
pcb: changed 2 pin molex connector to use bigger holes

2013-10-10
sch: changed thermal wall holes to be the skinny type

C

C

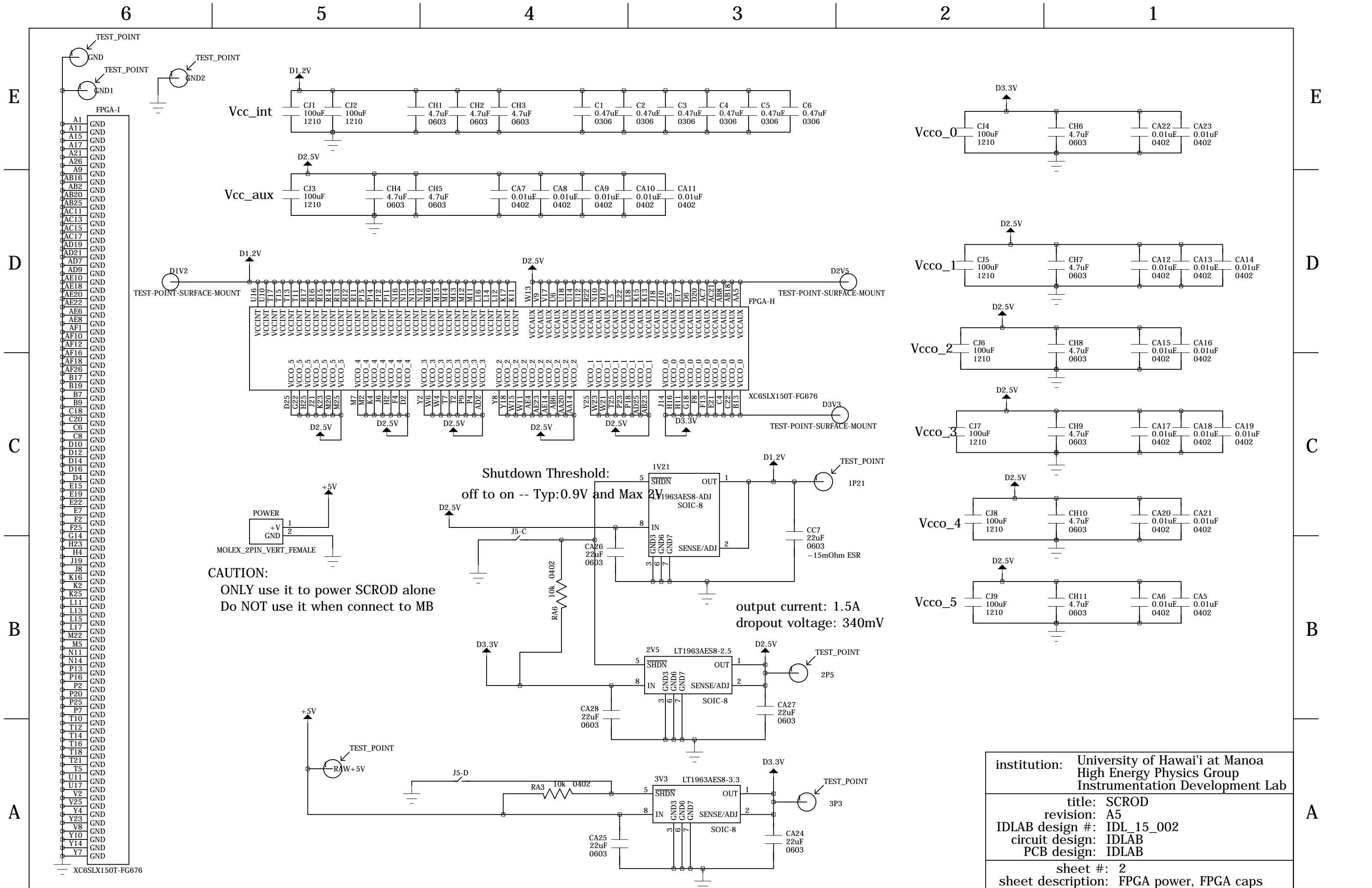
B

B

A

A

| | |
|---------------------|--|
| institution: | University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab |
| title: | SCROD |
| revision: | A5 |
| IDLAB design #: | IDL_15_002 |
| circuit design: | IDLAB |
| PCB design: | IDLAB |
| sheet #: | 1 |
| sheet description: | block diagram |
| date last modified: | 2015-01-17 |



E
D
C
B
A

E
D
C
B
A

CAUTION:
ONLY use it to power SCROD alone
Do NOT use it when connect to MB

| | |
|---------------------|--|
| institution: | University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab |
| title: | SCROD |
| revision: | A5 |
| IDLAB design #: | IDL_15_002 |
| circuit design: | IDLAB |
| PCB design: | IDLAB |
| sheet #: | 2 |
| sheet description: | FPGA power, FPGA caps |
| date last modified: | 2015-01-17 |

E

E

D

D

C

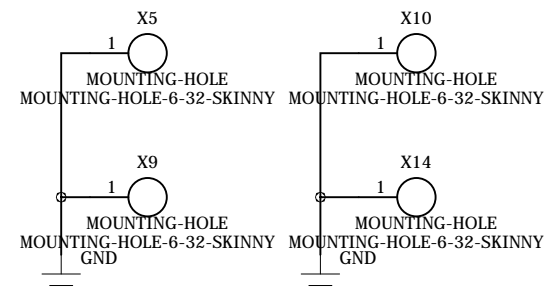
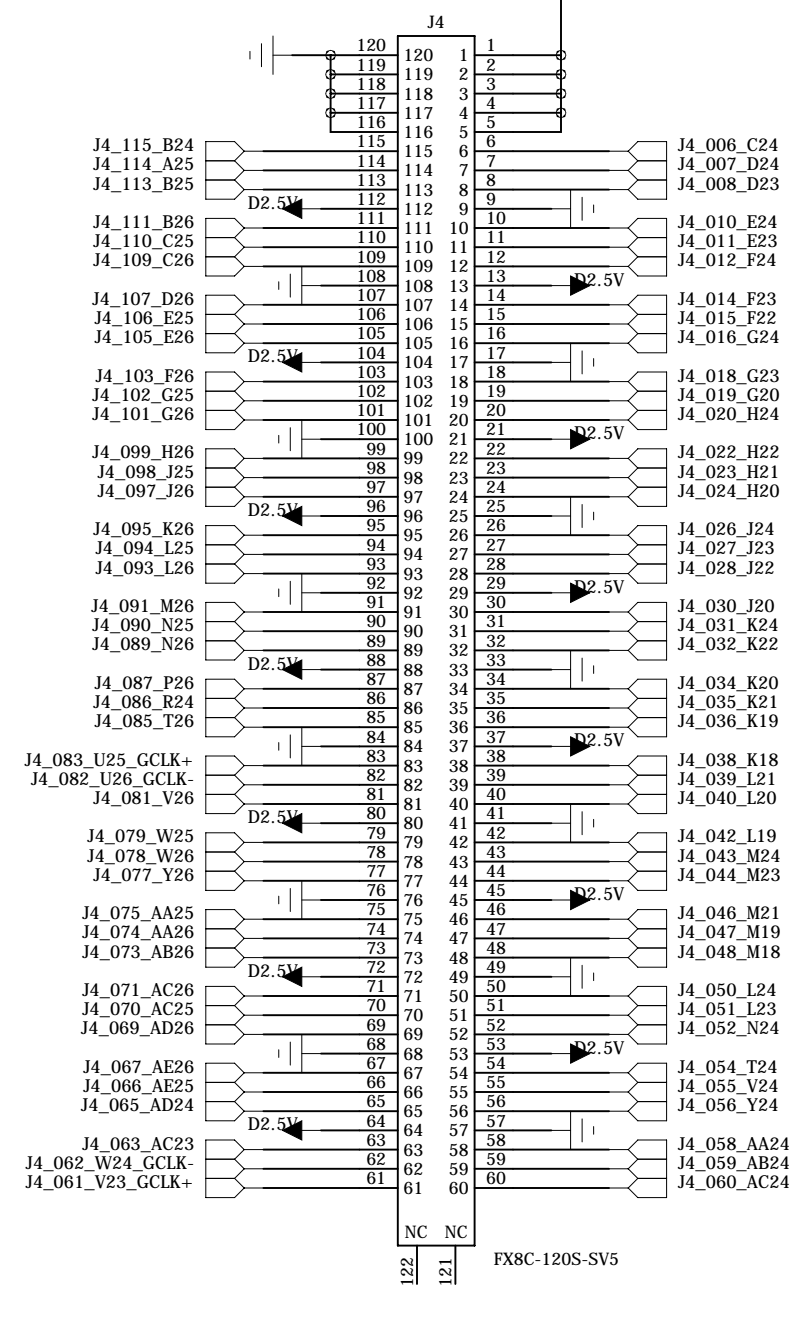
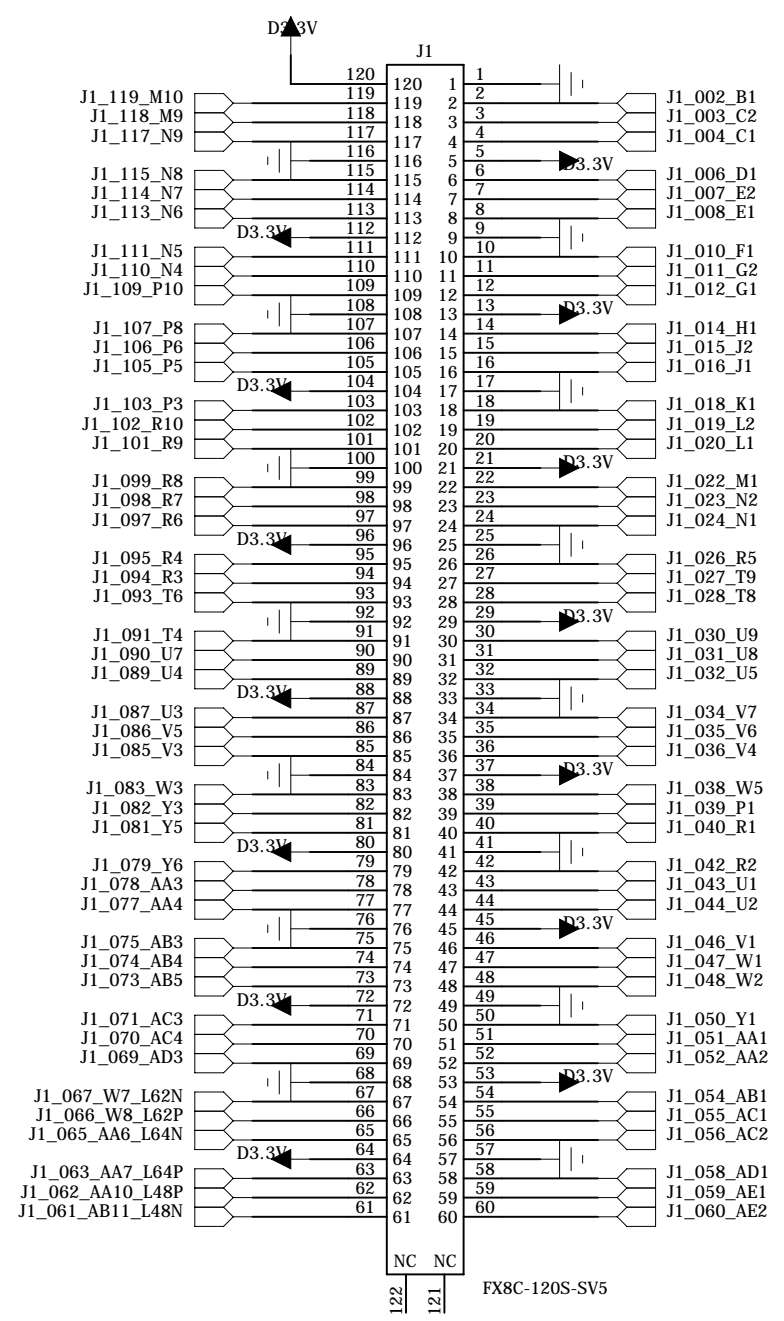
C

B

B

A

A



| | |
|---------------------|--|
| institution: | University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab |
| title: | SCROD |
| revision: | A5 |
| IDLAB design #: | IDL_15_002 |
| circuit design: | IDLAB |
| PCB design: | IDLAB |
| sheet #: | 3 |
| sheet description: | board-to-board interconnects |
| date last modified: | 2015-01-17 |

6

5

4

3

2

1

E

E

D

D

C

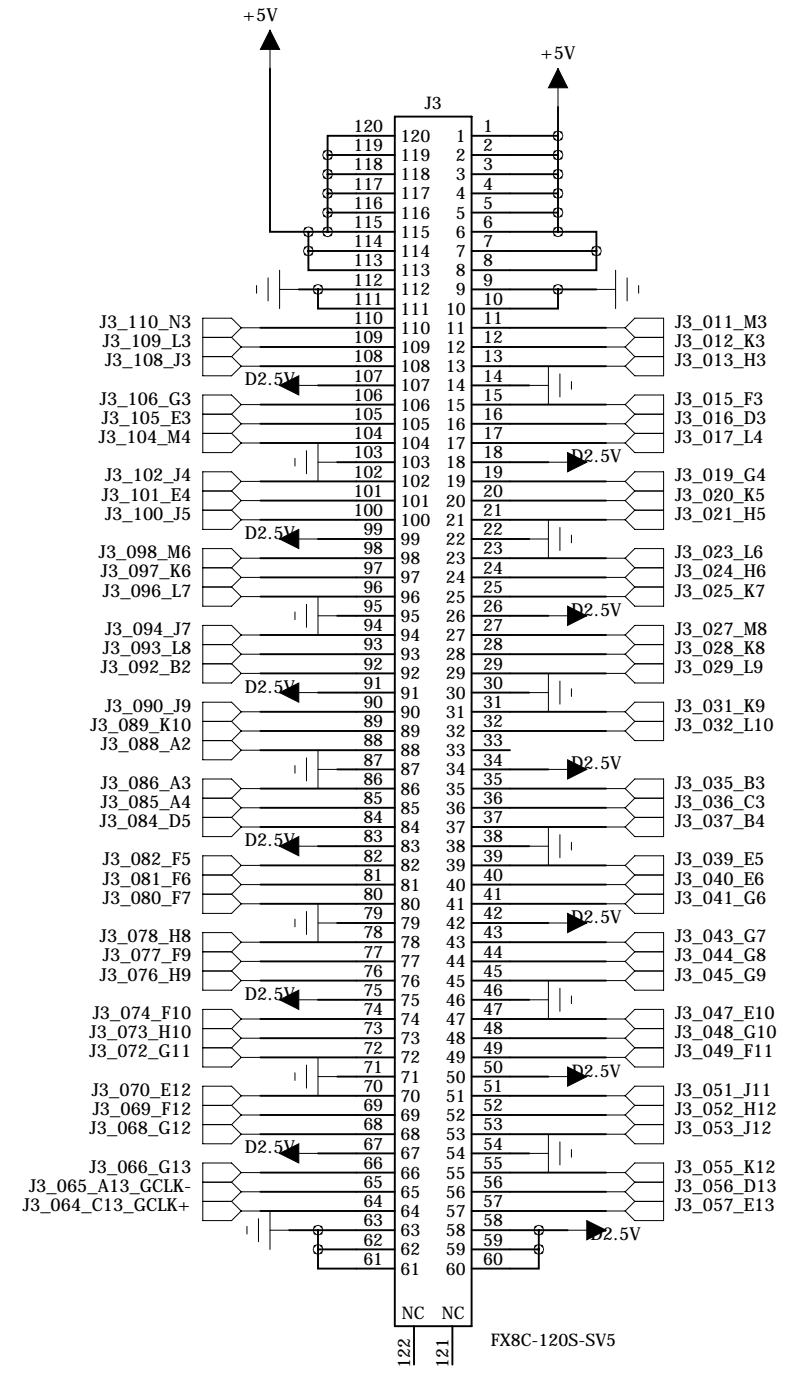
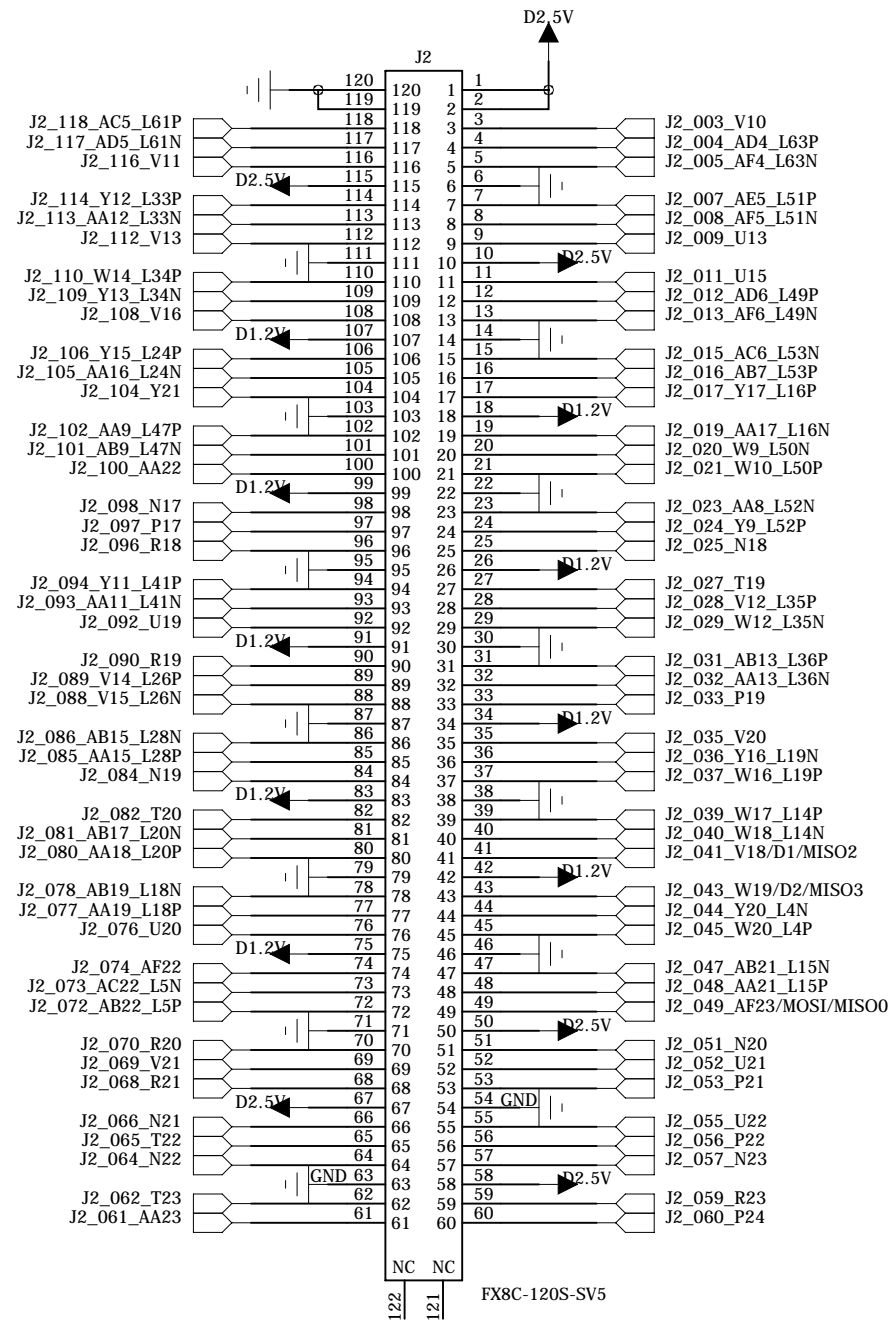
C

B

B

A

A

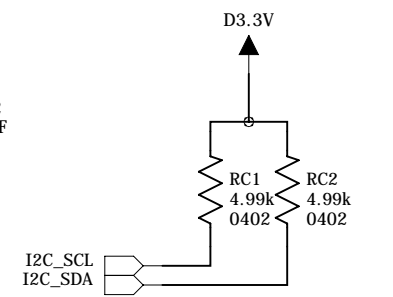
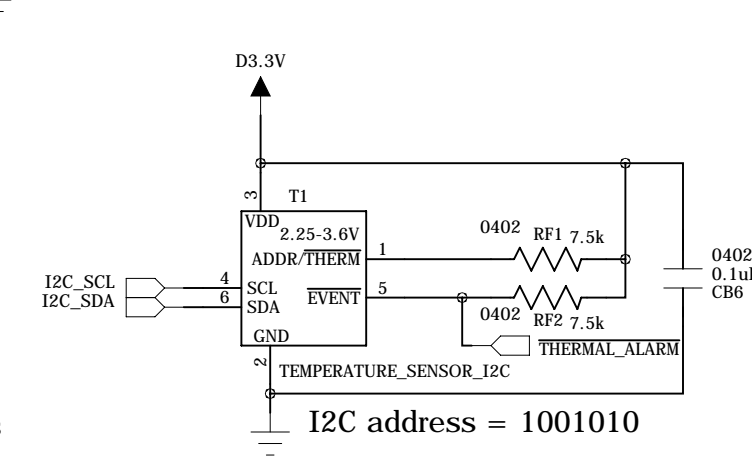
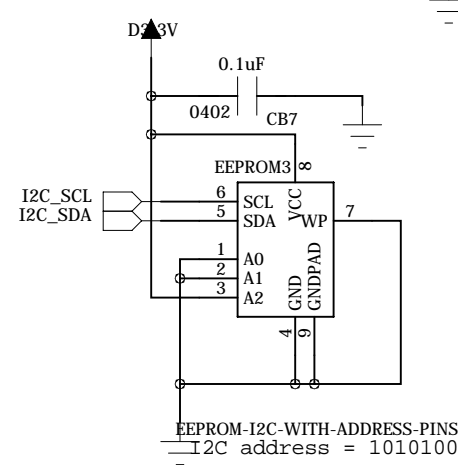
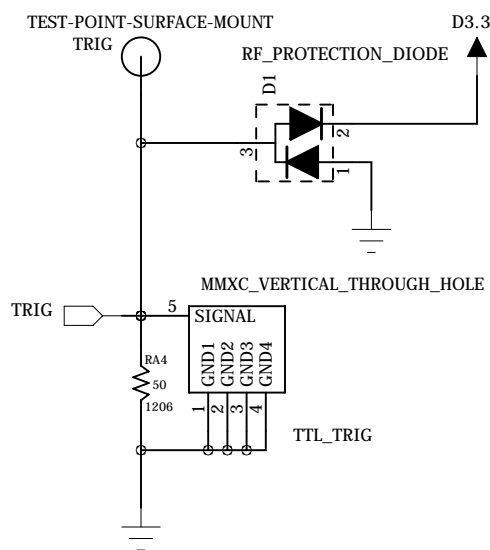


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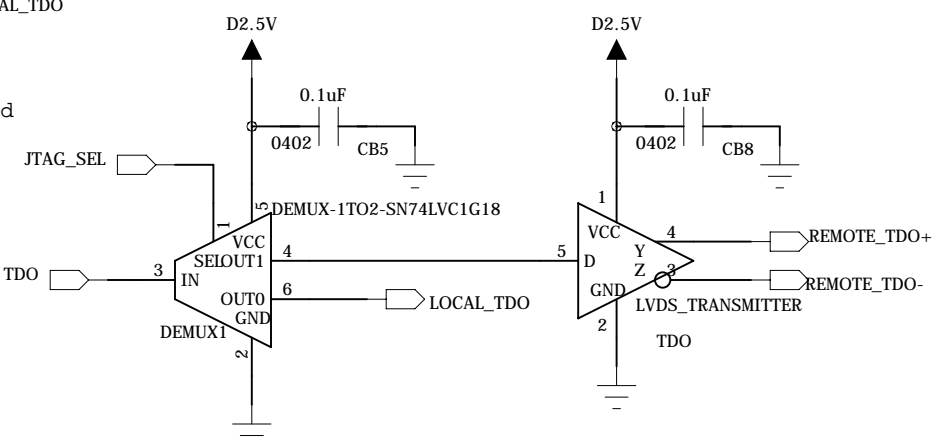
title: SCROD
 revision: A5
 IDLAB design #: IDL_15_002
 circuit design: IDLAB
 PCB design: IDLAB

sheet #: 4
 sheet description: board-to-board interconnects
 date last modified: 2015-01-17

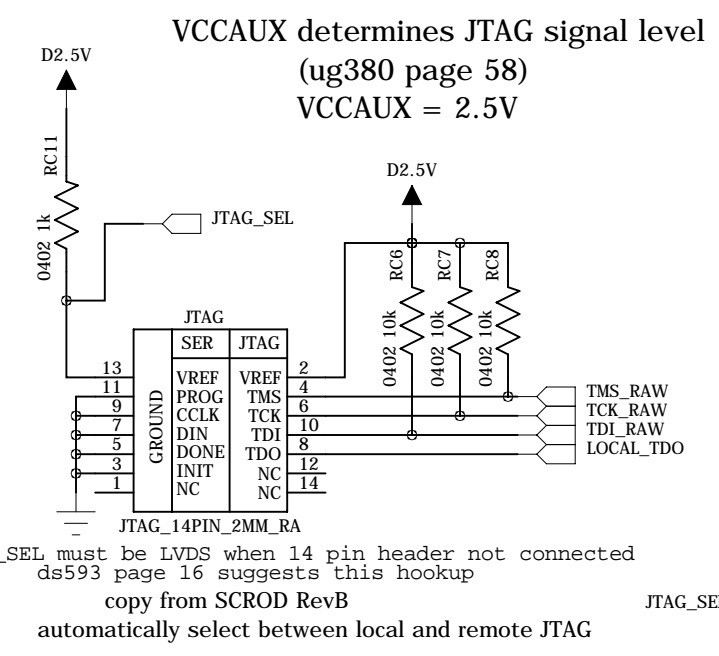
A



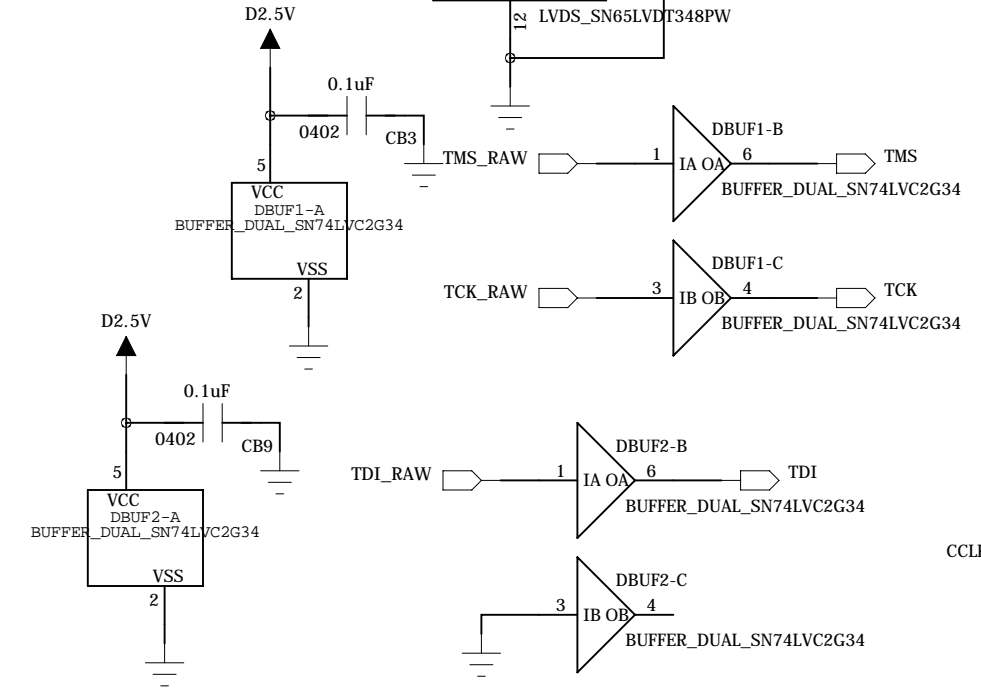
B



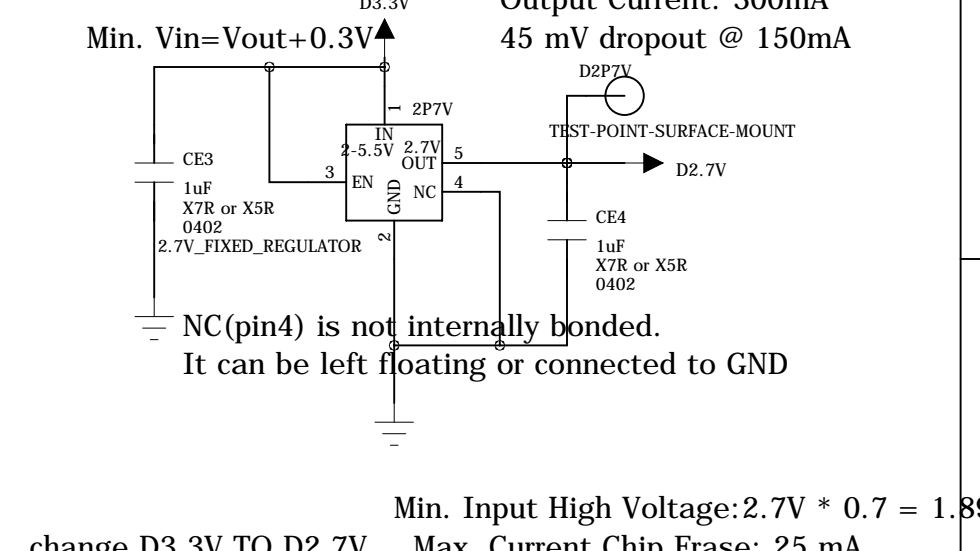
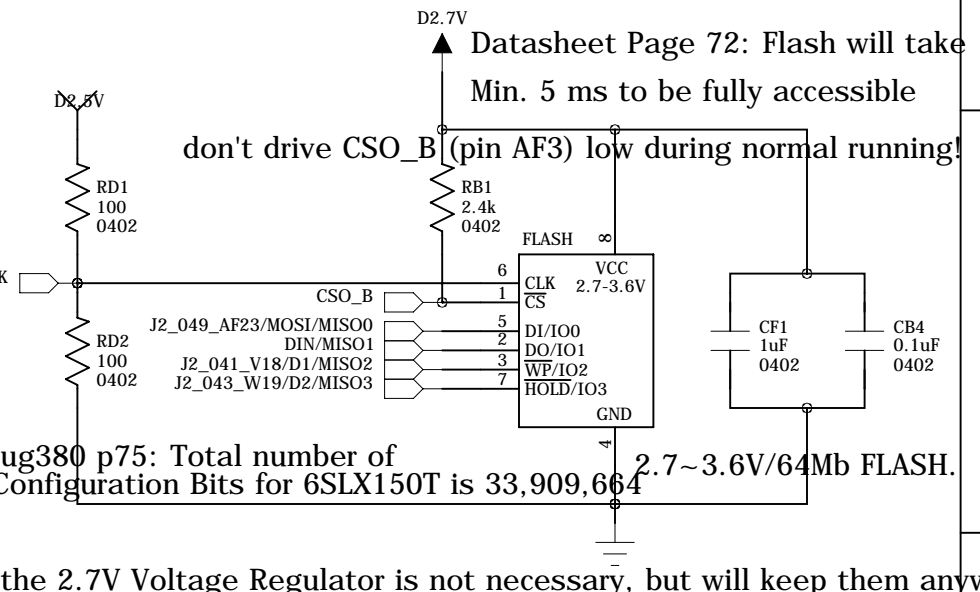
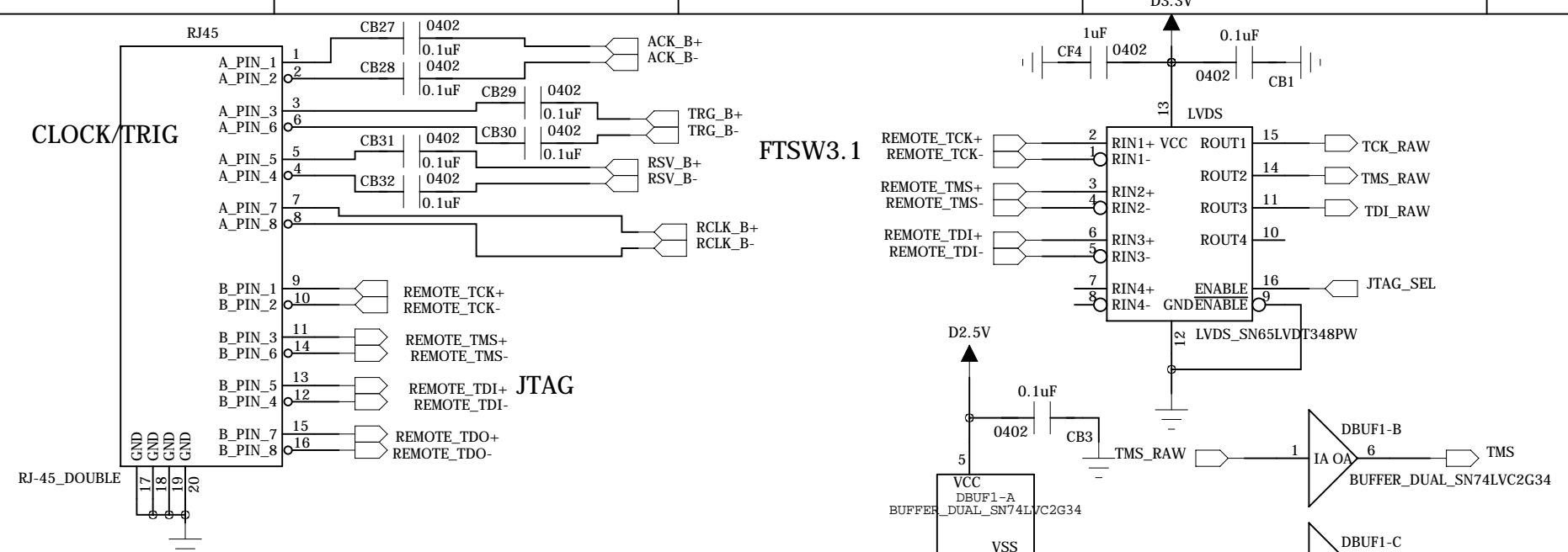
C



D



E



ug380 p75: Total number of Configuration Bits for 6SLX150T is 33,909,664

2.7~3.6V/64Mb FLASH.

don't drive CSO_B (pin AF3) low during normal running!

change D3.3V TO D2.7V

Min. Input High Voltage: 2.7V * 0.7 = 1.89V

Max. Current Chip Erase: 25 mA

Datasheet Page 72: Flash will take Min. 5 ms to be fully accessible

Output Current: 300mA

45 mV dropout @ 150mA

Min. Vin = Vout + 0.3V

NC (pin4) is not internally bonded. It can be left floating or connected to GND

the 2.7V Voltage Regulator is not necessary, but will keep them anyway.

| | |
|---------------------|--|
| institution: | University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab |
| title: | SCROD |
| revision: | A5 |
| IDLAB design #: | IDL_15_002 |
| circuit design: | IDLAB |
| PCB design: | IDLAB |
| sheet #: | 5 |
| sheet description: | JTAG, CLOCK, LEDs, PROM |
| date last modified: | 2015-01-17 |

A

B

C

D

E

E

E

D

D

C

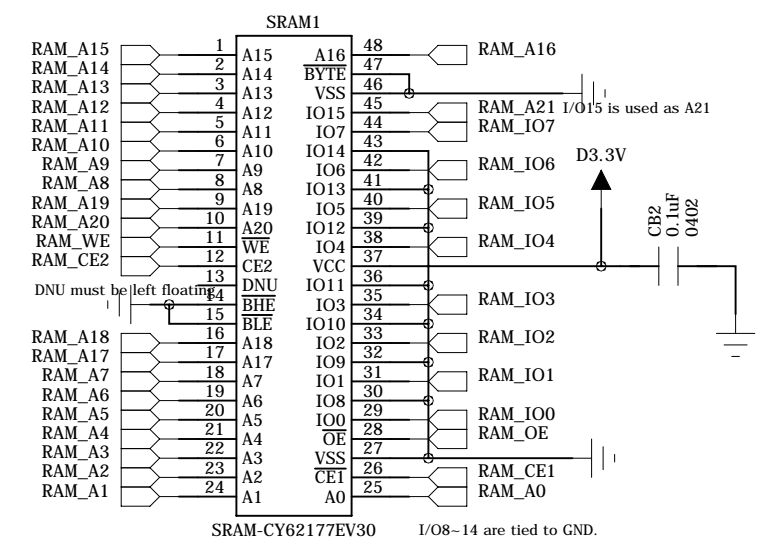
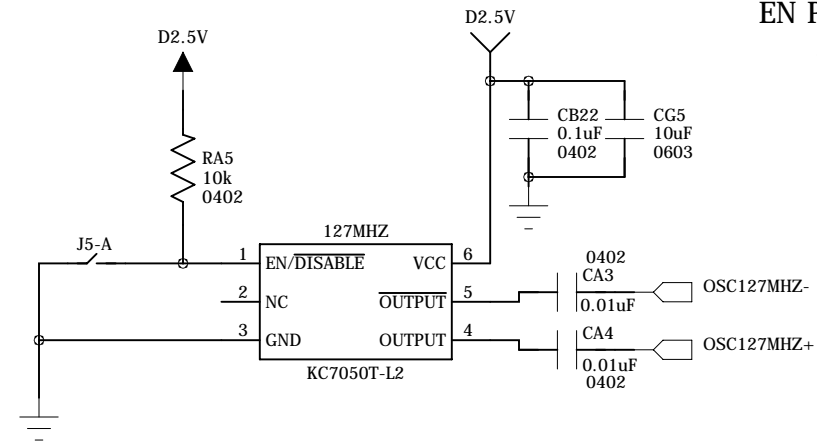
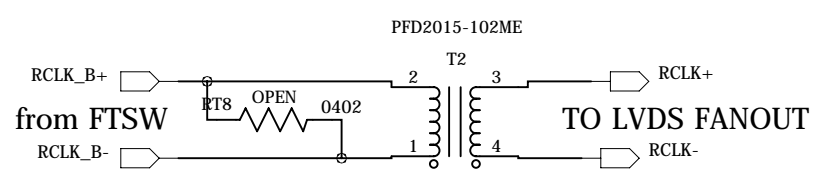
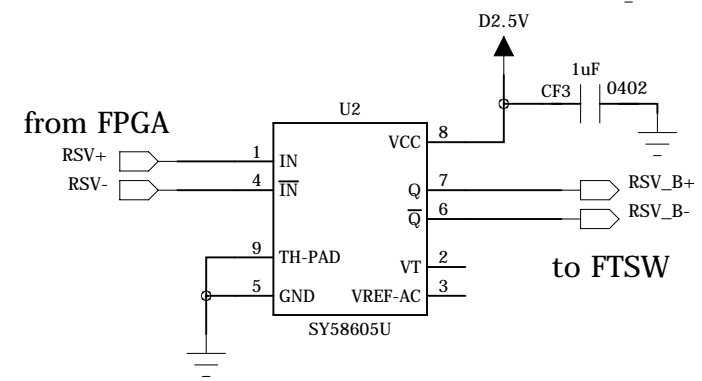
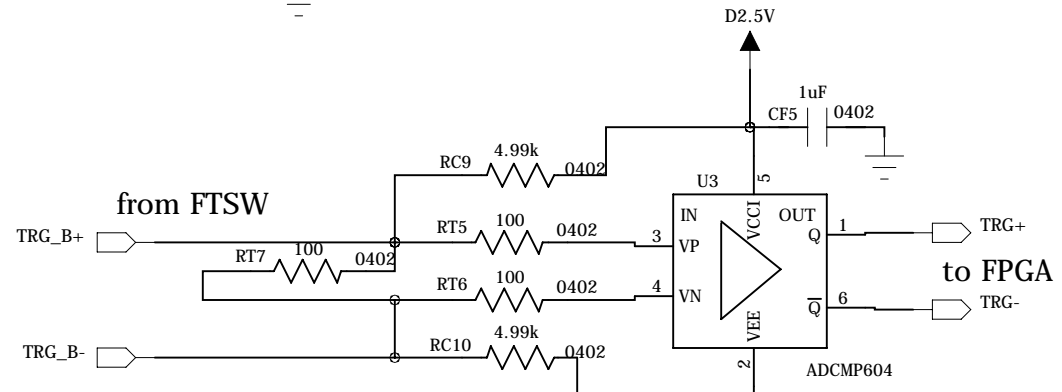
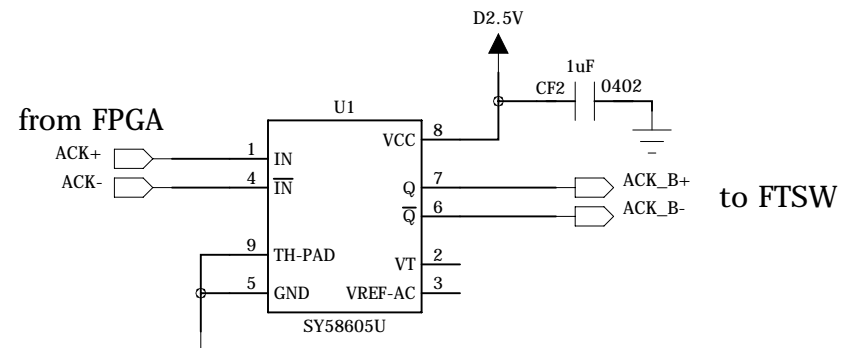
C

B

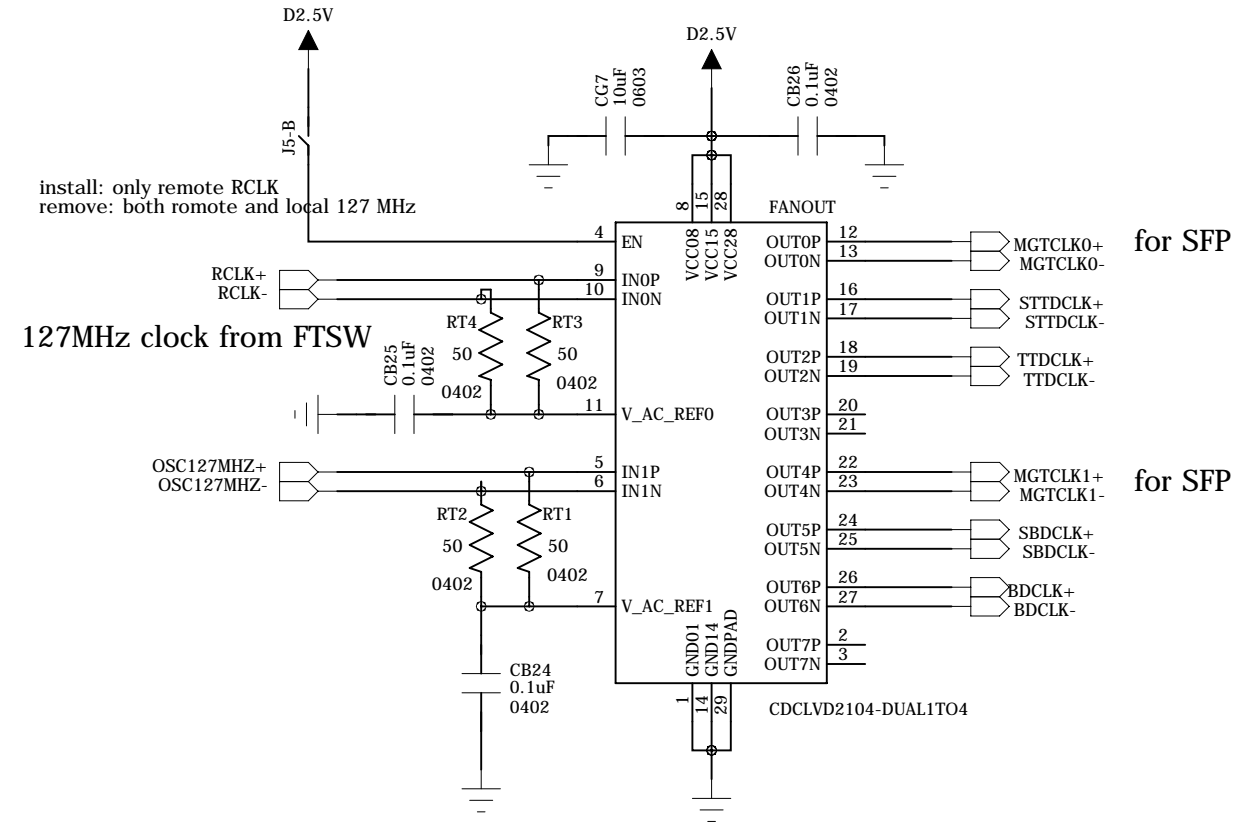
B

A

A



RAM uses 34 FPGA I/O Pins (3.3V bank).



EN Pin:
 open -> two buffers with all outputs are enabled.
 '0' -> two buffers with all outputs are disabled.
 '1' -> one buffers enabled and one disabled.
 '1' -> OUT0, OUT3 enabled and OUT4, OUT7 disabled

institution: University of Hawai'i at Manoa
 High Energy Physics Group
 Instrumentation Development Lab
 title: SCROD
 revision: A5
 IDLAB design #: IDL_15_002
 circuit design: IDLAB
 PCB design: IDLAB

sheet #: 6
 sheet description: block diagram
 date last modified: 2015-01-17

E

D

C

B

A

E

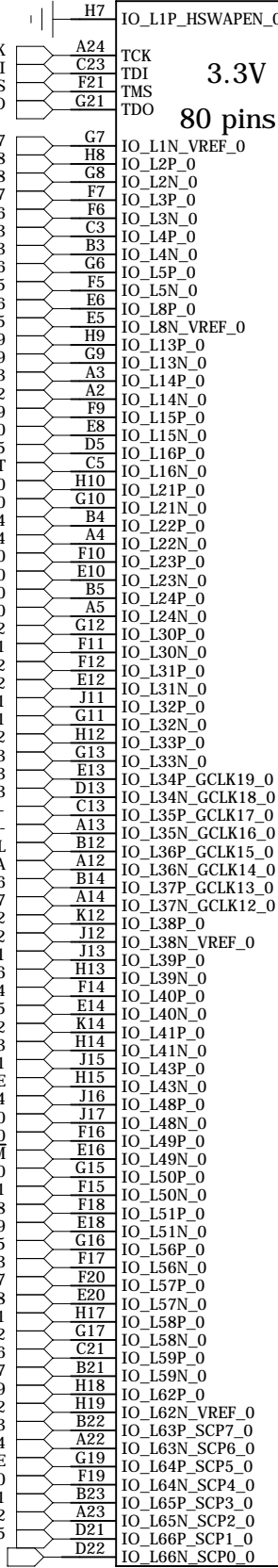
D

C

B

A

FPGA-A



XC6SLX150T-FG676

added bank pin counts

| | |
|---------------------|--|
| institution: | University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab |
| title: | SCROD |
| revision: | A5 |
| IDLAB design #: | IDL_15_002 |
| circuit design: | IDLAB |
| PCB design: | IDLAB |
| sheet #: | 7 |
| sheet description: | FPGA banks 0-5 |
| date last modified: | 2015-01-17 |

6

5

4

3

2

1

E

E

D

D

C

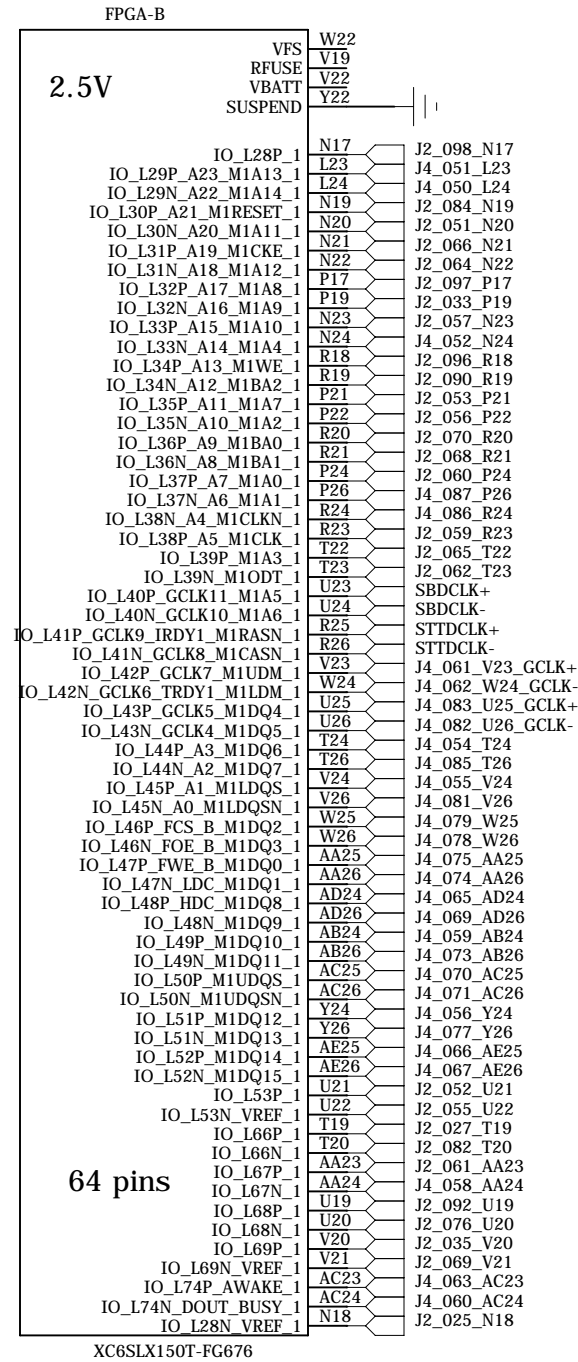
C

B

B

A

A



| | |
|---------------------|--|
| institution: | University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab |
| title: | SCROD |
| revision: | A5 |
| IDLAB design #: | IDL_15_002 |
| circuit design: | IDLAB |
| PCB design: | IDLAB |
| sheet #: | 8 |
| sheet description: | FPGA banks 0-5 |
| date last modified: | 2015-01-17 |

6

5

4

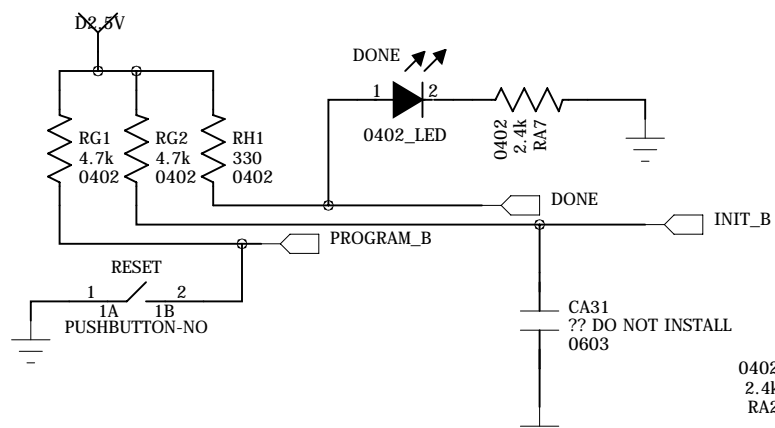
3

2

1

E

E



D2.5V M0 = 1
M1 = 0 master serial / SPI

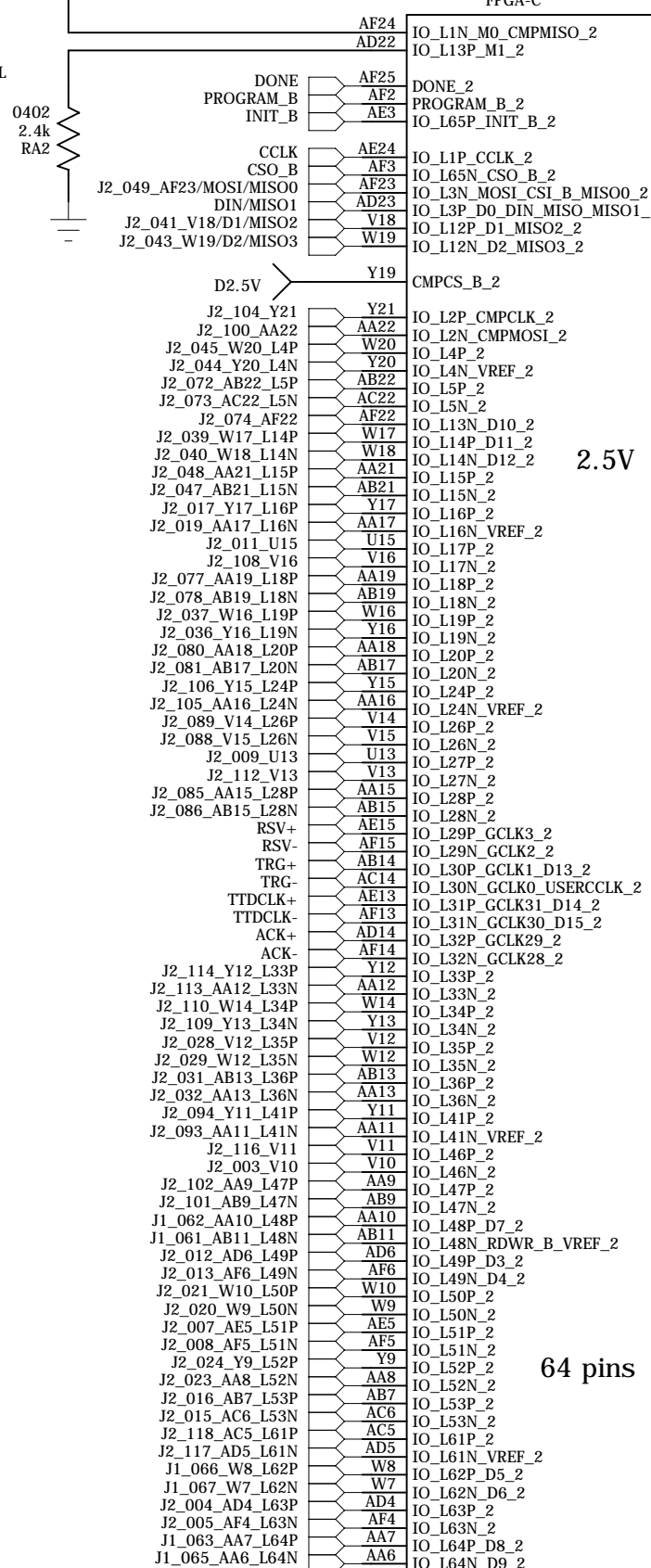
ug628 page 210/334 and ug380 page 42/66 says we don't need a pullup on done, program_b nor init_b
ug380 page 40 (note 5) suggests we need a 2.5V Vcc on the SPI flash

datasheet ug380 says on page 41, Table 2-6

Tests show that the SPI Flash(W25Q64FVSSIG) works

D

D



2.5V

64 pins

XC6SLX150T-FG676

C

C

B

B

A

A

| | |
|---------------------|--|
| institution: | University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab |
| title: | SCROD |
| revision: | A5 |
| IDLAB design #: | IDL_15_002 |
| circuit design: | IDLAB |
| PCB design: | IDLAB |
| sheet #: | 9 |
| sheet description: | FPGA banks 0-5 |
| date last modified: | 2015-01-17 |

6

5

4

3

2

1

E

E

D

D

C

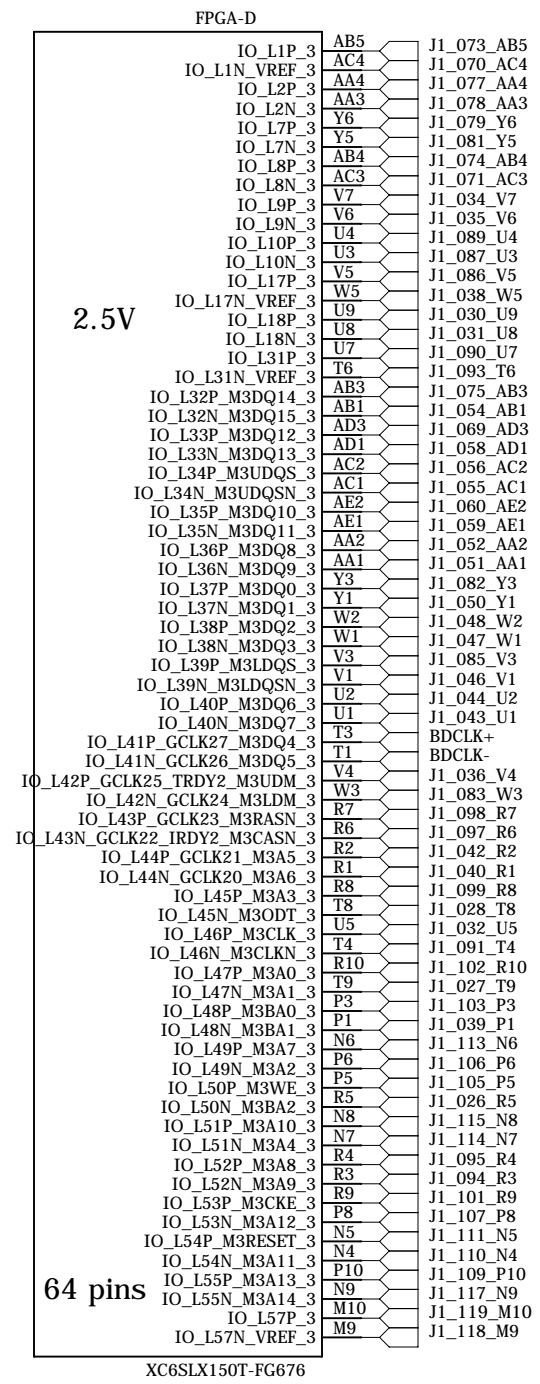
C

B

B

A

A



| | |
|---------------------|--|
| institution: | University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab |
| title: | SCROD |
| revision: | A5 |
| IDLAB design #: | IDL_15_002 |
| circuit design: | IDLAB |
| PCB design: | IDLAB |
| sheet #: | 10 |
| sheet description: | FPGA banks 0-5 |
| date last modified: | 2015-01-17 |

6

5

4

3

2

1

E

E

D

D

C

C

B

B

A

A

| FPGA-E | | |
|------------|-----|-------------------|
| J3_104_M4 | M4 | IO_L58P_4 |
| J3_110_N3 | N3 | IO_L58N_VREF_4 |
| J1_023_N2 | N2 | IO_L59P_M4DQ14_4 |
| J1_024_N1 | N1 | IO_L59N_M4DQ15_4 |
| J3_011_M3 | M3 | IO_L60P_M4DQ12_4 |
| J1_022_M1 | M1 | IO_L60N_M4DQ13_4 |
| J1_019_L2 | L2 | IO_L61P_M4UDQS_4 |
| J1_020_L1 | L1 | IO_L61N_M4UDQSN_4 |
| J3_012_K3 | K3 | IO_L62P_M4DQ10_4 |
| J1_018_K1 | K1 | IO_L62N_M4DQ11_4 |
| J1_015_J2 | J2 | IO_L63P_M4DQ8_4 |
| J1_016_J1 | J1 | IO_L63N_M4DQ9_4 |
| J3_013_H3 | H3 | IO_L64P_M4DQ0_4 |
| J1_014_H1 | H1 | IO_L64N_M4DQ1_4 |
| J1_011_G2 | G2 | IO_L65P_M4DQ2_4 |
| J1_012_G1 | G1 | IO_L65N_M4DQ3_4 |
| J3_015_F3 | F3 | IO_L66P_M4LDQS_4 |
| J1_010_F1 | F1 | IO_L66N_M4LDQSN_4 |
| J1_007_E2 | E2 | IO_L67P_M4DQ6_4 |
| J1_008_E1 | E1 | IO_L67N_M4DQ7_4 |
| J3_016_D3 | D3 | IO_L68P_M4DQ4_4 |
| J1_006_D1 | D1 | IO_L68N_M4DQ5_4 |
| J3_102_J4 | J4 | IO_L69P_M4UDM_4 |
| J3_108_J3 | J3 | IO_L69N_M4LDM_4 |
| J3_029_L9 | L9 | IO_L70P_M4RASN_4 |
| J3_093_L8 | L8 | IO_L70N_M4CASN_4 |
| J3_017_L4 | L4 | IO_L71P_M4A5_4 |
| J3_109_L3 | L3 | IO_L71N_M4A6_4 |
| J3_027_M8 | M8 | IO_L72P_M4A3_4 |
| J3_098_M6 | M6 | IO_L72N_M4ODT_4 |
| J3_020_K5 | K5 | IO_L73P_M4CLK_4 |
| J3_100_J5 | J5 | IO_L73N_M4CLKN_4 |
| J3_096_L7 | L7 | IO_L74P_M4A0_4 |
| J3_023_L6 | L6 | IO_L74N_M4A1_4 |
| J3_092_B2 | B2 | IO_L75P_M4BA0_4 |
| J1_002_B1 | B1 | IO_L75N_M4BA1_4 |
| J3_032_L10 | L10 | IO_L76P_M4A7_4 |
| J3_089_K10 | K10 | IO_L76N_M4A2_4 |
| J3_019_G4 | G4 | IO_L77P_M4WE_4 |
| J3_106_G3 | G3 | IO_L77N_M4BA2_4 |
| J3_090_J9 | J9 | IO_L78P_M4A10_4 |
| J3_094_J7 | J7 | IO_L78N_M4A4_4 |
| J1_003_C2 | C2 | IO_L79P_M4A8_4 |
| J1_004_C1 | C1 | IO_L79N_M4A9_4 |
| J3_031_K9 | K9 | IO_L80P_M4CKE_4 |
| J3_028_K8 | K8 | IO_L80N_M4A12_4 |
| J3_101_E4 | E4 | IO_L81P_M4RESET_4 |
| J3_105_E3 | E3 | IO_L81N_M4A11_4 |
| J3_025_K7 | K7 | IO_L82P_M4A13_4 |
| J3_097_K6 | K6 | IO_L82N_M4A14_4 |
| J3_024_H6 | H6 | IO_L83P_4 |
| J3_021_H5 | H5 | IO_L83N_VREF_4 |

XC6SLX150T-FG676

52 pins

2.5V

| | |
|---------------------|--|
| institution: | University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab |
| title: | SCROD |
| revision: | A5 |
| IDLAB design #: | IDL_15_002 |
| circuit design: | IDLAB |
| PCB design: | IDLAB |
| sheet #: | 11 |
| sheet description: | FPGA banks 0-5 |
| date last modified: | 2015-01-17 |

6

5

4

3

2

1

E

E

D

D

C

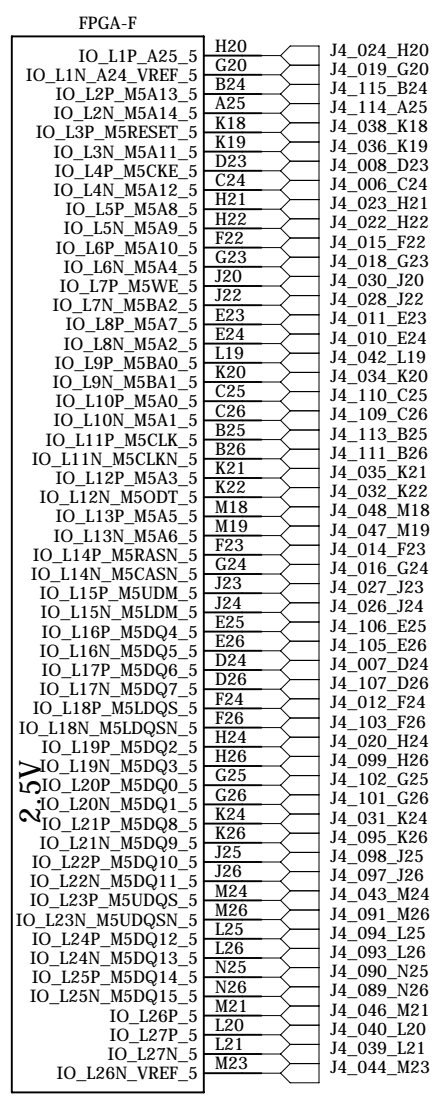
C

B

B

A

A

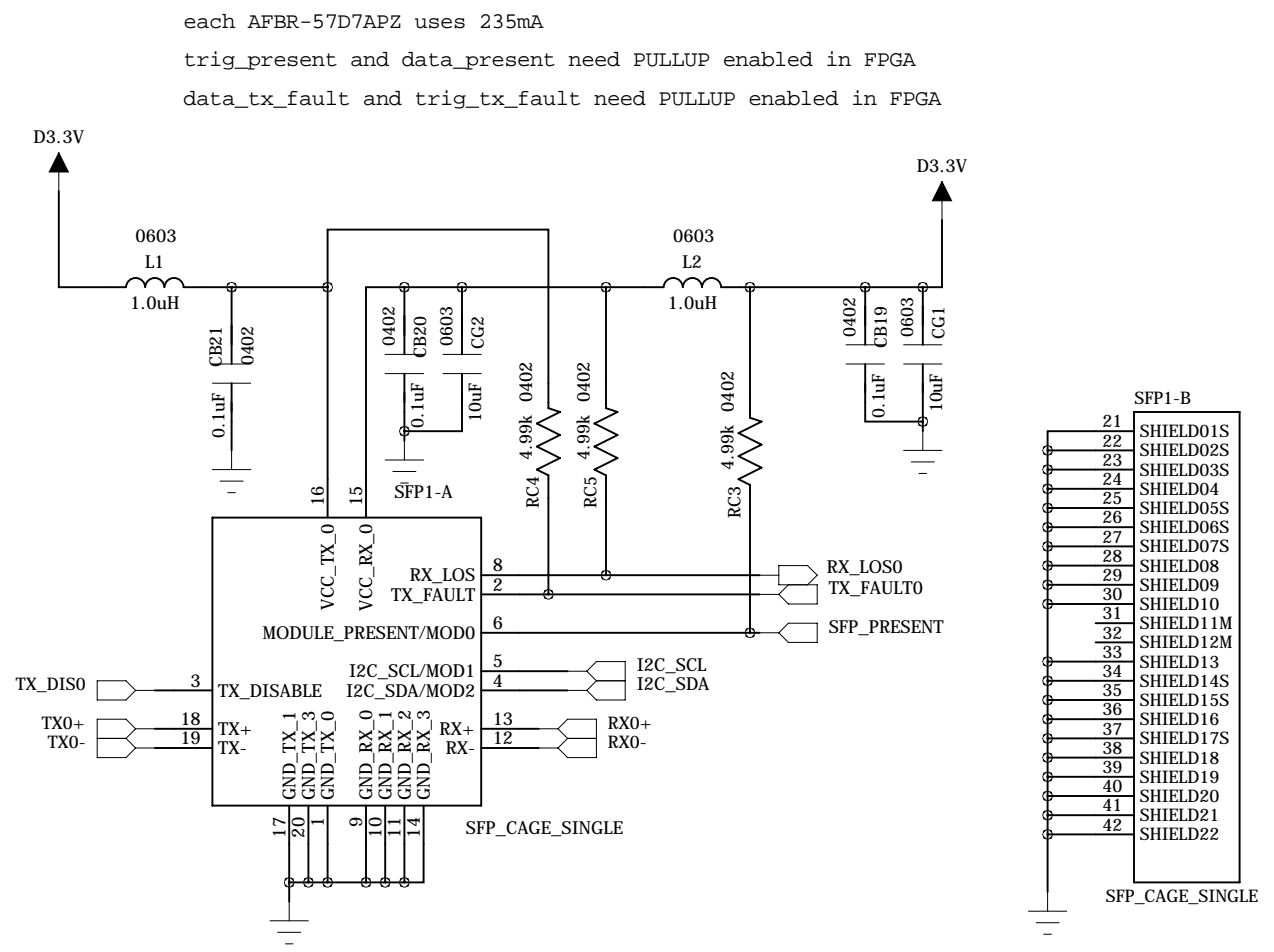
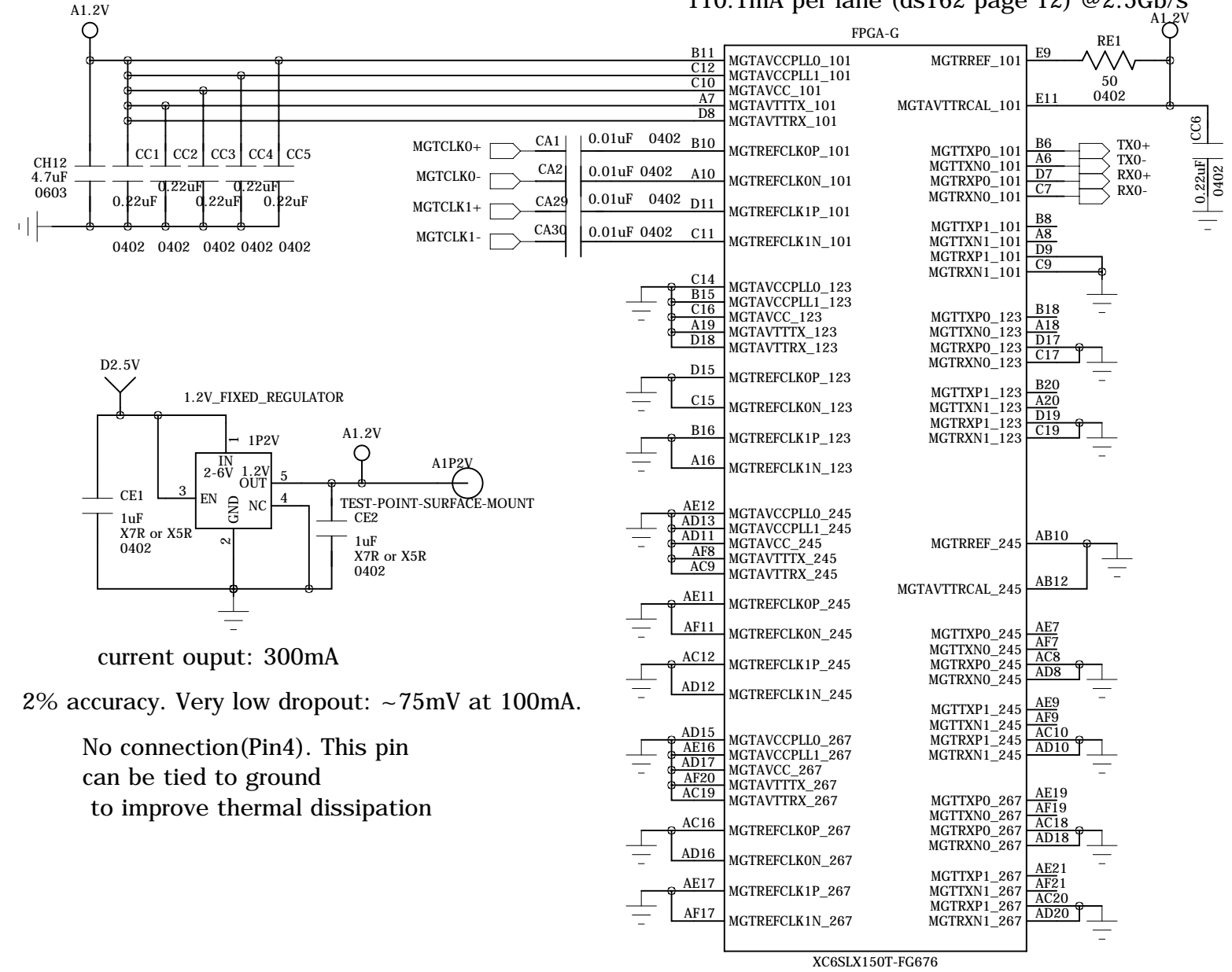


XC6SLX150T-FG676

50 pins

| | |
|---------------------|--|
| institution: | University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab |
| title: | SCROD |
| revision: | A5 |
| IDLAB design #: | IDL_15_002 |
| circuit design: | IDLAB |
| PCB design: | IDLAB |
| sheet #: | 12 |
| sheet description: | FPGA banks 0-5 |
| date last modified: | 2015-01-17 |

110.1mA per lane (ds162 page 12) @2.5Gb/s



I2C addresses = 1010000, 1010001

1.2V_FIXED_REGULATOR

current output: 300mA

2% accuracy. Very low dropout: ~75mV at 100mA.

No connection(Pin4). This pin can be tied to ground to improve thermal dissipation

| | |
|---------------------|--|
| institution: | University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab |
| title: | SCROD |
| revision: | A5 |
| IDLAB design #: | IDL_15_002 |
| circuit design: | IDLAB |
| PCB design: | IDLAB |
| sheet #: | 13 |
| sheet description: | fiber transceiver, fiber clock |
| date last modified: | 2015-01-17 |