5mil trace; outer layer trace spacing=5; inner layer spacing=8
dielectric layer thickness: 5 mil(microstrip) and 9 mil(stripline)
will work for both symmetry and asymmetry layer stackup.

SWITCH

A - Enalbe/disable local 127MHz clock

B - Voltage Regulators SHUTDOWN
should be set to "down" by default unless you want to power it alone.

C - LVDS fanout Enable

D - Remote/local JTAG

E - not used

Assembly instructions:

install 2mm 2 pin jumper header 156_DIS and 250_DIS
install GND test points

notes updated 2012-05-16
added size/package notes to schematic

notes updated 2012-10-05
added notes about bank voltages and N18/M18/L10/K10/J2/M10

2013-10-09
pcb: changed 2 pin molex connector to use bigger holes

2013-10-10
sch: changed thermal wall holes to be the skinny type

2013-10-25:

forgot pullup on $\overline{\text{shdn}}$ net for regulators
holes for power connector too small
changed note on what switch #4 does

2013-10-31:

be careful wiring up the 2 pin power connector; pin 1 on the schematic doesn't correspond to pin 1 on the connector

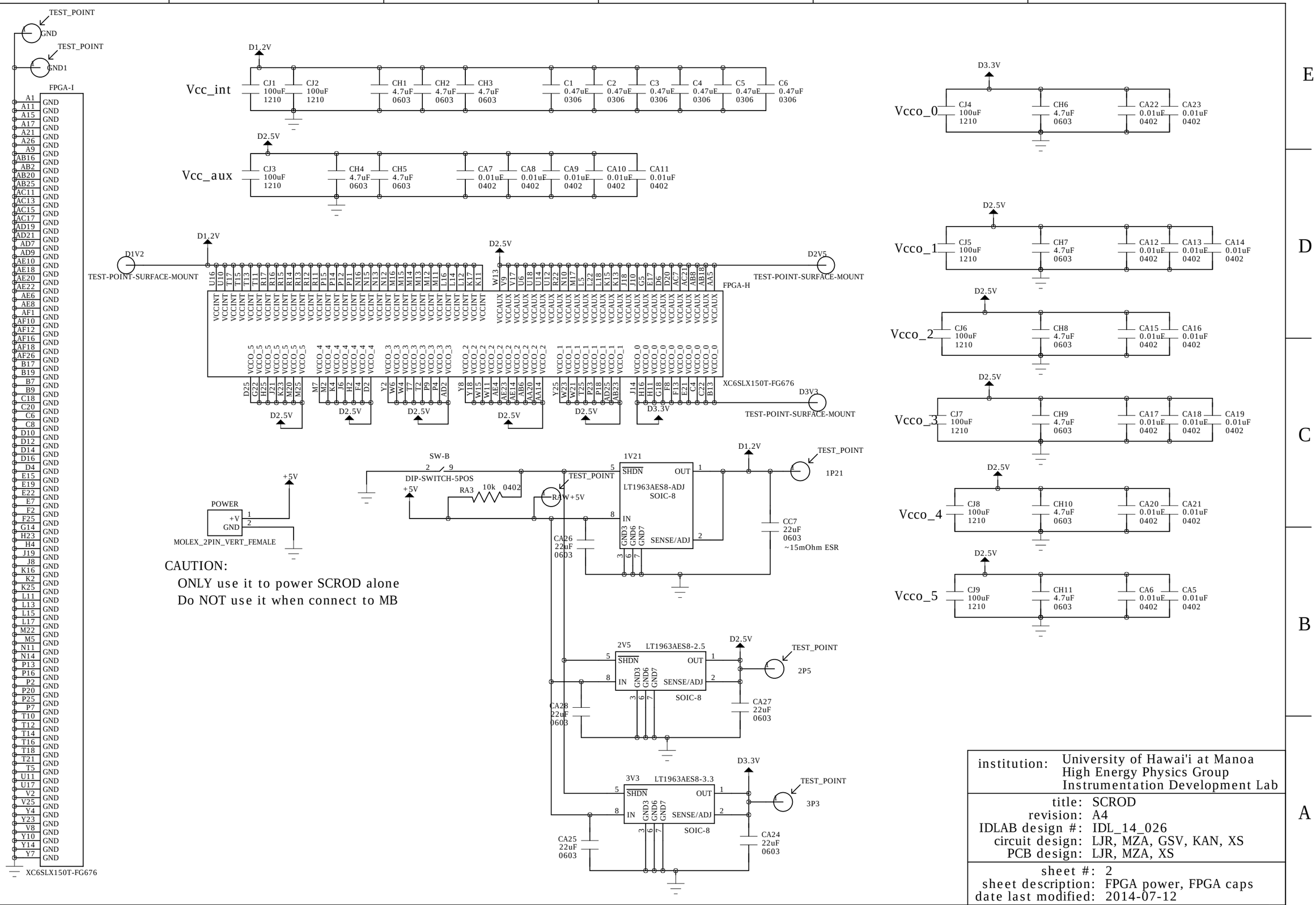
2014-01-09

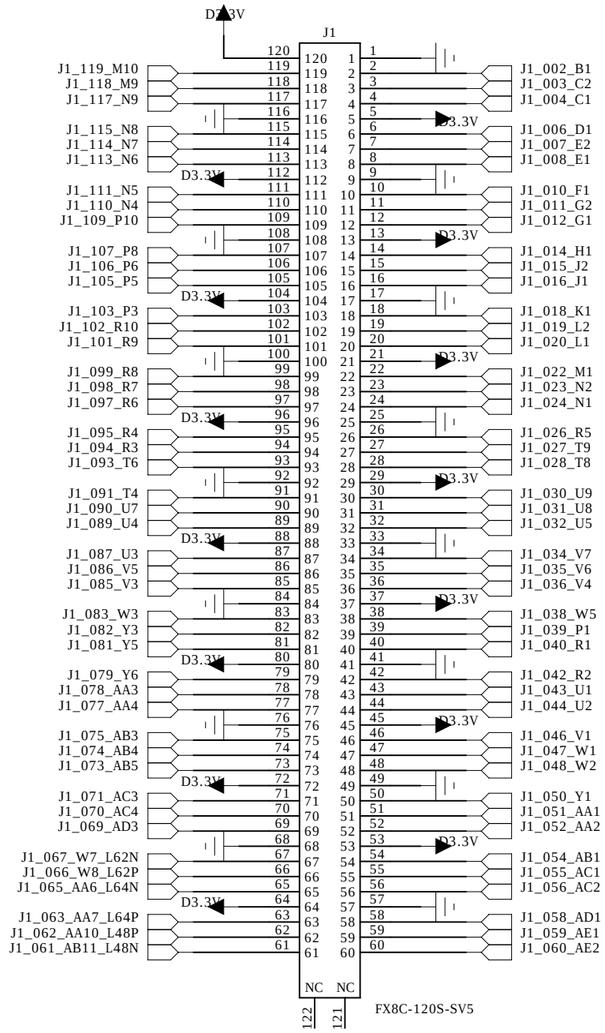
FPGA is XC6SLX150T-3FGG676I (RoHS; speed grade 3; industrial temp)

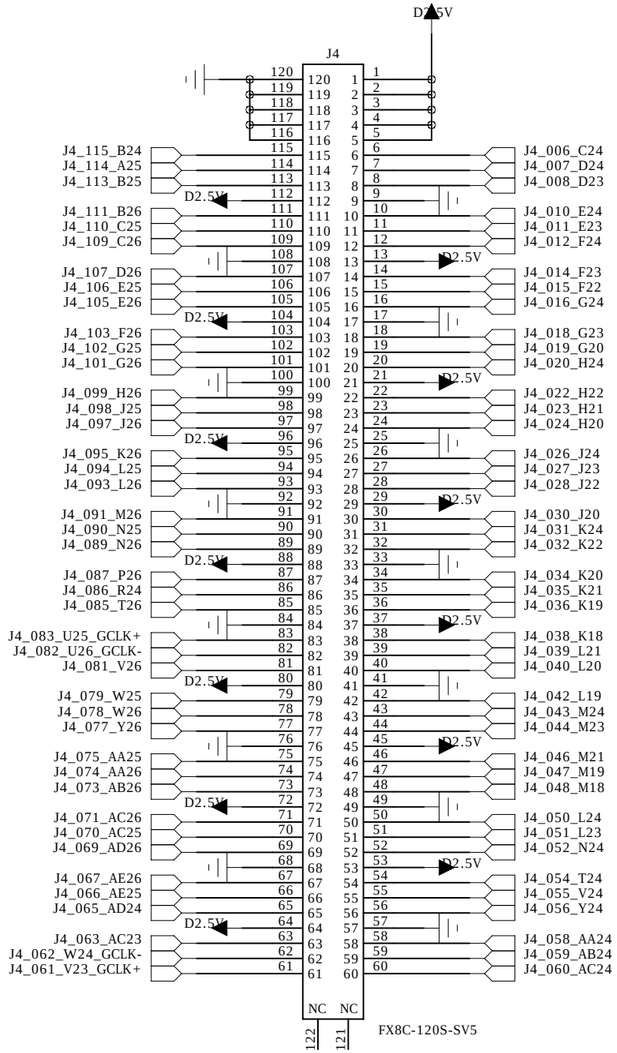
2014-02-12:

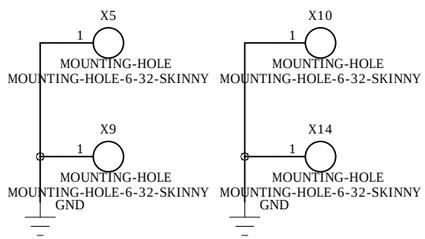
noticed that DIP sw for disconnecting cypress eeprom should probably be on other side of pull-up resistor

| | |
|---|---|
| institution: | University of Hawai'i at Manoa<br>High Energy Physics Group<br>Instrumentation Development Lab |
| title: | SCROD |
| revision: | A4 |
| IDLAB design #: | IDL_14_026 |
| circuit design: | LJR, MZA, GSV, KAN, XS |
| PCB design: | LJR, MZA, XS |
| sheet #: | 1 |
| sheet description: | block diagram |
| date last modified: | 2014-07-12 |


TEST_POINT
GND
TEST_POINT
GND1
FPGA-I
XC6SLX150T-FG676
D1.2V
Vcc_int
CJ1 100uF 1210
CJ2 100uF 1210
CH1 4.7uF 0603
CH2 4.7uF 0603
CH3 4.7uF 0603
C1 0.47uF 0306
C2 0.47uF 0306
C3 0.47uF 0306
C4 0.47uF 0306
C5 0.47uF 0306
C6 0.47uF 0306
D2.5V
Vcc_aux
CJ3 100uF 1210
CH4 4.7uF 0603
CH5 4.7uF 0603
CA7 0.01uF 0402
CA8 0.01uF 0402
CA9 0.01uF 0402
CA10 0.01uF 0402
CA11 0.01uF 0402
D1V2
TEST-POINT-SURFACE-MOUNT
D2V5
TEST-POINT-SURFACE-MOUNT
FPGA-H
XC6SLX150T-FG676
D3V3
TEST-POINT-SURFACE-MOUNT
POWER
+V
GND
MOLEX_2PIN_VERT_FEMALE
+5V
CAUTION:
ONLY use it to power SCROD alone
Do NOT use it when connect to MB
SW-B
DIP-SWITCH-5POS
RA3 10k 0402
TEST_POINT
1V21
LT1963AES8-ADJ
SOIC-8
SHDN
OUT
IN
SENSE/ADJ
GND3
GND6
GND7
D1.2V
TEST_POINT
1P21
CC7 22uF 0603 ~15mOhm ESR
CA26 22uF 0603
2V5
LT1963AES8-2.5
D2.5V
TEST_POINT
2P5
CA27 22uF 0603
CA28 22uF 0603
3V3
LT1963AES8-3.3
D3.3V
TEST_POINT
3P3
CA24 22uF 0603
CA25 22uF 0603
D3.3V
Vcco_0
CJ4 100uF 1210
CH6 4.7uF 0603
CA22 0.01uF 0402
CA23 0.01uF 0402
D2.5V
Vcco_1
CJ5 100uF 1210
CH7 4.7uF 0603
CA12 0.01uF 0402
CA13 0.01uF 0402
CA14 0.01uF 0402
Vcco_2
CJ6 100uF 1210
CH8 4.7uF 0603
CA15 0.01uF 0402
CA16 0.01uF 0402
Vcco_3
CJ7 100uF 1210
CH9 4.7uF 0603
CA17 0.01uF 0402
CA18 0.01uF 0402
CA19 0.01uF 0402
Vcco_4
CJ8 100uF 1210
CH10 4.7uF 0603
CA20 0.01uF 0402
CA21 0.01uF 0402
Vcco_5
CJ9 100uF 1210
CH11 4.7uF 0603
CA6 0.01uF 0402
CA5 0.01uF 0402
institution: University of Hawai'i at Manoa
High Energy Physics Group
Instrumentation Development Lab
title: SCROD
revision: A4
IDLAB design #: IDL_14_026
circuit design: LJR, MZA, GSV, KAN, XS
PCB design: LJR, MZA, XS
sheet #: 2
sheet description: FPGA power, FPGA caps
date last modified: 2014-07-12




| | |
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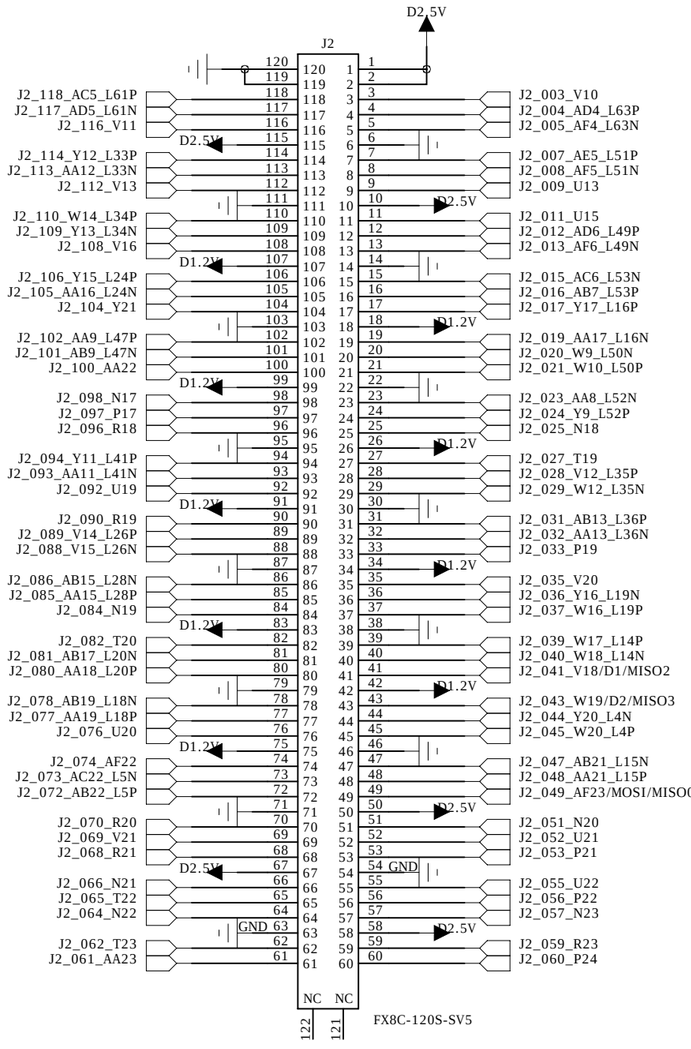
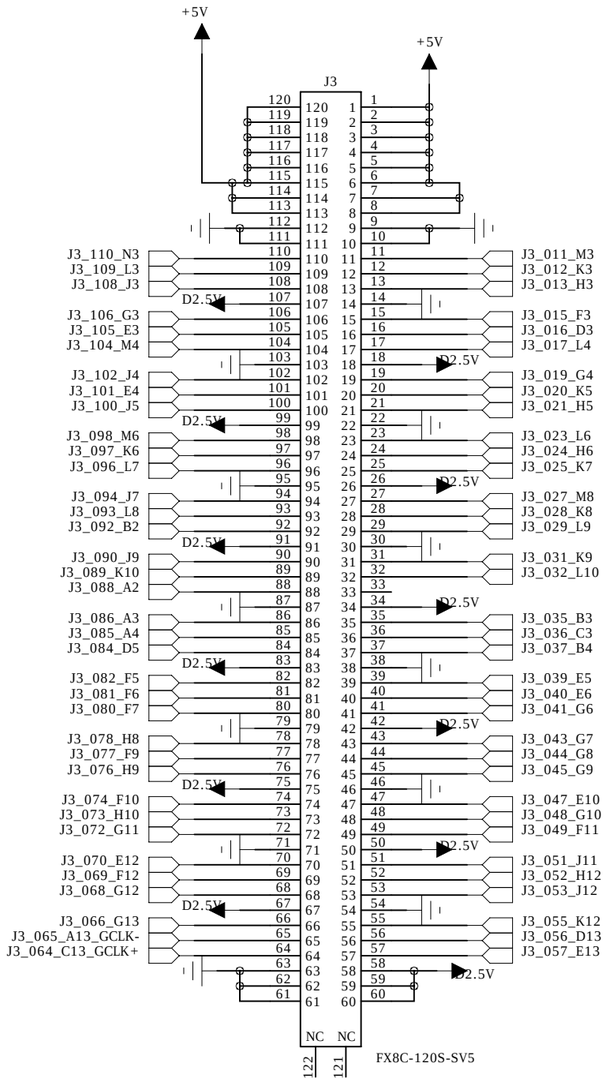
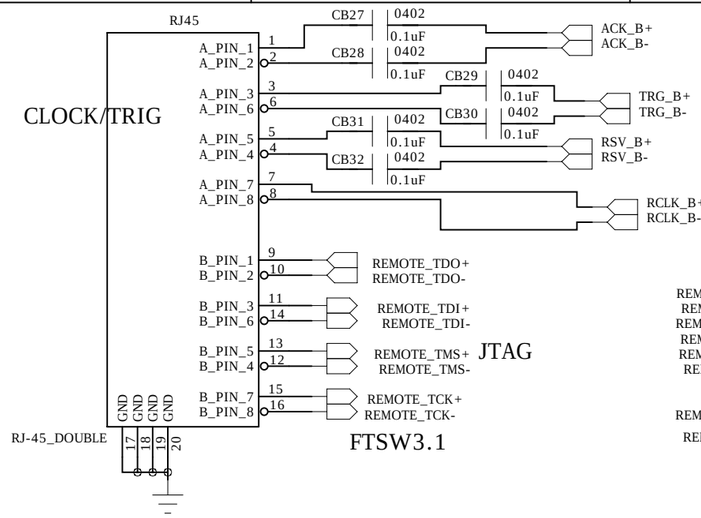
| institution: | University of Hawai'i at Manoa<br>High Energy Physics Group<br>Instrumentation Development Lab |
| title: | SCROD |
| revision: | A4 |
| IDLAB design #: | IDL_14_026 |
| circuit design: | LJR, MZA, GSV, KAN, XS |
| PCB design: | LJR, MZA, XS |
| sheet #: | 3 |
| sheet description: | board-to-board interconnects |
| date last modified: | 2014-07-12 |

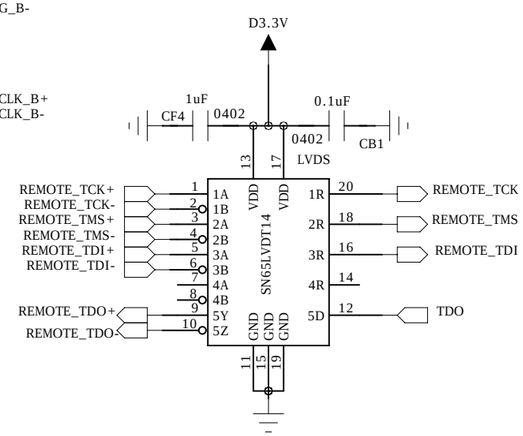
a backup option to power the SCROD using +5V on the MB

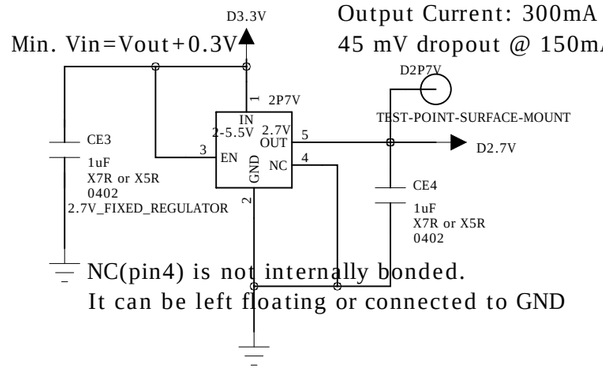



| | |
|---|---|
| institution: | University of Hawai'i at Manoa<br>High Energy Physics Group<br>Instrumentation Development Lab |
| title: | SCROD |
| revision: | A4 |
| IDLAB design #: | IDL_14_026 |
| circuit design: | LJR, MZA, GSV, KAN, XS |
| PCB design: | LJR, MZA, XS |
| sheet #: | 4 |
| sheet description: | board-to-board interconnects |
| date last modified: | 2014-07-12 |

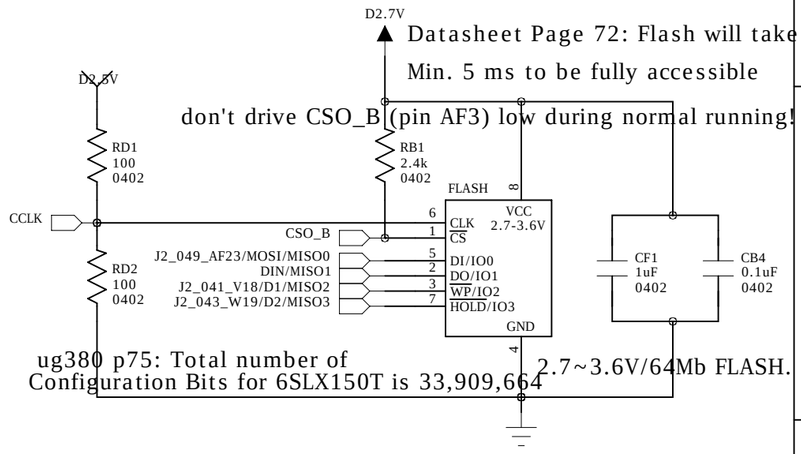



Min. Input High Voltage:2.7V * 0.7 = 1.89V

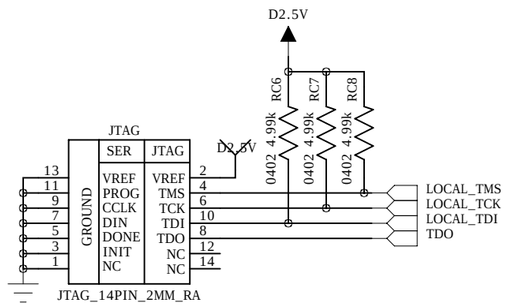
change D3.3V TO D2.7V  Max. Current Chip Erase: 25 mA

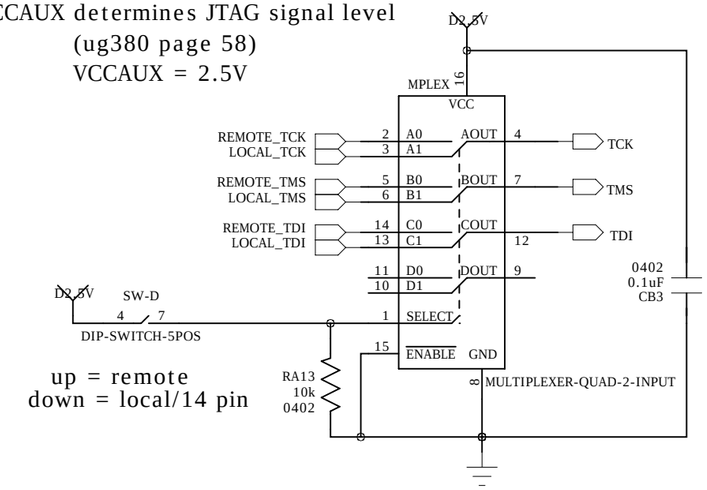


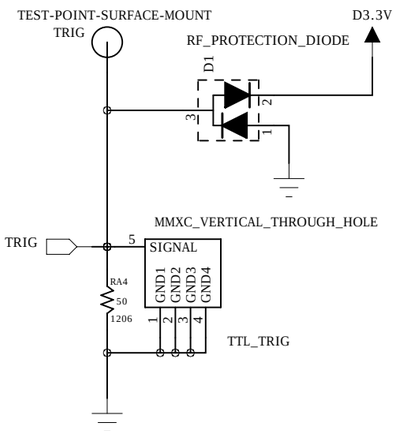

ug380 p75: Total number of Configuration Bits for 6SLX150T is 33,909,664

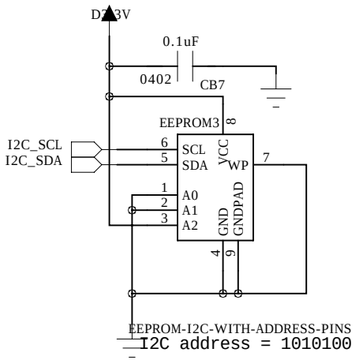
2.7~3.6V/64Mb FLASH.

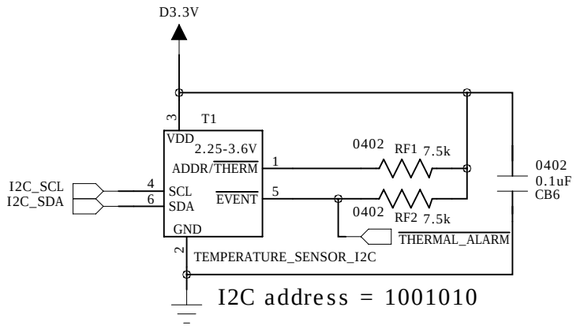
VCCAUX determines JTAG signal level
(ug380 page 58)
VCCAUX = 2.5V

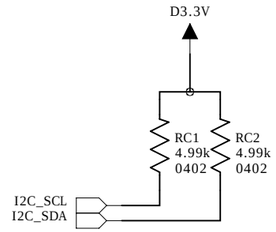


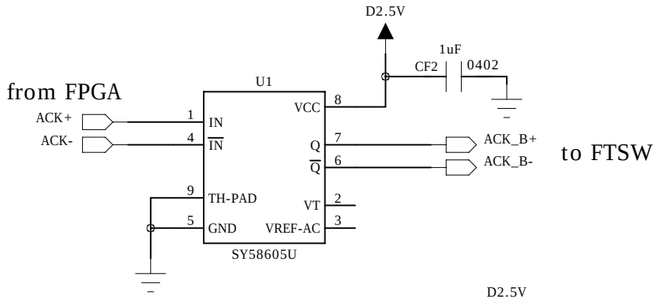



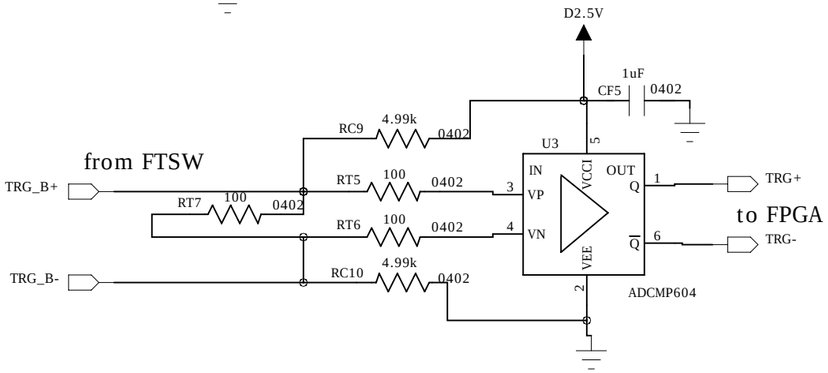



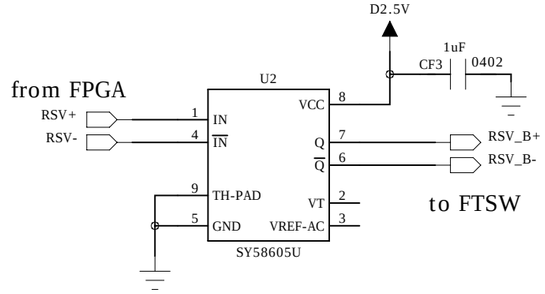

| | |
|---|---|
| institution: | University of Hawai'i at Manoa<br>High Energy Physics Group<br>Instrumentation Development Lab |
| title: | SCROD |
| revision: | A4 |
| IDLAB design #: | IDL_14_026 |
| circuit design: | LJR, MZA, GSV, KAN, XS |
| PCB design: | LJR, MZA, XS |
| sheet #: | 5 |
| sheet description: | JTAG, CLOCK, LEDs, PROM |
| date last modified: | 2014-07-12 |



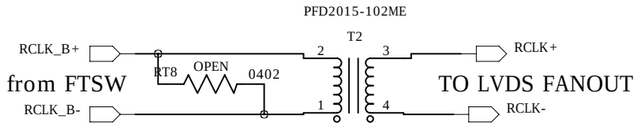

to FTSW

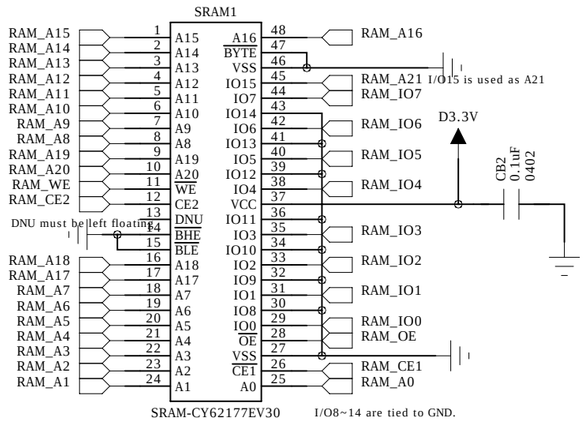



to FPGA

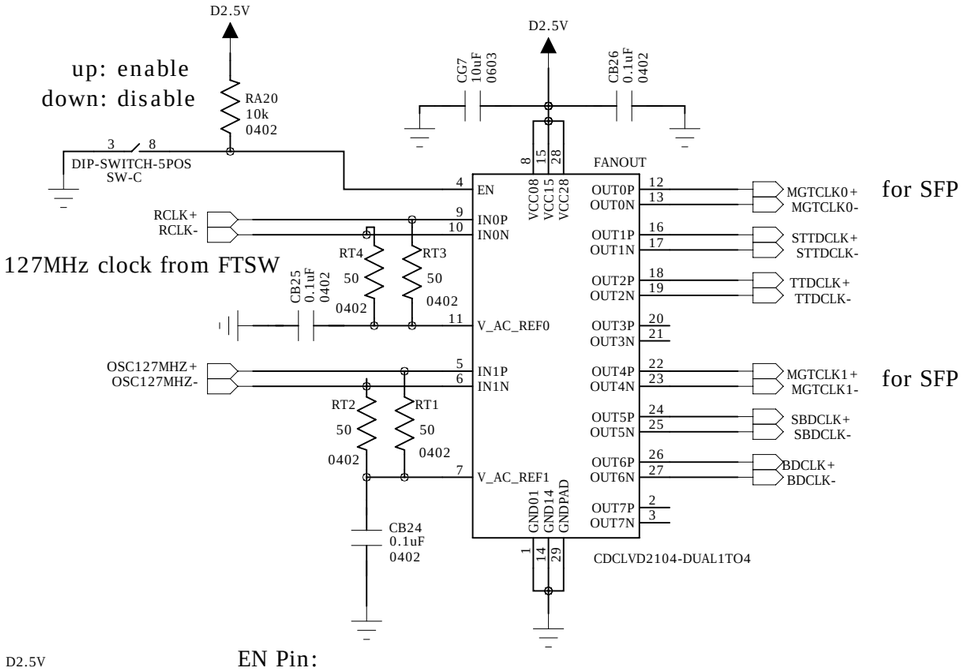



to FTSW




RAM uses 34 FPGA I/O Pins(3.3V bank).



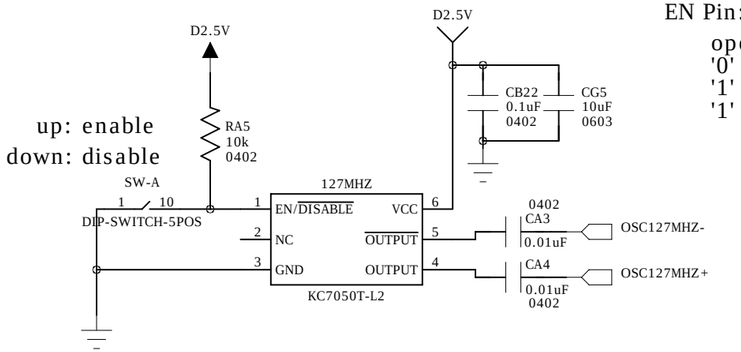

127MHz clock from FTSW

for SFP

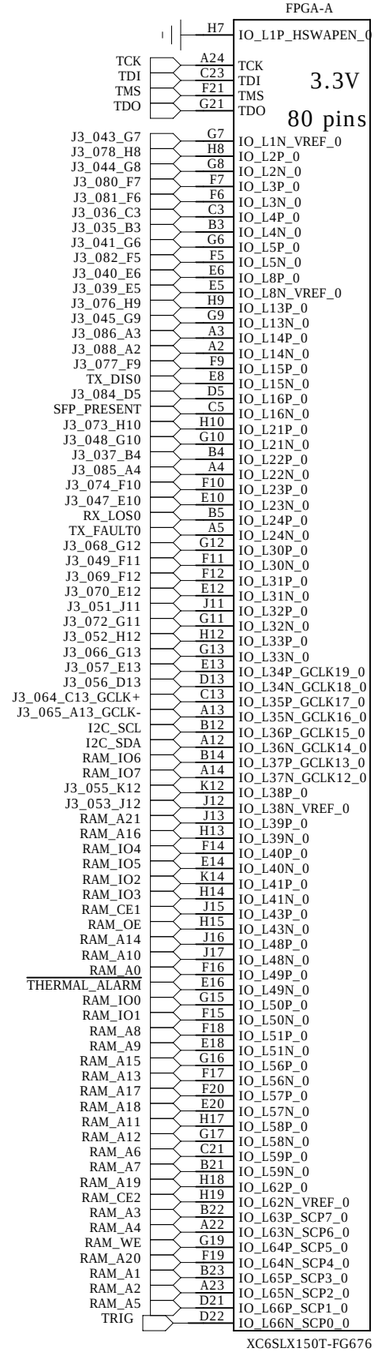
for SFP

EN Pin:

open -> two buffers with all outputs are enabled.
'0' -> two buffers with all outputs are disabled.
'1' -> one buffers enabled and one disabled.
'1' -> OUT0, OUT3 enabled and OUT4, OUT7 disabled

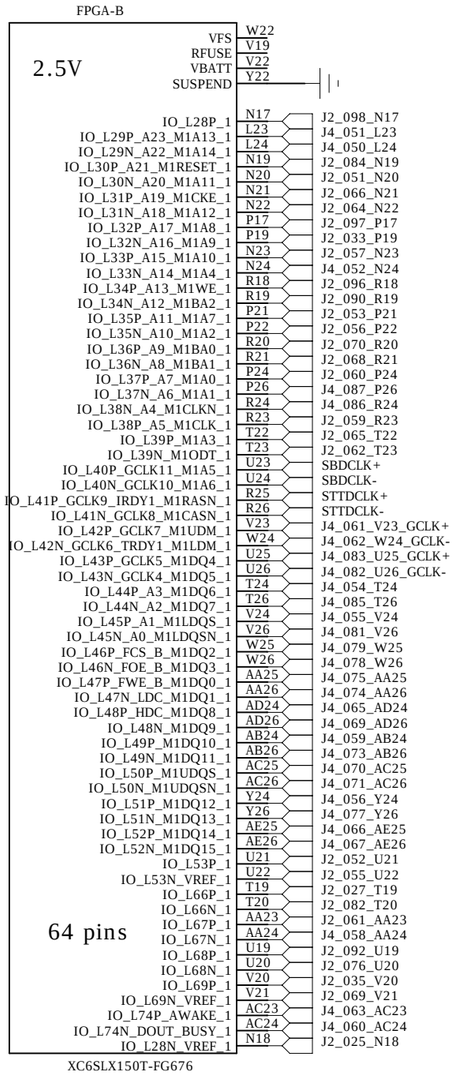



| | |
|---|---|
| institution: | University of Hawai'i at Manoa<br>High Energy Physics Group<br>Instrumentation Development Lab |
| title: | SCROD |
| revision: | A4 |
| IDLAB design #: | IDL_14_026 |
| circuit design: | LJR, MZA, GSV, KAN, XS |
| PCB design: | LJR, MZA, XS |
| sheet #: | 6 |
| sheet description: | block diagram |
| date last modified: | 2014-07-12 |

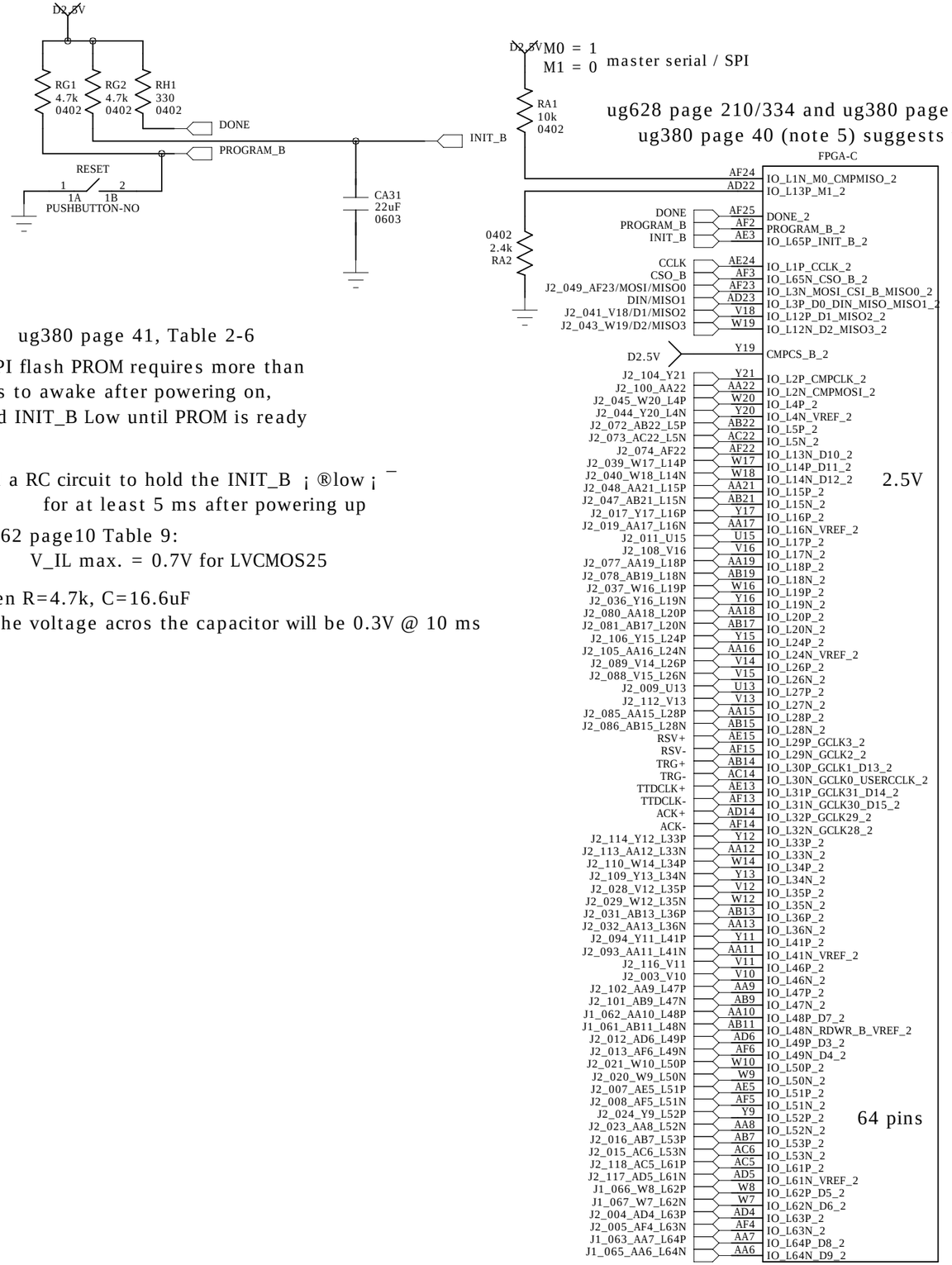



added bank pin counts

| | |
|---|---|
| institution: | University of Hawai'i at Manoa<br>High Energy Physics Group<br>Instrumentation Development Lab |
| title: | SCROD |
| revision: | A4 |
| IDLAB design #: | IDL_14_026 |
| circuit design: | LJR, MZA, GSV, KAN, XS |
| PCB design: | LJR, MZA, XS |
| sheet #: | 7 |
| sheet description: | FPGA banks 0-5 |
| date last modified: | 2014-07-12 |




| | |
|---|---|
| institution: | University of Hawai'i at Manoa<br>High Energy Physics Group<br>Instrumentation Development Lab |
| title: | SCROD |
| revision: | A4 |
| IDLAB design #: | IDL_14_026 |
| circuit design: | LJR, MZA, GSV, KAN, XS |
| PCB design: | LJR, MZA, XS |
| sheet #: | 8 |
| sheet description: | FPGA banks 0-5 |
| date last modified: | 2014-07-12 |




ug628 page 210/334 and ug380 page 42/66 says we don't need a pullup on done, program_b nor init_b
ug380 page 40 (note 5) suggests we need a 2.5V Vcc on the SPI flash

ug380 page 41, Table 2-6

If SPI flash PROM requires more than
2 ms to awake after powering on,
hold INIT_B Low until PROM is ready

add a RC circuit to hold the INIT_B ¡ ®low ¡ ¯
for at least 5 ms after powering up

ds162 page10 Table 9:
V_IL max. = 0.7V for LVCMOS25

when R=4.7k, C=16.6uF
the voltage acros the capacitor will be 0.3V @ 10 ms

| | |
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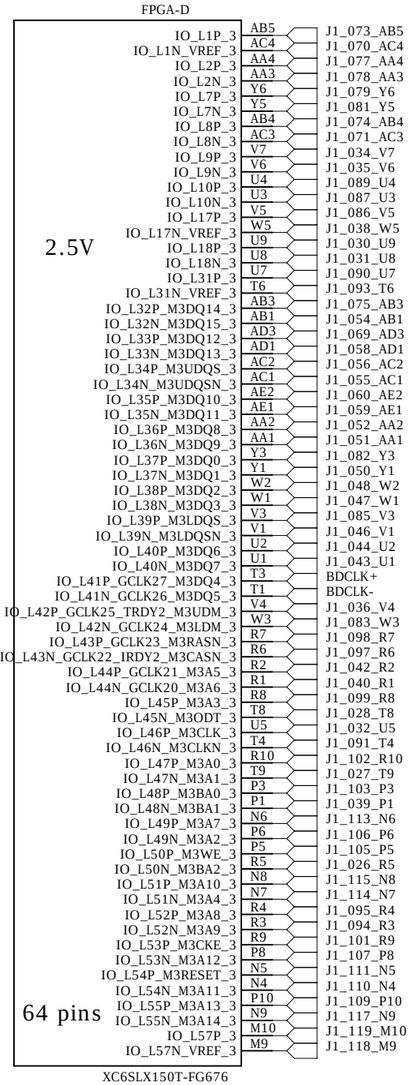
| institution: | University of Hawai'i at Manoa<br>High Energy Physics Group<br>Instrumentation Development Lab |
| title: | SCROD |
| revision: | A4 |
| IDLAB design #: | IDL_14_026 |
| circuit design: | LJR, MZA, GSV, KAN, XS |
| PCB design: | LJR, MZA, XS |
| sheet #: | 9 |
| sheet description: | FPGA banks 0-5 |
| date last modified: | 2014-07-12 |




| | |
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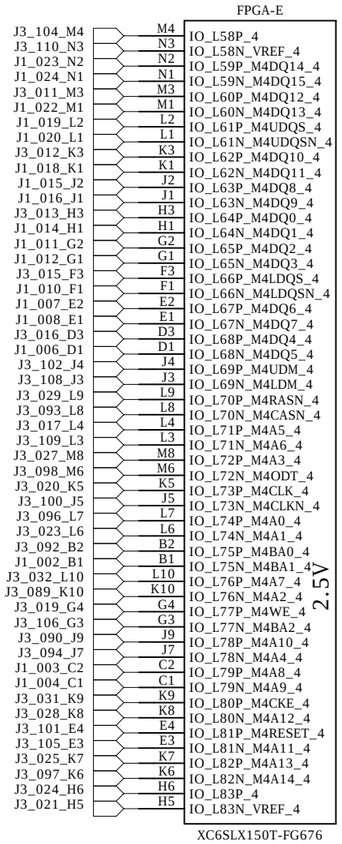
| institution: | University of Hawai'i at Manoa<br>High Energy Physics Group<br>Instrumentation Development Lab |
| title: | SCROD |
| revision: | A4 |
| IDLAB design #: | IDL_14_026 |
| circuit design: | LJR, MZA, GSV, KAN, XS |
| PCB design: | LJR, MZA, XS |
| sheet #: | 10 |
| sheet description: | FPGA banks 0-5 |
| date last modified: | 2014-07-12 |

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|---|---|
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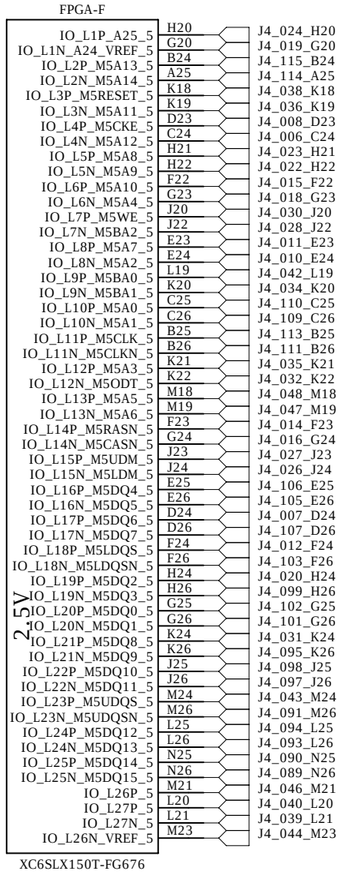
| title: | SCROD |
| revision: | A4 |
| IDLAB design #: | IDL_14_026 |
| circuit design: | LJR, MZA, GSV, KAN, XS |
| PCB design: | LJR, MZA, XS |
| sheet #: | 11 |
| sheet description: | FPGA banks 0-5 |
| date last modified: | 2014-07-12 |




50 pins

| | |
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| title: | SCROD |
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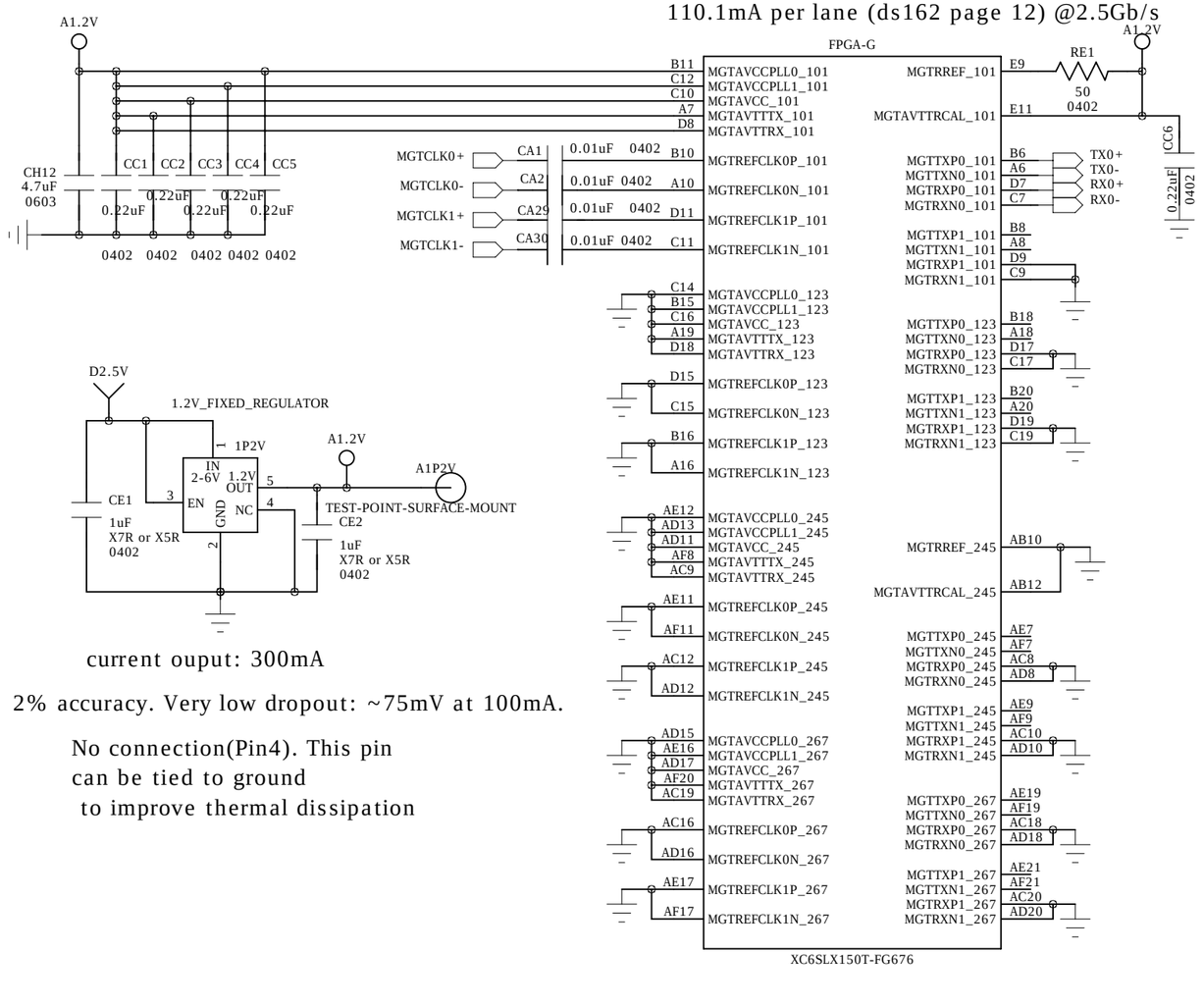
| IDLAB design #: | IDL_14_026 |
| circuit design: | LJR, MZA, GSV, KAN, XS |
| PCB design: | LJR, MZA, XS |
| sheet #: | 12 |
| sheet description: | FPGA banks 0-5 |
| date last modified: | 2014-07-12 |




| | |
|---|---|
| institution: | University of Hawai'i at Manoa<br>High Energy Physics Group<br>Instrumentation Development Lab |
| title: | SCROD |
| revision: | A4 |
| IDLAB design #: | IDL_14_026 |
| circuit design: | LJR, MZA, GSV, KAN, XS |
| PCB design: | LJR, MZA, XS |
| sheet #: | 13 |
| sheet description: | fiber transceiver, fiber clock |
| date last modified: | 2014-07-12 |