High Energy Physics Group
Instrumentation Development Laboratory
2505 Correa Road, Honolulu, HI 96822

Production Documentation for:

Project Name:	***HMB***
Board Name:	***SCROD_TO_RJ45_BOARD***
IDL num:	***IDL_18_020***
Revision:	***A***
Variant:	***[No Variations]***
Designer:	***Khanh Le***
Drawn by:	***Khanh Le***
Approved by:	***Gary S. Varner***

2x4 right angle RJ45 connector

Notes:
-If internal FPGA diff termination is not available install 100ohm resisters

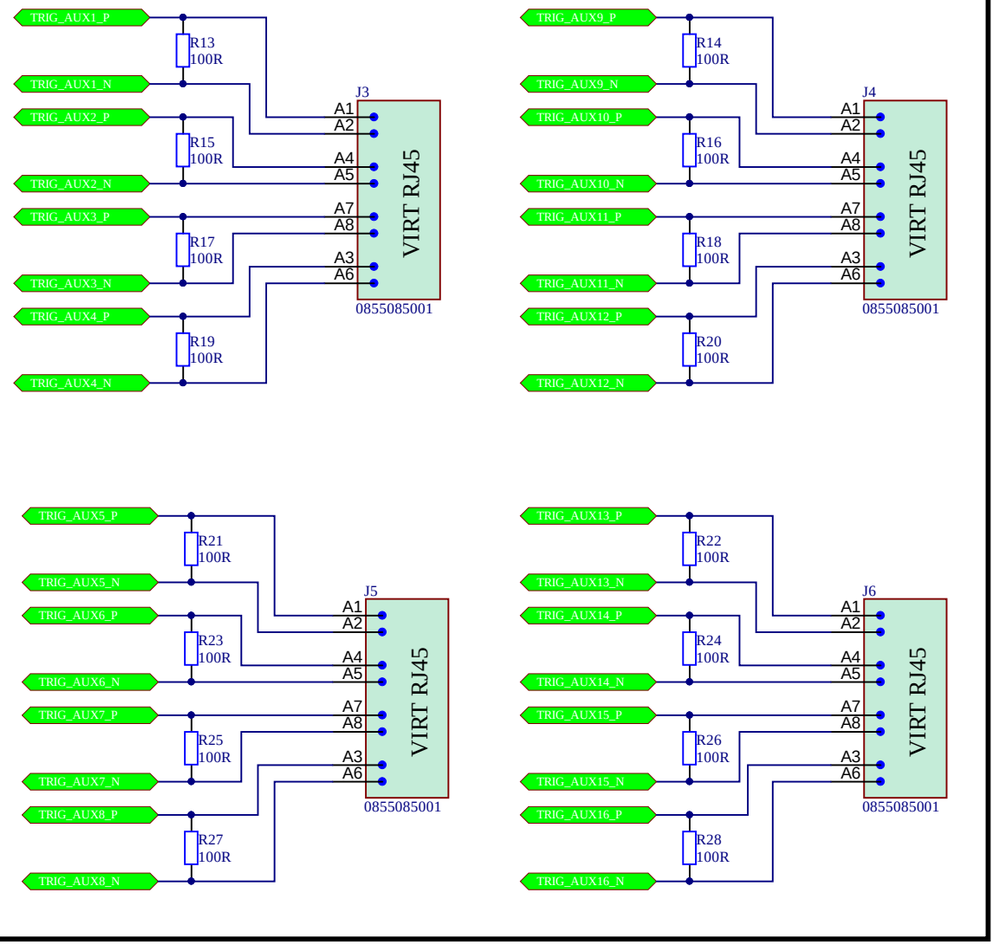
L1

IDLab Logo

IDLab Logo

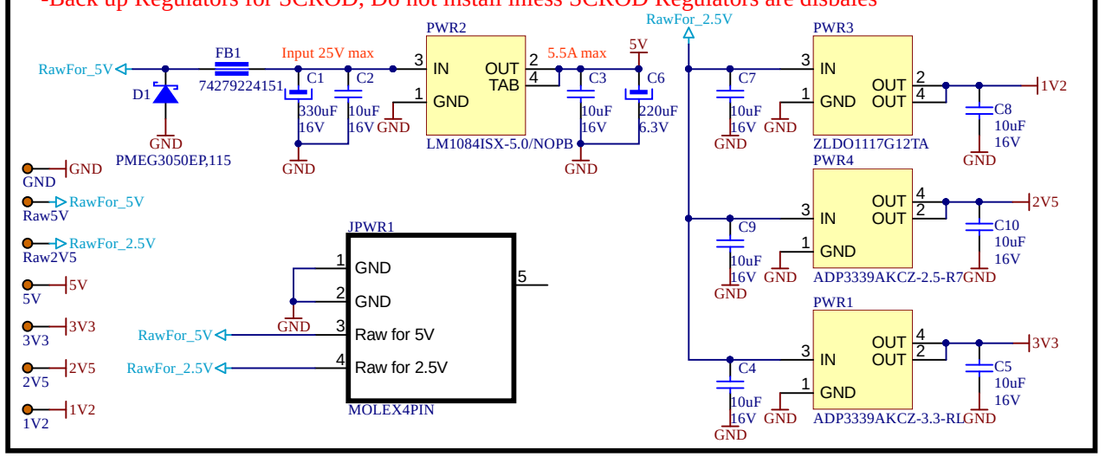
Verticle RJ45 connector

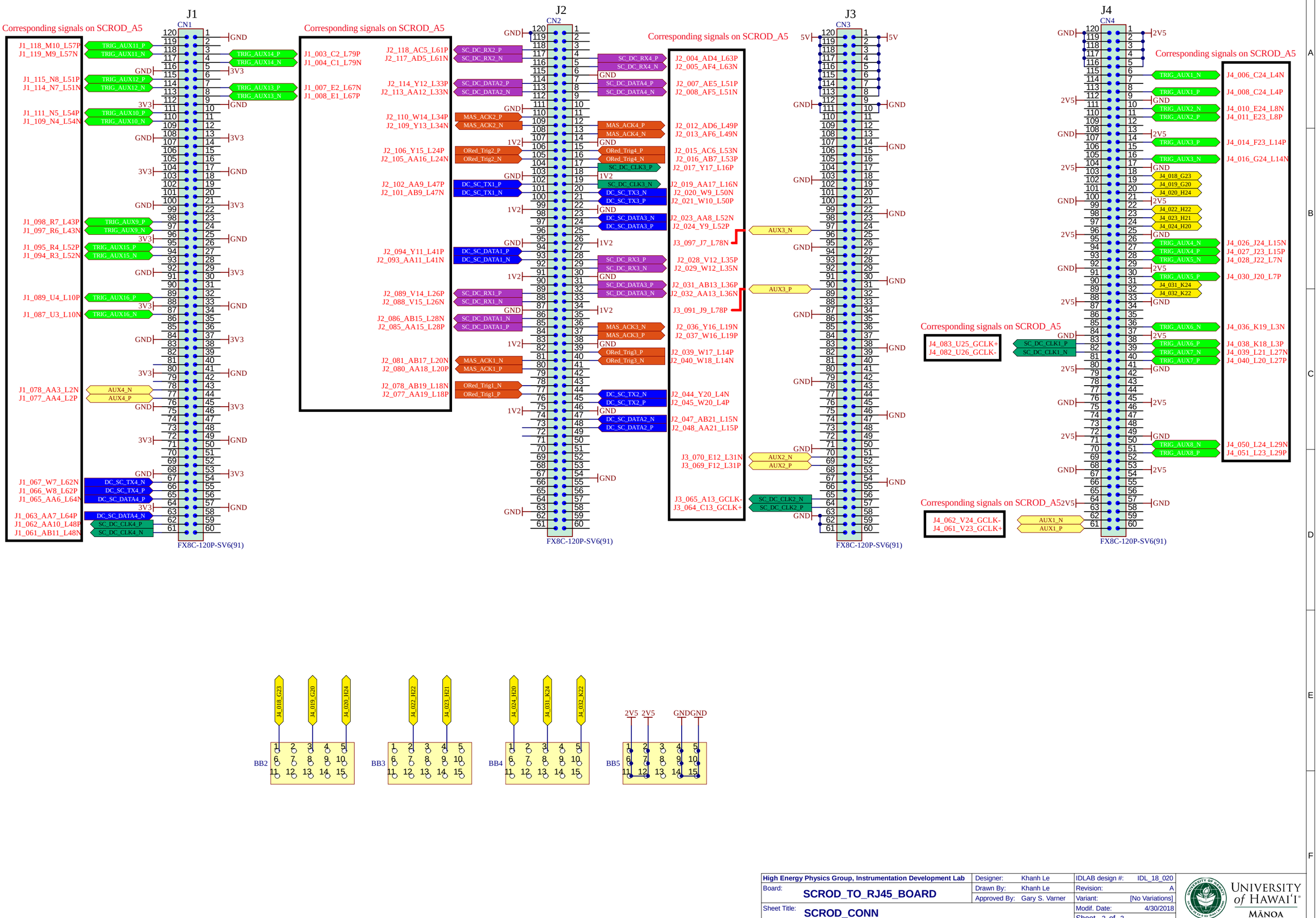
Notes:
-If internal FPGA diff termination is not available install 100ohm resisters



Power reg connector

Notes:
-Back up Regulators for SCROD, Do not install inless SCROD Regulators are disbales





High Energy Physics Group, Instrumentation Development Lab	Designer: Khanh Le	IDLAB design #: IDL_18_020	
Board: SCROD_TO_RJ45_BOARD	Drawn By: Khanh Le	Revision: A	
	Approved By: Gary S. Varner	Variant: [No Variations]	
Sheet Title: SCROD_CONN		Modif. Date: 4/30/2018	
		Sheet 3 of 3	

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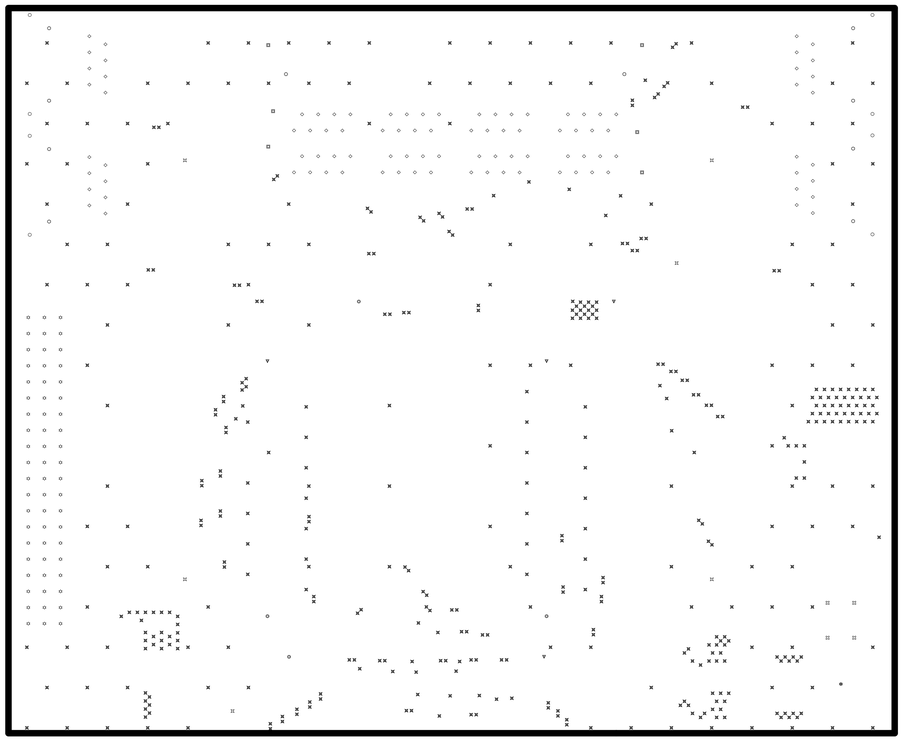

Notes:

1. Board shall be fabricated - performace class II as per IPC-6011 and IPC6012
2. PCB manufacturer logo, P/N, revision and/or date code of manufacturing
   shall be printed in top solder mask (not over pcb traces, allowed over copper plane).
   The date code shall be in the format: "WWYY" where WW=week and YY= year, max height 0.15 inches
3. Silkscreen printed on both sides
4. Material: high temperature FR4 class epoxy glass rated UL94V-0. UL symbol and rating shall be marked farside
   35um copper for external layers and 18um for all internal layers
   Must be RoHS compliant and survive a lead-free assembly max reflow of 260 deg C (5 passes)
   Td rating: >340 deg C
   Tg = 150 deg C (min)
5. Solder mask: SMOBC per IPC-SM-840C, class T must be Rohs compliant, 0.001" max measured over bare copper plating,
   must clear all lands as indicated on gerber solder mask layers, color= GREEN
6. Finish: electro-less nickel immersion gold (ENIG), 0.05-0.125um Au over 3-6um Ni - over bare copper only
7. Solderability test: Category 2 of J-STD-003
8. Finished boards shall not have nicks, scratches, voids, exposed copper, poor plating or misdrilled holes
9. All holes sizes are after plating
10. PCB manufacturer may add copper thieving as needed to improve manufacturability,
    thieving to be 0.030" round pads at 0.050" spacing.
    Thieving will have a minimum of 0.100" clearance from existing copper and should not be placed under surface mounted devices
11. PCB manufacturer may use tear drops to improve annular rings as long as DRC rules are followed
12. All via connections to power and ground planes are solid
13. All unconnected pads on inner signal layers are removed
14. All finished boards are to be 100% electrically tested
15. Unless otherwise indicated, all linear toleracnes shall be XX.X +/-0.2mm and XX.XX +/- 0.1mm
16. Gerber file GM1 shows board outline (milling line)
17. Table 1 shows Layer stack details

Table 1a: Layer Stack Details in mils for IDL_17_009 Rev.A

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack
1	Top Overlay					
2	Top Solder	Solder Resist	0.40mil	3.5		
3	Top Layer	Copper	1.38mil			
4	Dielectric 1	FR-4	9.00mil	4.65		
5	MID PWR	Copper	1.42mil			
6	Dielectric 2	FR-4	37.61mil	4.65		
7	MID GND	Copper	1.42mil			
8	Dielectric 3	FR-4	9.00mil	4.65		
9	Bottom Layer	Copper	1.38mil			
10	Bottom Solder	Solder Resist	0.40mil	3.5		
11	Bottom Overlay					

Table 1b: Layer Stack Details in mm for IDL_17_009 Rev.A

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack
1	Top Overlay					
2	Top Solder	Solder Resist	0.010mm	3.5		
3	Top Layer	Copper	0.035mm			
4	Dielectric 1	FR-4	0.229mm	4.65		
5	MID PWR	Copper	0.036mm			
6	Dielectric 2	FR-4	0.955mm	4.65		
7	MID GND	Copper	0.036mm			
8	Dielectric 3	FR-4	0.229mm	4.65		
9	Bottom Layer	Copper	0.035mm			
10	Bottom Solder	Solder Resist	0.010mm	3.5		
11	Bottom Overlay					

Table 2: Drill Details for IDL_17_002 Rev.A

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape
	1	118.11mil (3.000mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded
	4	27.56mil (0.700mm)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded
	4	43.31mil (1.100mm)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded
	4	72.00mil (1.829mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded
	6	61.81mil (1.570mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded
	6	150.00mil (3.810mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded
	8	62.99mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded
	10	127.95mil (3.250mm)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded
	60	50.00mil (1.270mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rectangle
	96	35.43mil (0.900mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded
	477	12.00mil (0.305mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded
	676 Total						

Designer: Khanh Le	Revision: .Version	File: IDL_18_020.PcbDoc	Sheet 1 of 1
Drawn By: Khanh Le	Modif. Date: Date	Variant: [No Variations]	PCB
Approved By: Gary S. Varner	Print Date: 4/30/2018	Signature:	Size: A3 H

Title: Drill Drawing and Dimensions GD1

Code: **IDL_18_020**

ID: **SCROD_TO_RJ45_BOARD**

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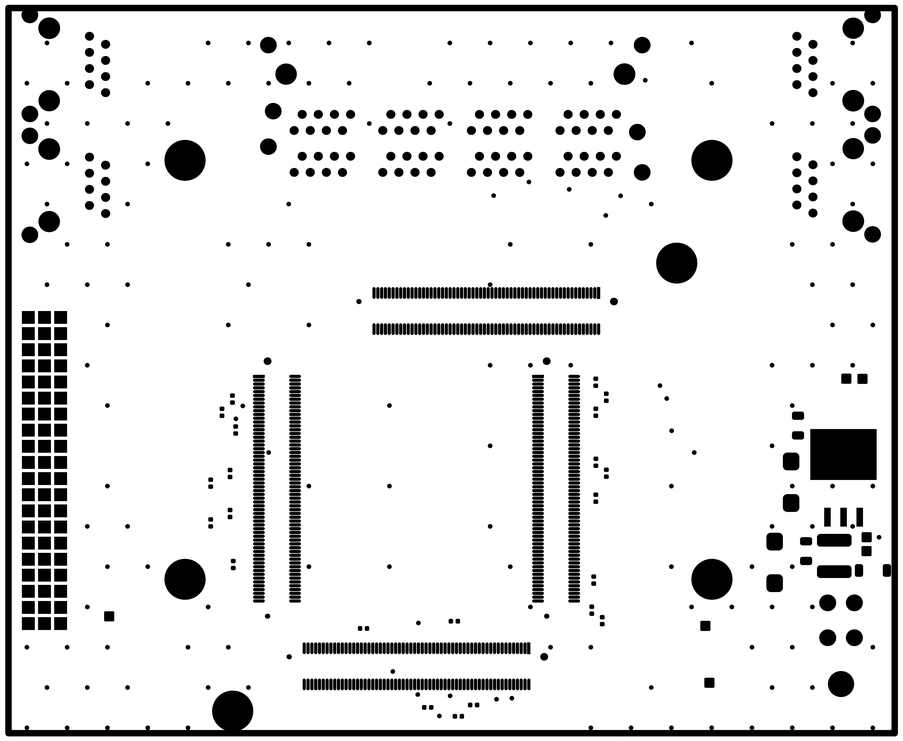

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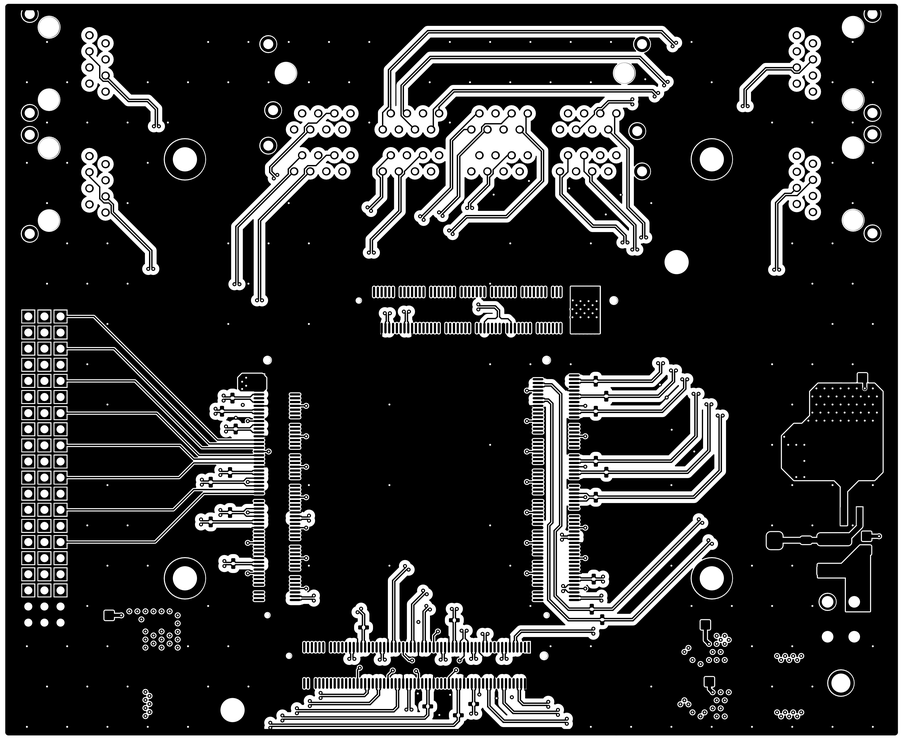
Drawn By: Khanh Le	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **SCROD_TO_RJ45_BOARD**	
Approved By: Gary S. Varner	Print Date: 4/30/2018	Signature:	Size: A3 H		
Title: Top Solder Mask GTS				**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**	



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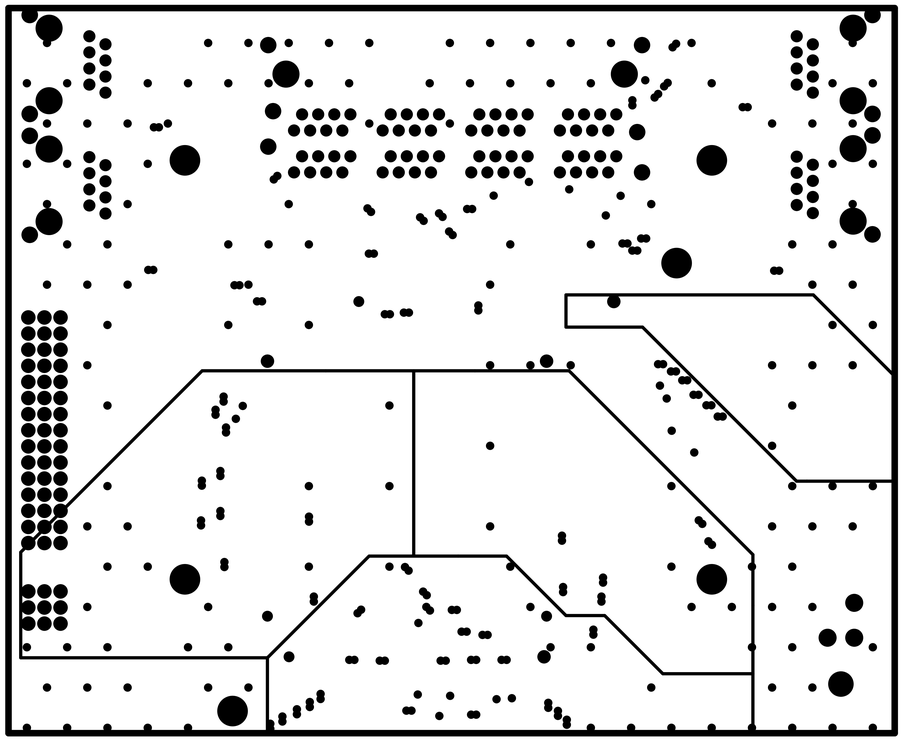
Approved By: Gary S. Varner	Print Date: 4/30/2018	Signature:	Size: A3 H	
Title: Top Layer 1 GTL				**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**



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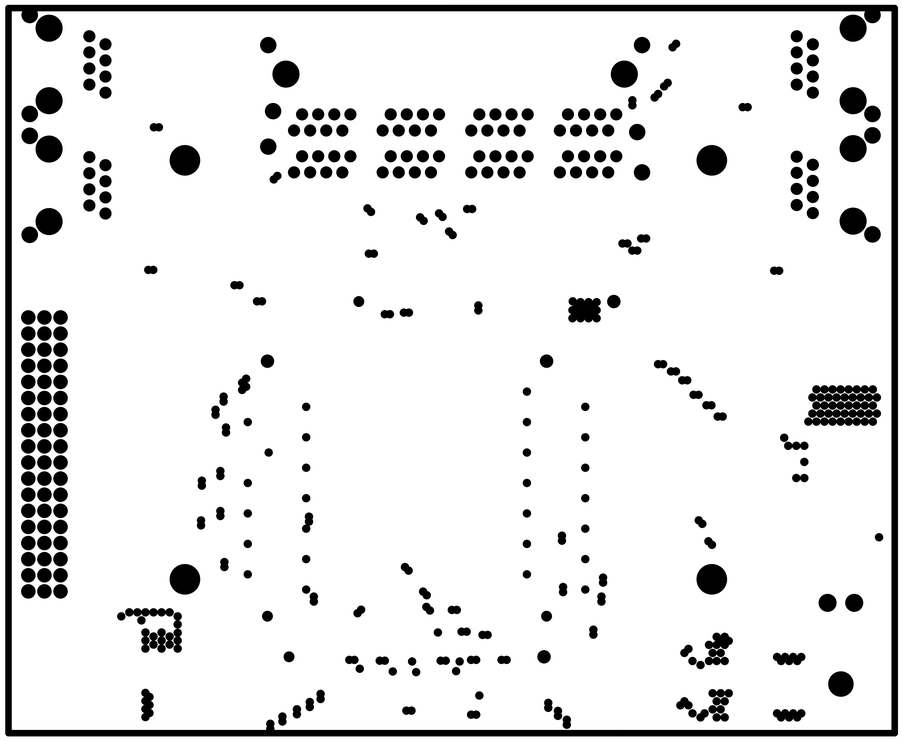
Approved By: Gary S. Varner	Print Date: 4/30/2018	Signature:	Size: A3 H	
Title: GND Plane Layer 2 GP1				**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**



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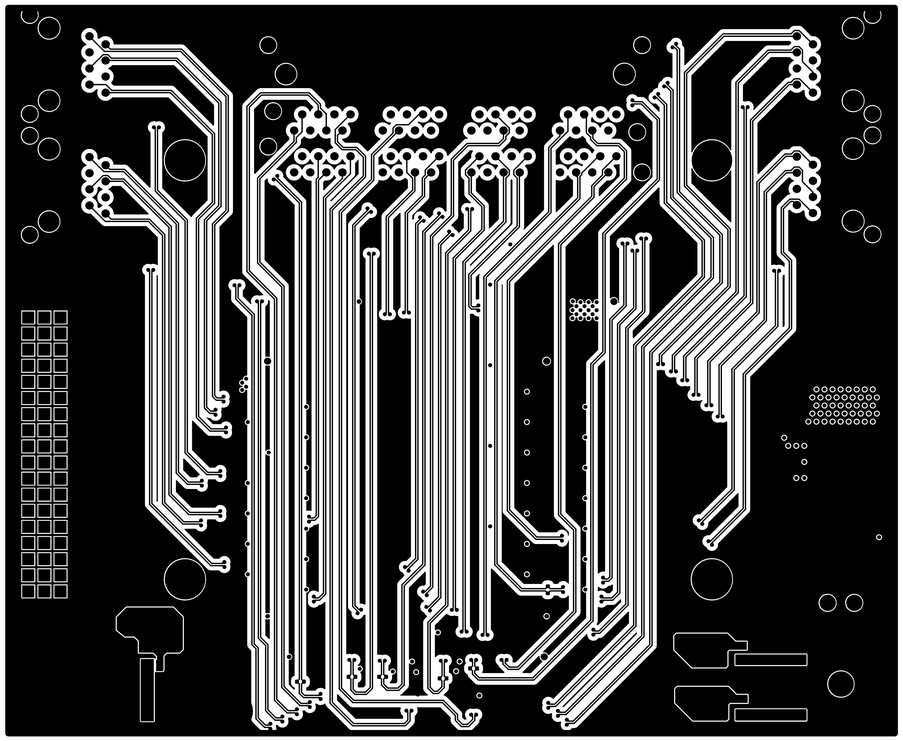
Approved By: Gary S. Varner	Print Date: 4/30/2018	Signature:	Size: A3 H	
Title: PWR Plane Layer 3 GP2				**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**



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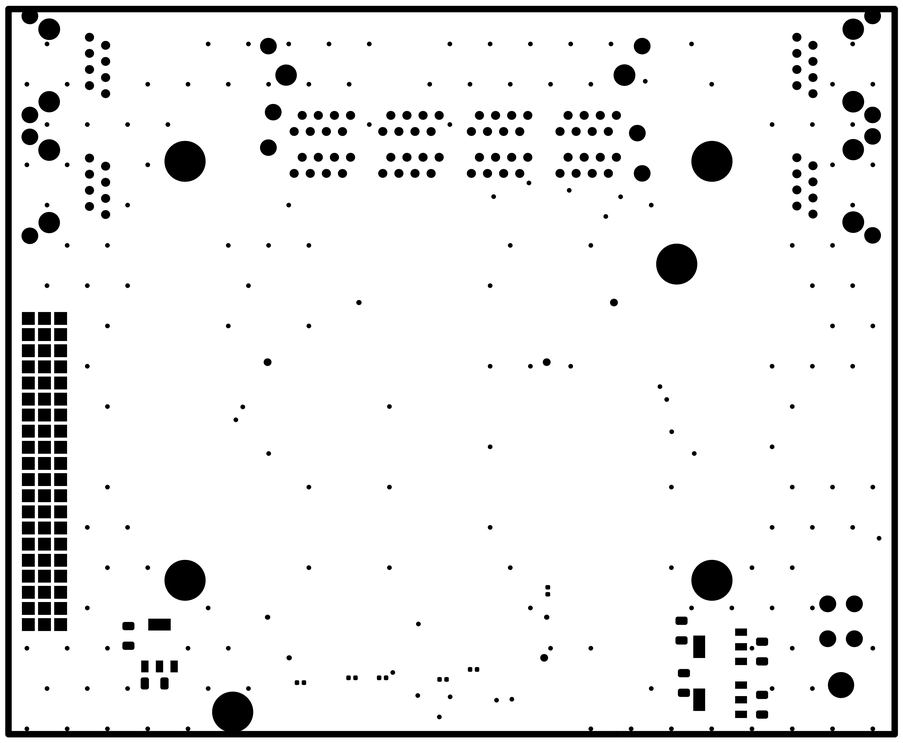
Approved By: Gary S. Varner	Print Date: 4/30/2018	Signature:	Size: A3 H	
Title: Bottom Layer 4 GBL				**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**



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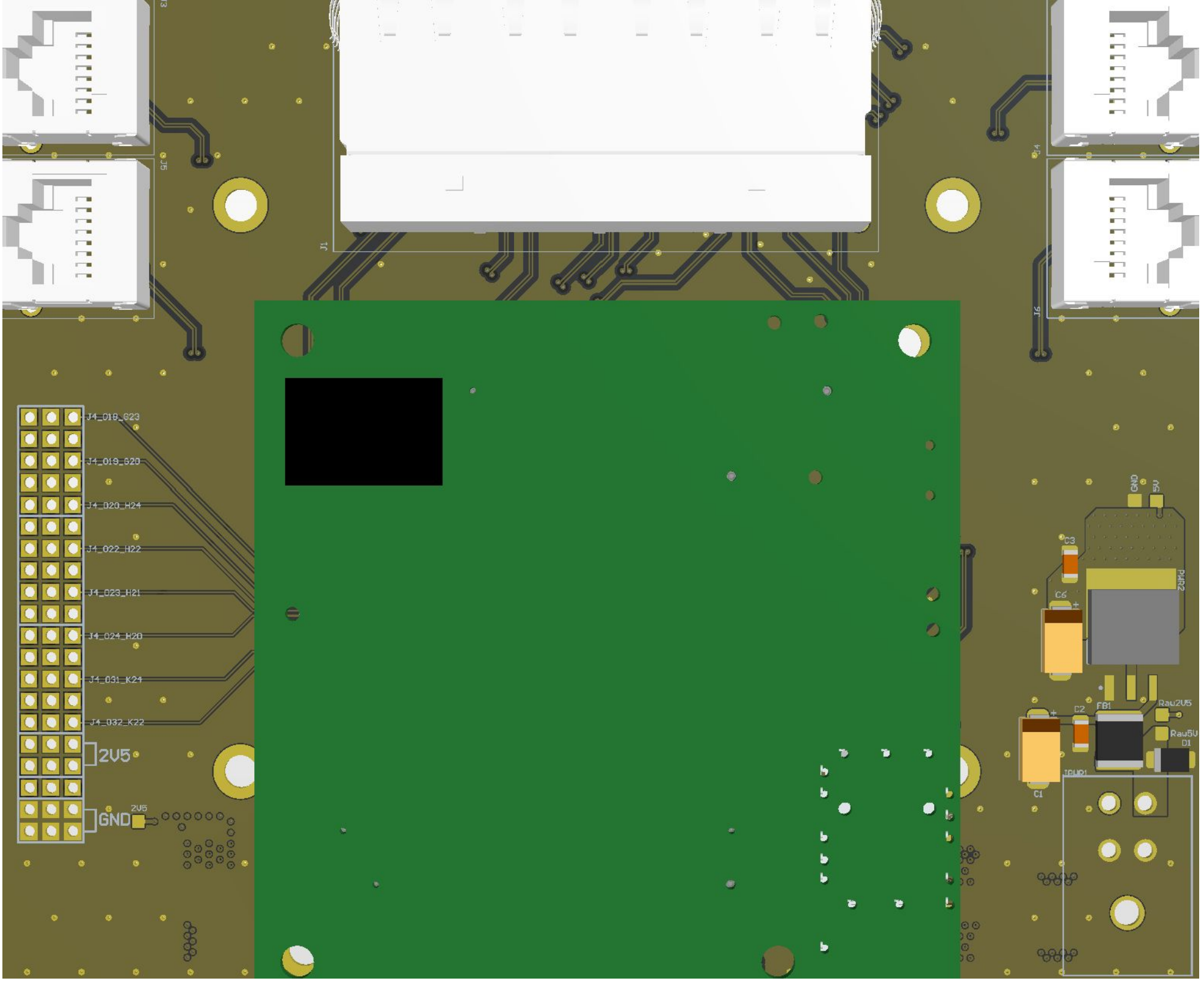
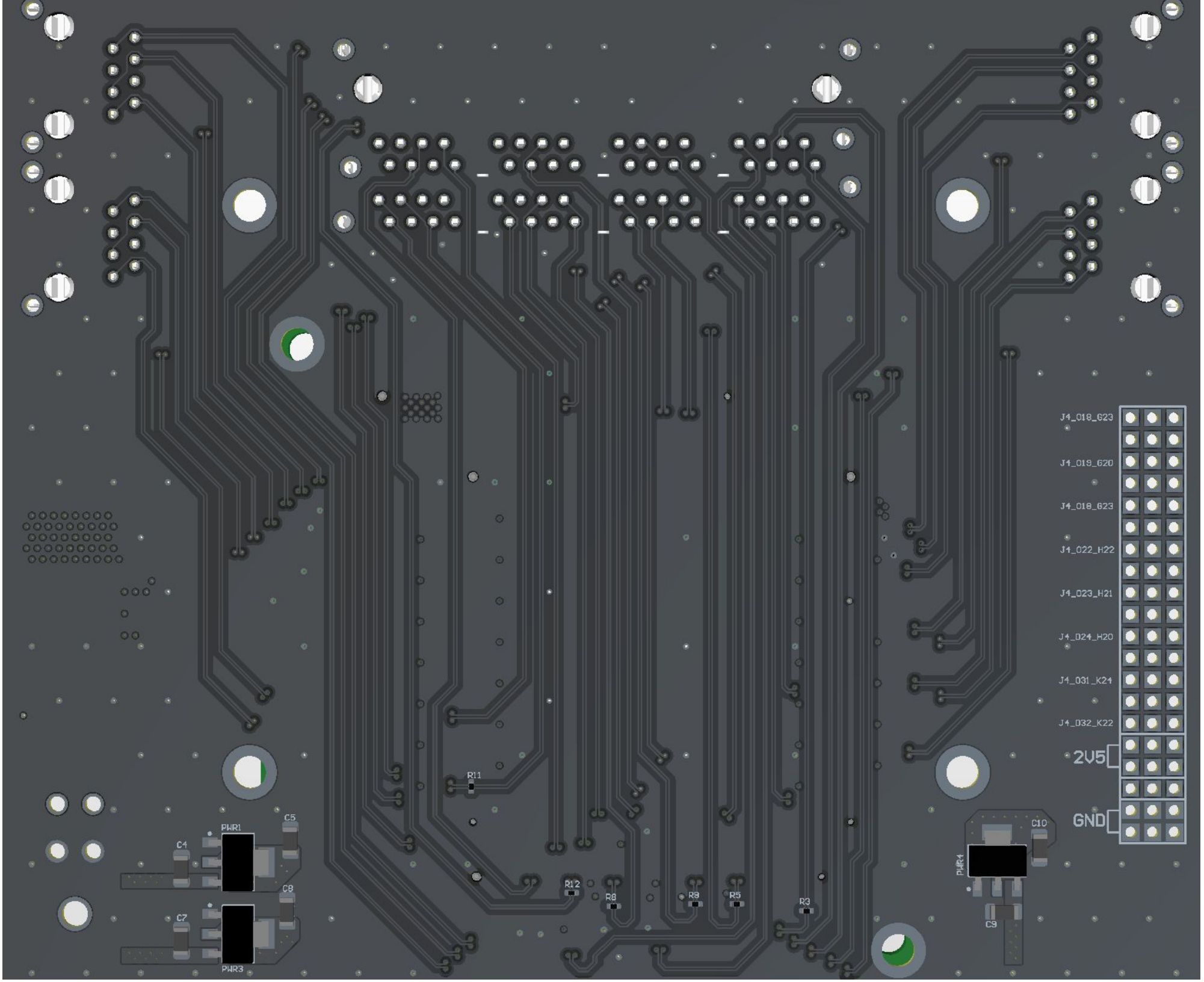
Title: Bottom Solder Mask GBS				**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**


J1
J3
J4
J5
J6
J4_018_G23
J4_019_G20
J4_020_H24
J4_022_H22
J4_023_H21
J4_024_H20
J4_031_K24
J4_032_K22
2V5
GND
2V5
GND
5V
C3
PWR2
C6
C2
FB1
Rau2V5
Rau5V
D1
C1


J4_018_G23
J4_019_G20
J4_018_G23
J4_022_H22
J4_023_H21
J4_024_H20
J4_031_K24
J4_032_K22
2V5
GND
R11
C5
PWR1
C4
C8
C7
PWR3
R12
R8
R9
R5
R3
C10
PWR4
C9