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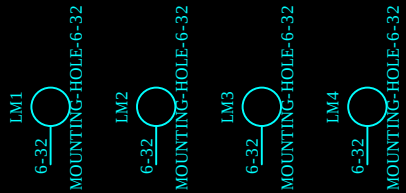
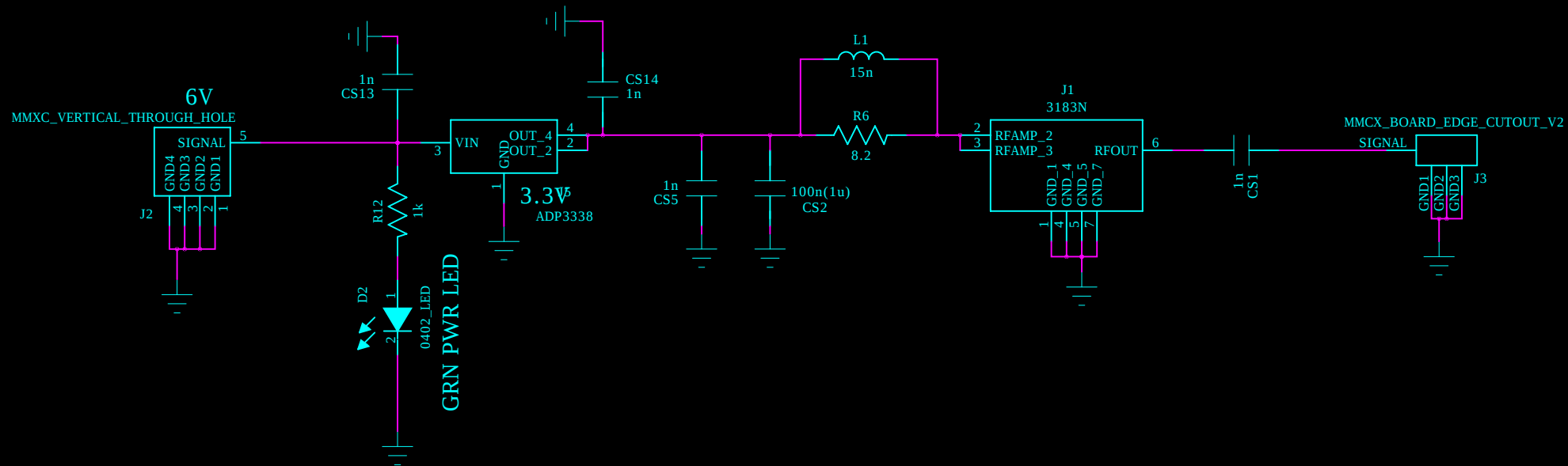
E

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institution:	<UH> <hepg> <idlab>
title:	<Title>
revision:	<Revision>
IDLAB design #:	<manifest>
circuit design:	<sch>
PCB design:	<pcb>
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sheet description:	RoF_Trans & Power
date last modified:	<modification date>