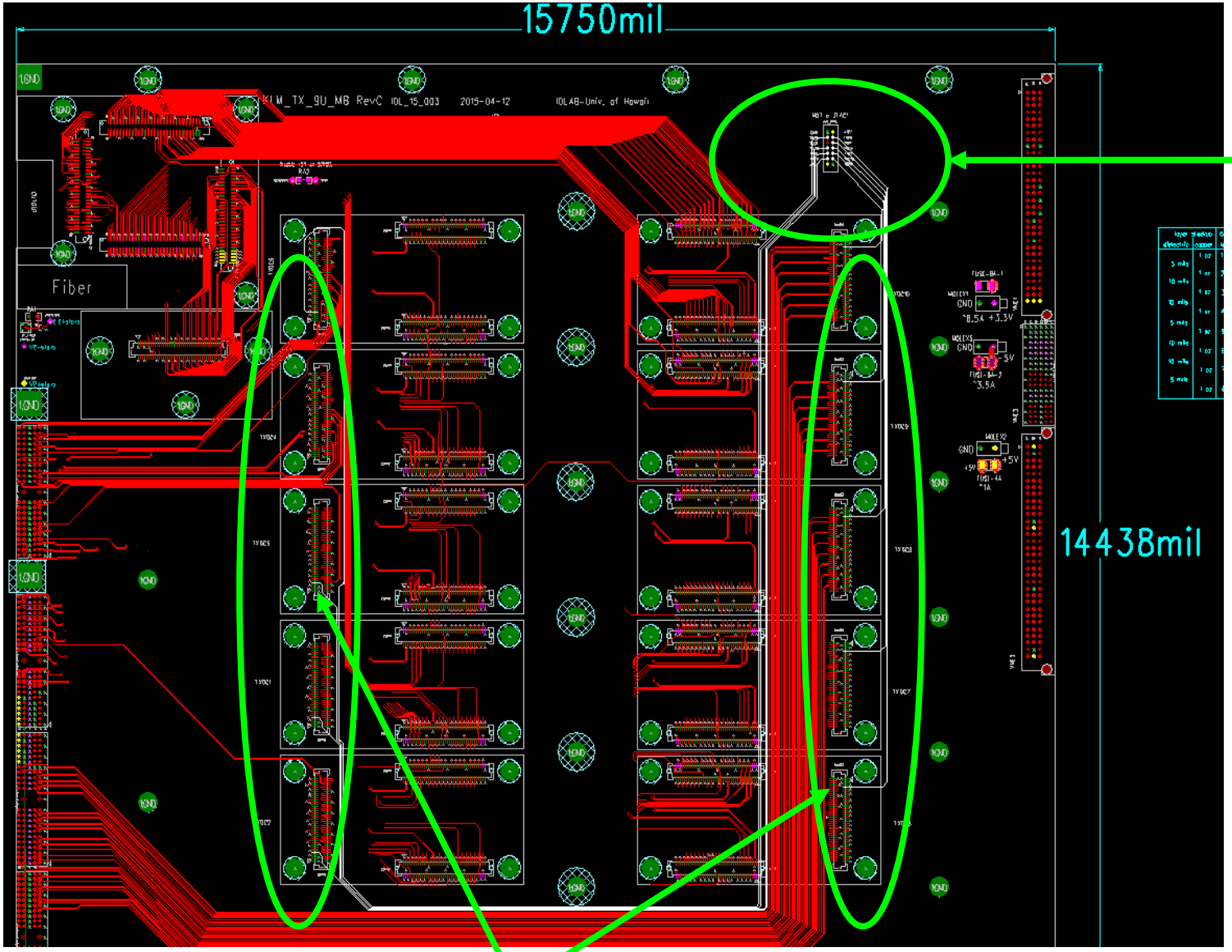
UNIVERSITY of HAWAI'I® MĀNOA

Instrumentation Development Laboratory

2015-05-18

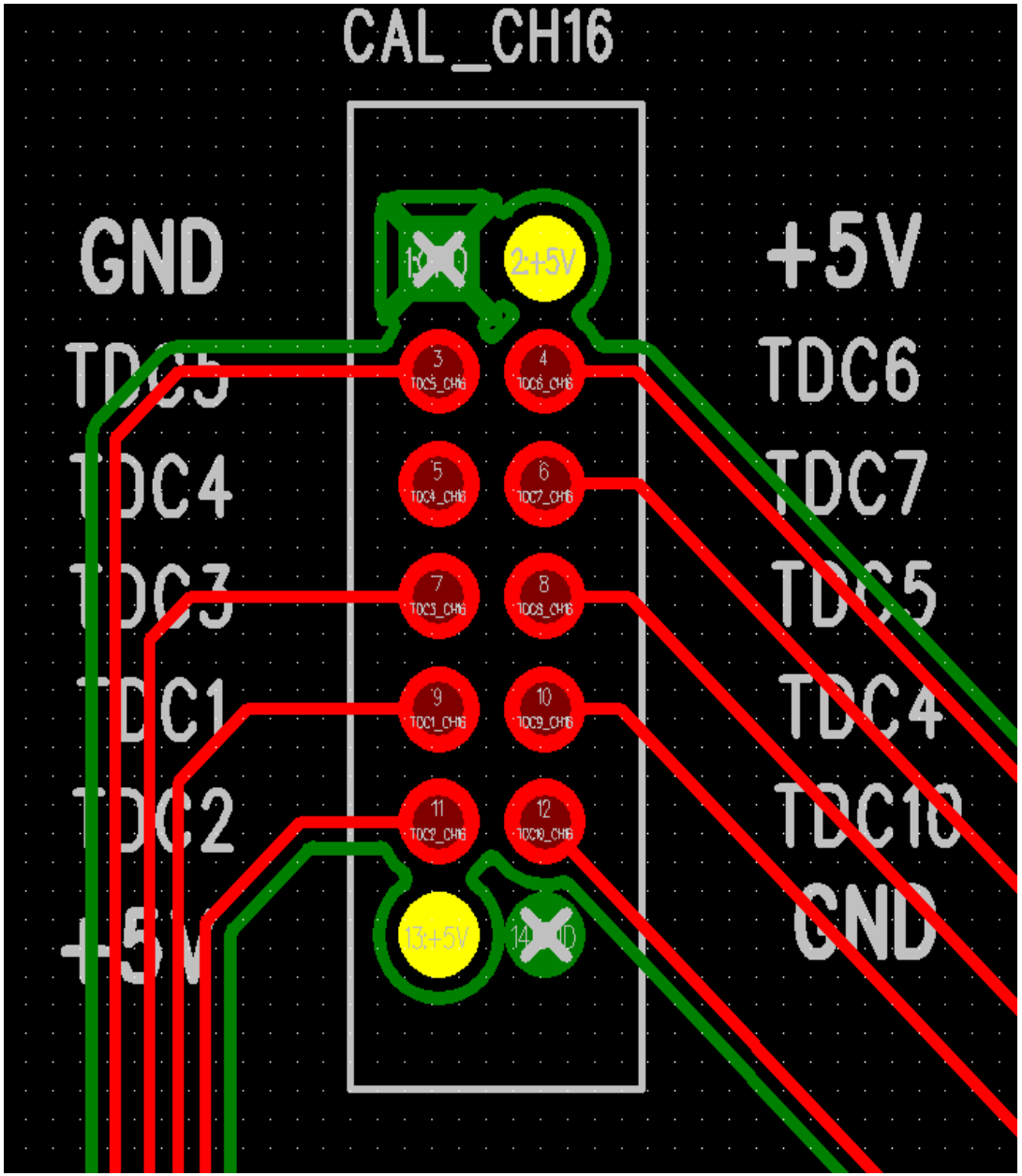
KLM Calibration Board

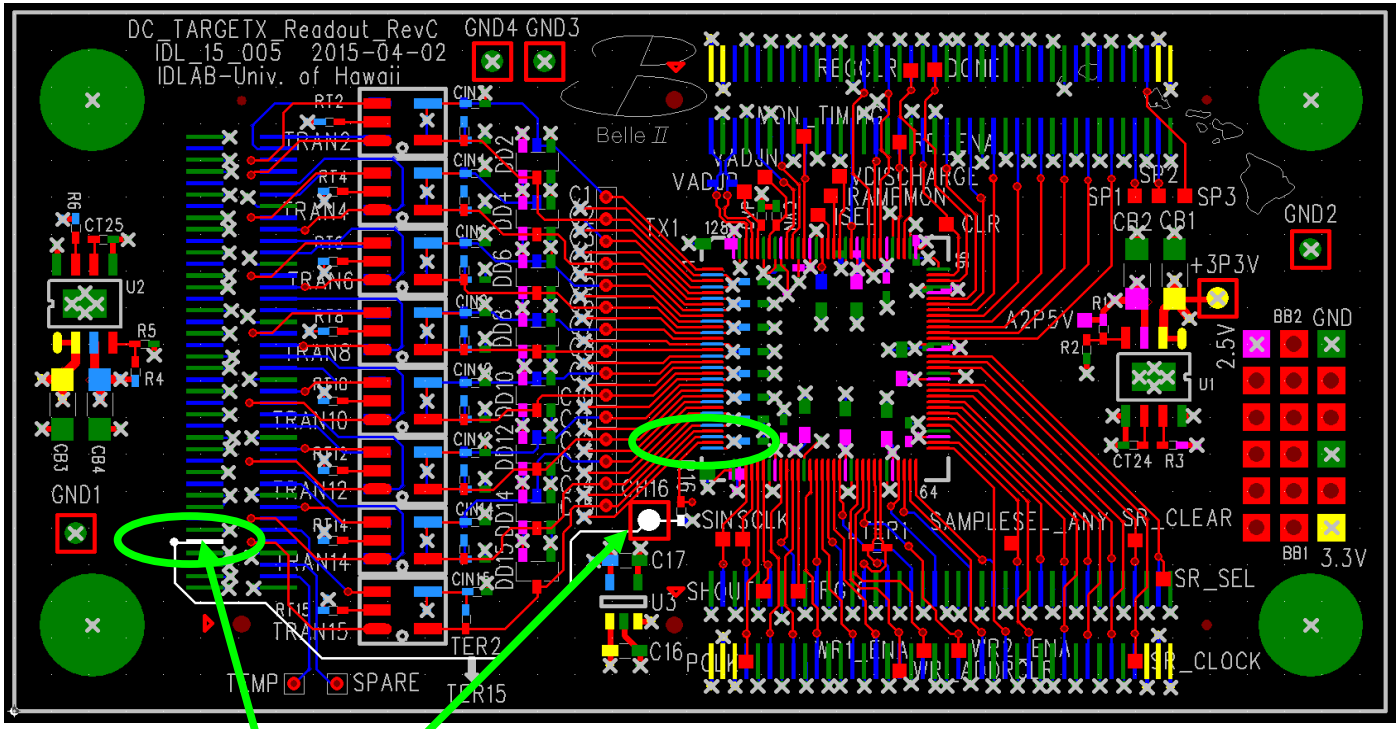
- overview
- Schematics
- layout
- Parts
- Cost



2mm
14-pin
Connector
For the
Calibration
Board

Traces to the “CH16” on each Daughtercard


CAL_CH16
GND
+5V
TDC6
TDC7
TDC5
TDC4
TDC1
TDC2
GND
2:+5V
3
TDC5_CH16
4
TDC6_CH16
5
TDC4_CH16
6
TDC7_CH16
7
TDC3_CH16
8
TDC8_CH16
9
TDC1_CH16
10
TDC9_CH16
11
TDC2_CH16
12
TDC10_CH16
13:+5V
14


DC_TARGETX_Readout_RevC
IDL_15_005 2015-04-02
IDLAB-Univ. of Hawaii
GND4 GND3
Belle II
CH16
SIN SCLK
SAMPLESEL_ANY
SR_CLEAR
SR_SEL
SR_CLOCK
TEMP
SPARE
TER2
TER15
GND1
GND2
+3P3V
A2P5V
2.5V
3.3V
U1
U2
U3
TX1

CH16

Saturn PCB Design, Inc. - PCB Toolkit V6.6 - www.saturnpcb.com

File | Program Function | Tools | Help | Contact Saturn PCB Design, Inc.

Fusing Current | Embedded Resistors | PPM Calculator | Crosstalk Calculator | Wavelength Calculator

Via Properties | Conductor Properties | Bandwidth & Max Conductor Length | Differential Pairs | Padstack Calculator | Mechanical Information

Conductor Spacing | **Conductor Impedance** | Conversion Data | Planar Inductors | PDN Impedance | Thermal

Conductor Impedance

Conductor Width (W): 17 mils

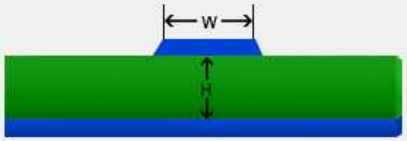
Conductor Height (H): 10 mils

W/H = 1.700

T/H = 0.140

Formula Restrictions:

0.1 < W/H < 3.0
T/H < 0.25



Zo: 50.3511 Ohms

Lo: 7.0280 nH/in

Co: 2.7721 pF/in

Tpd: 139.5804 ps/in

Options

Base Copper Weight
- 0.25oz
- 0.5oz
- 1oz
- 1.5oz
- 2oz
- 2.5oz
- 3oz
- 4oz
- 5oz

Plating Thickness
- Bare PCB
- 0.5oz
- 1oz
- 1.5oz
- 2oz
- 2.5oz
- 3oz

Passive Circuits
- Microstrip
- Microstrip Embed
- Stripline
- Stripline Asym
- Dual Stripline
- Coplanar Wave

Units
- Imperial
- Metric

Substrate Options

Material Selection: Custom

Er: 4.3 | Tg (°C): 130

Temp Rise (°C): 20

Temp in (°F) = 36.0

Ambient Temp (°C): 22

Temp in (°F) = 71.6

Print | Solve!

Information

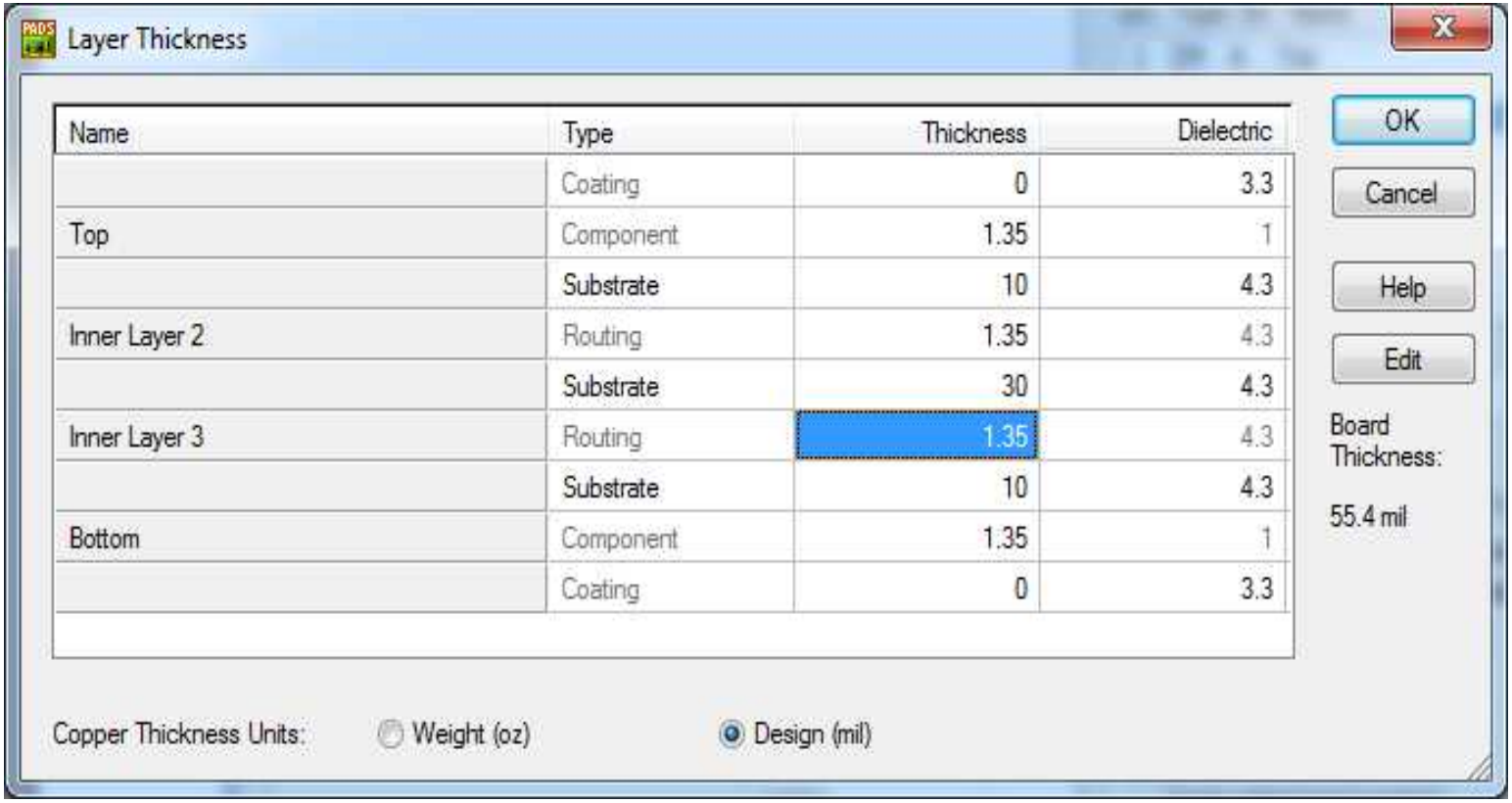
Total Copper Thickness
1.40 mils

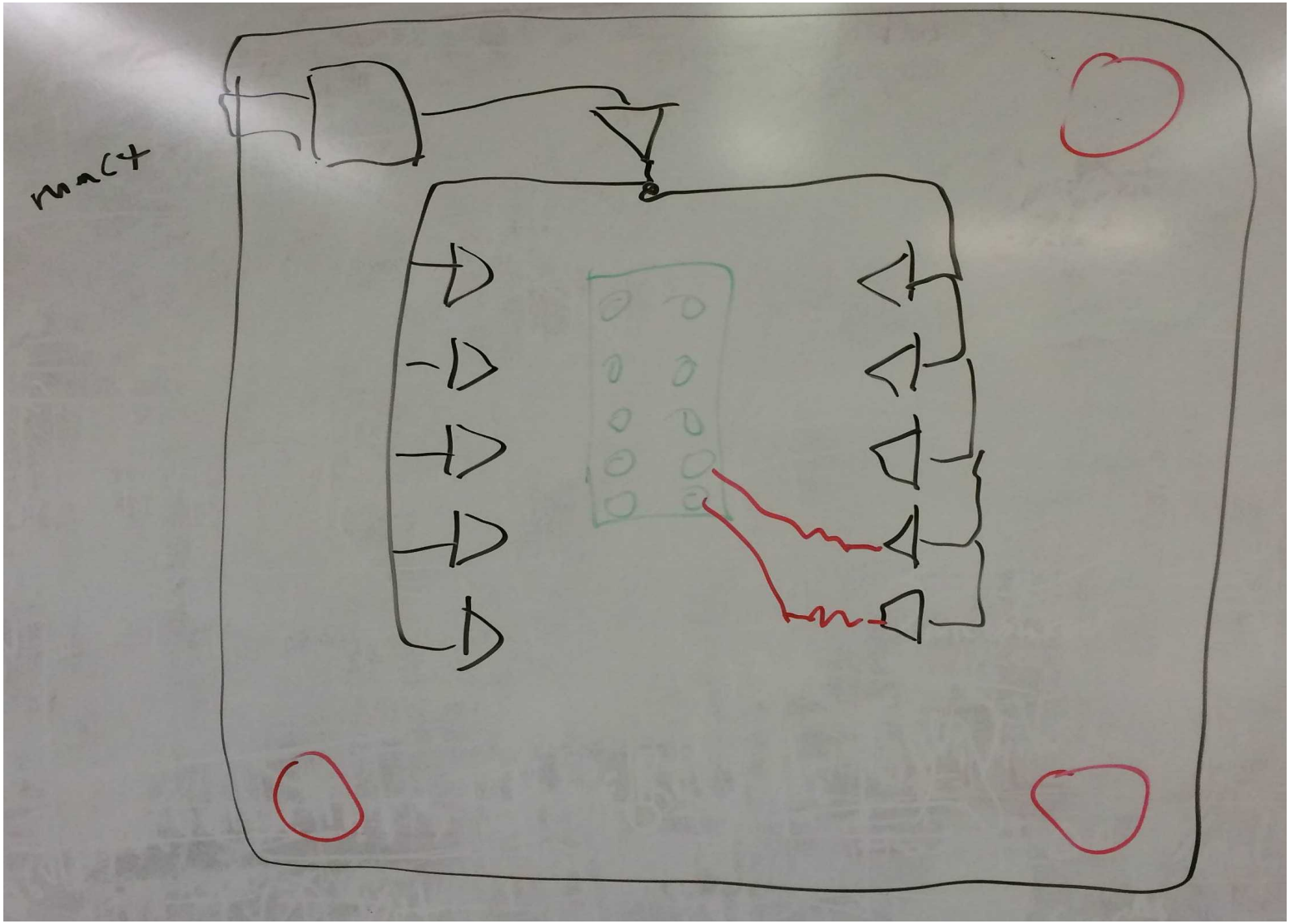
VIA Thermal Resistance
N/A

Conductor Temperature
Temp in (°C) = N/A
Temp in (°F) = N/A

VIA Voltage Drop
N/A

SATURN PCB DESIGN, INC
Turnkey Electronic Engineering Solutions


Layer Thickness
Name
Type
Thickness
Dielectric
Coating 0 3.3
Top Component 1.35 1
Substrate 10 4.3
Inner Layer 2 Routing 1.35 4.3
Substrate 30 4.3
Inner Layer 3 Routing 1.35 4.3
Substrate 10 4.3
Bottom Component 1.35 1
Coating 0 3.3
OK
Cancel
Help
Edit
Board Thickness:
55.4 mil
Copper Thickness Units:
Weight (oz)
Design (mil)



Parts

LMH6559MF/NOPB : IC OPAMP BUFFER 1.75GHZ SOT23-5
http://www.digikey.com/product-search/en?x=0&y=0&lang=en&site=us&keywords=lmh6559Mf%2Fnopbct-nd

http://www.ti.com/lit/ds/symlink/lmh6559.pdf

KLM - LMH6559_DC Linearity Test [.docx] – Peter Orel

2015-5-15 Gary's email:

I don't see DC transfer curve as an important measurement to perform on production boards.
The intrinsic linearity (or measurements from sine wave checks) is good enough.

If we need to do that on one or 2 boards, we can remove their 50ohm loads,
in which case this curve will be acceptable, I believe.

I suggest moving ahead with this part. (it has a standard footprint, as I understand it,
so if we desperately need another part, options exist)

Email train summary

By the way - what is the bandwidth / gain flatness expected here? You should have an idea about that before trying to decide on the fanout circuit. Probably up to some frequency limited by the buffer input capacitance loading, you can surely have decent performance from an input buffer driving a _short_ line with termination at the end and 10 output buffers snooping the line. There'll be a bunch of reflections there in principle, but they probably don't matter as long as that line is short enough, which is probably the case. Of course, more of a tree structure of small fanout stages is better for bandwidth probably, but I'm not sure it is necessary here.

- Gerard

This the part plenty of which we have in the lab:
http://www.ti.com/lit/ds/symlink/lmh6559.pdf
The gain is not that high, but the small signal BW goes up to ~700 MHz with a 0.1dB flatness up to 100 MHz.

The proposed testing frequency will be up to 40 MHz. The two distinct tests will be:
1) Sinewave test where the The required input DC level at the chip will be ~1.25 V
2) DC scan test for linearity where the DC will be swept from 0 to 2.5V (or close to these limits).

- Isar

You can then have the extra two outputs going to MMCX connectors (both so you can check what the output looks like on a scope / do S12 measurements, but also so you could potentially daisy-chain these boards).

- Matt

Specifically, this is a card on the Motherboard, to do the 10 way fanout to the Daughtercards.

iTOP has a requirement for in-situ functionality testing, in particular BPM phase measurement, since maintaining precision event timing is needed. KLM has no such requirement, so this would be complete overkill. Given that funds are tight, we had no such plans to do such calibration in deployed units, but rather only use a couple of these as part of production testing.

Nevertheless, if we could afford, it would be a nice sanity check. However that is distinct from the fan-out on the Motherboard, which is what this card represents.

Since cabling costs would dominate for driving 144 Motherboards, it might make sense to have a single output per group of 7/8 Motherboards and do an 8-way split at the crate. If decide to go this route -- and such scope is not in the baseline.

-Gary

Email train summary continuted

Output range of the circuit as drawn is actually 0.5V to 0.85V.

So yes you have to do something different, such as use only series termination on the internal lines (this should be fine at 40MHz!), or use a Thevinin termination there. Again I do not think omitting the output series termination is a good idea.

I suggest fix the schematic, before fabricating the board, so that you can see that the plan is sound.

Since the amp output is low-impedance, if placed close by you can drive two 50 Ohm lines with two series termination resistors, you don't need the Y splitter. Isolation between the lines is much better that way too, as a by-product. But, this isn't important here, and attenuation is the same either way. So no problem to keep it as is, I am just mentioning it.

– Gerard