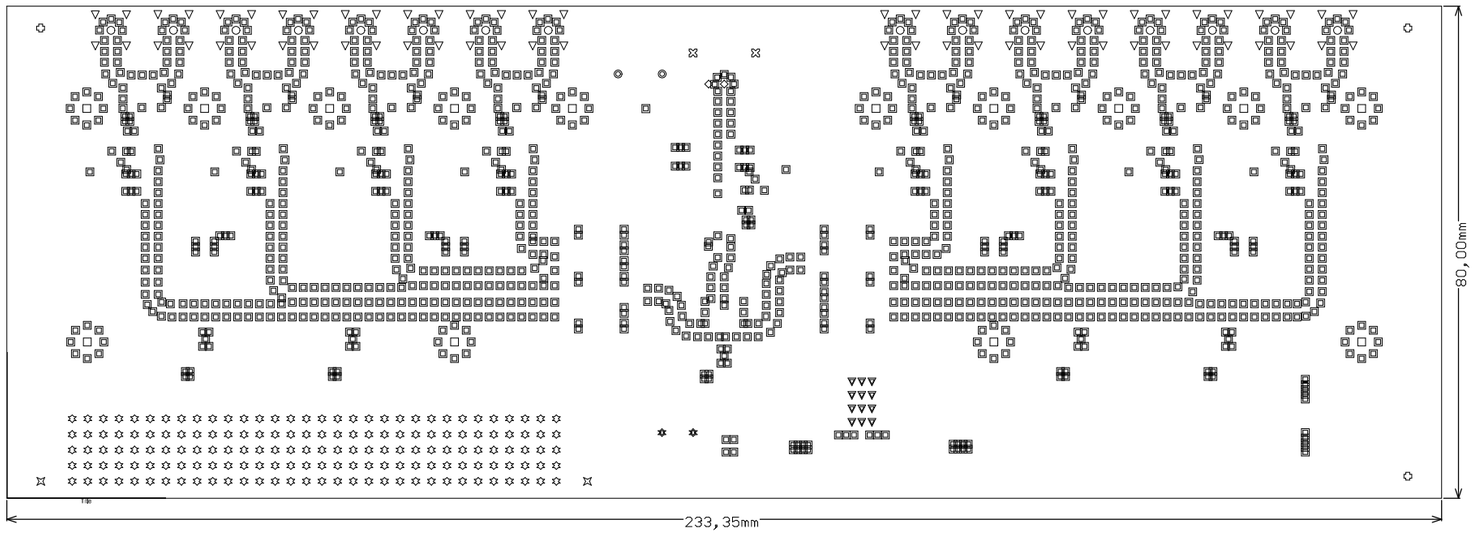


Notes:

1. Board shall be fabricated - performace class II as per IPC-6011 and IPC6012
2. PCB manufacturer logo, P/N, revision and/or date code of manufacturing
   shall be printed in top solder mask (not over pcb traces, allowed over copper plane).
   The date code shall be in the format: "WWYY" where WW=week and YY= year, max height 0.15 inches
3. Silkscreen printed on both sides
4. Material: high temperature FR4 class epoxy glass rated UL94V-0. UL symbol and rating shall be marked farside
   35um copper for external layers and 18um for all internal layers
   Must be RoHS compliant and survive a lead-free assembly max reflow of 260 deg C (5 passes)
   Td rating: >340 deg C
   Tg = 150 deg C (min)
5. Solder mask: SMOBC per IPC-SM-840C, class T must be Rohs compliant, 0.001" max measured over bare copper plating,
   must clear all lands as indicated on gerber solder mask layers, color= GREEN
6. Finish: electro-less nickel immersion gold (ENIG), 0.05-0.125um Au over 3-6um Ni - over bare copper only
7. Solderability test: Category 2 of J-STD-003
8. Finished boards shall not have nicks, scratches, voids, exposed copper, poor plating or misdrilled holes
9. All holes sizes are after plating
10. PCB manufacturer may add copper thieving as needed to improve manufacturability,
    thieving to be 0.030" round pads at 0.050" spacing.
    Thieving will have a minimum of 0.100" clearance from existing copper and should not be placed under surface mounted devices
11. PCB manufacturer may use tear drops to improve annular rings as long as DRC rules are followed
12. All via connections to power and ground planes are solid
13. All unconnected pads on inner signal layers are removed
14. All finished boards are to be 100% electrically tested
15. Unless otherwise indicated, all linear toleracnes shall be XX.X +/-0.2mm and XX.XX +/- 0.1mm
16. Gerber file GM1 shows board outline (milling line)
17. Table 1 shows Layer stack details

Additional notes:

A1. Finished board thickness = 1.6mm +/- 10%; measured over top/bottom copper and solder mask

Table 2: NC Drill Details for IDL_15_22 Rev.A

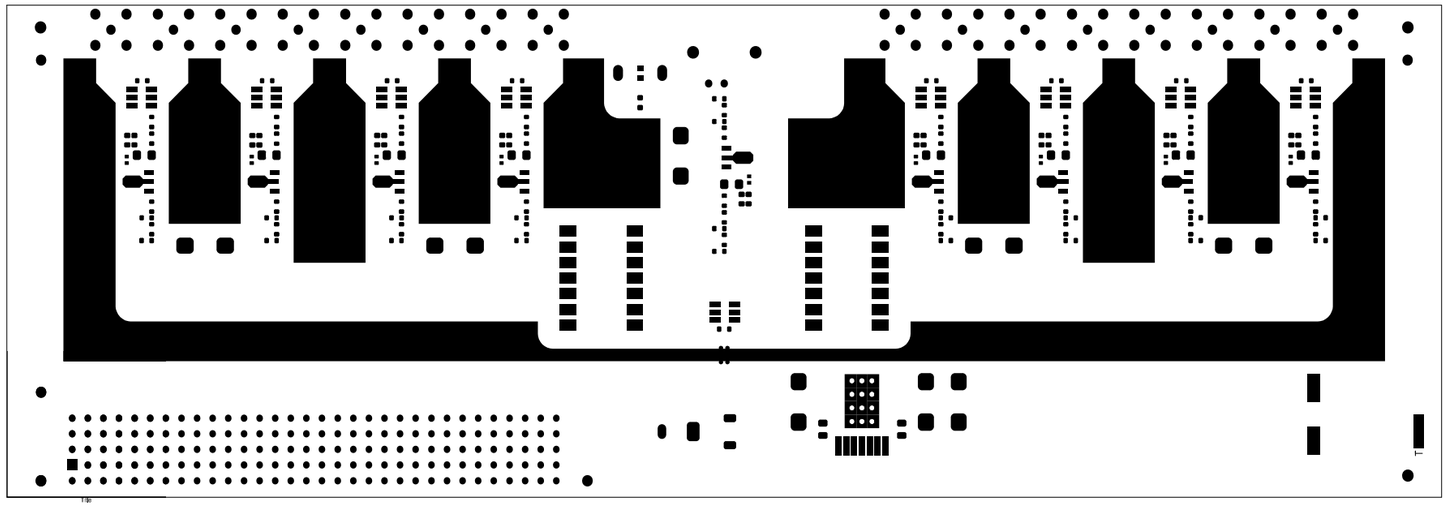
Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
◇	2	0,900mm (35,43mil)	PTH	Round
✡	2	1,400mm (55,12mil)	PTH	Round
⊠	2	2,000mm (78,74mil)	PTH	Round
◎	2	2,000mm (78,74mil)	NPTH	Slot
⊠	2	2,800mm (110,24mil)	NPTH	Round
✣	3	2,700mm (106,30mil)	NPTH	Round
▽	12	0,400mm (15,75mil)	PTH	Round
□	14	3,683mm (145,00mil)	PTH	Round
○	16	1,200mm (47,24mil)	PTH	Round
▽	64	1,600mm (62,99mil)	PTH	Round
✡	160	1,000mm (39,37mil)	PTH	Round
▣	1241	0,300mm (11,81mil)	PTH	Round
	1520 Total			

Slot definitions : **Rout Path Length** = Calculated from tool start centre position to tool end centre position.
Hole Length = Rout Path Length + Tool Size = Slot length as defined in the PCB layout

Table 1a: Layer Stack Details for IDL_15_22 Rev.A (Imperial Units)

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,40mil	3,5	
3	Top Layer - SIG1	Copper	1,38mil		
4	Dielectric 1	FR-4	15,00mil	4,65	
5	Layer 2 - GND1	Copper	0,71mil		
6	Dielectric 3	FR-4	27,00mil	4,65	
7	Layer 3 - SIG2	Copper	0,71mil		
8	Dielectric 6	FR-4	15,00mil	4,65	
9	Bottom Layer - SIG4	Copper	1,38mil		
10	Bottom Solder	Solder Resist	0,40mil	3,5	
11	Bottom Overlay				

Designer: Peter Orel	Revision: .Version	File: IDL_15_22_A.PcbDoc	Sheet 1 of 1	Code: **IDL_15_22**
Drawn By: Peter Orel	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **ITOP_CALIB_FN1**
Approved By: Gary S. Varner	Print Date: 1. okt 2015	Signature:	Size: A3 H	**University of Hawaii at Manoa**
Title: Drill Drawing and Dimensions (GD1)				**High Energy Physics Group**
				Instrumentation Development Laboratory



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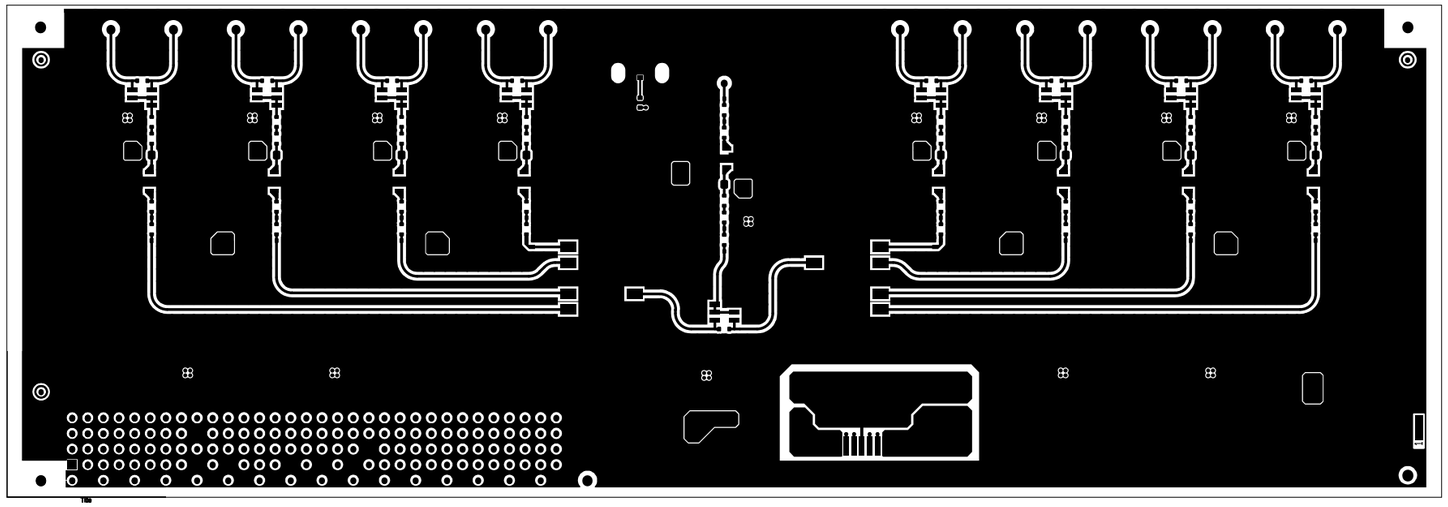
Drawn By: Peter Orel	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **ITOP_CALIB_FN1**
Approved By: Gary S. Varner	Print Date: 1. okt 2015	Signature:	Size: A3 H	**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**
Title: Top Solder Mask (GTS)				



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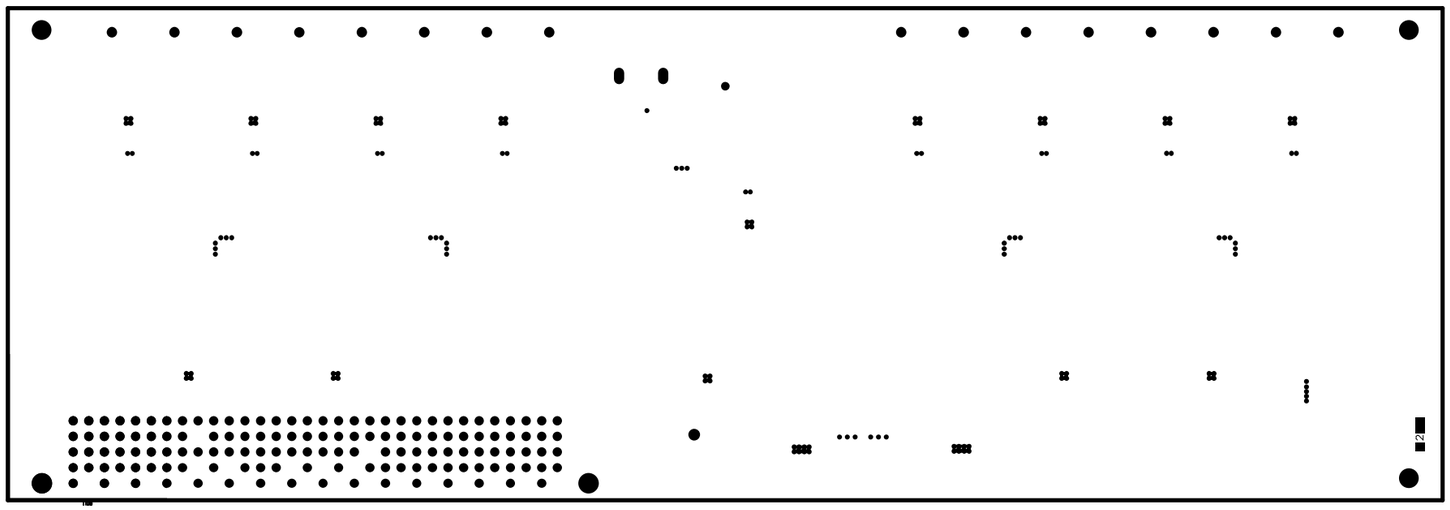
Drawn By: Peter Orel	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **ITOP_CALIB_FN1**
Approved By: Gary S. Varner	Print Date: 1. okt 2015	Signature:	Size: A3 H	**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**
Title: Top Layer- SIG1 (GTL)				



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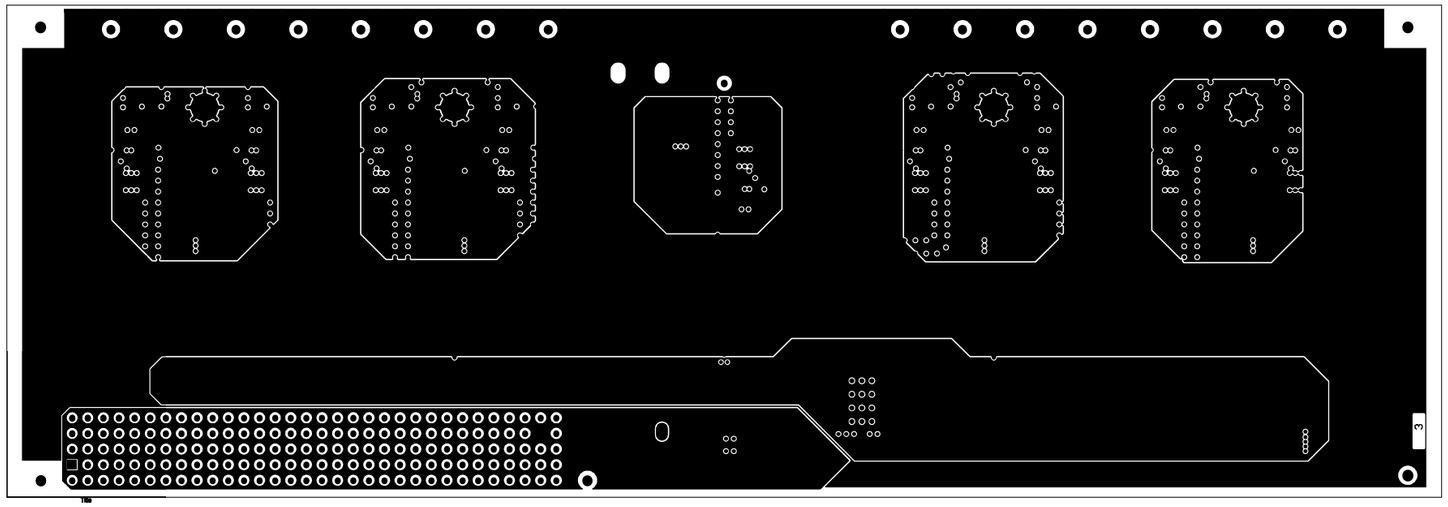
Drawn By: Peter Orel	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **ITOP_CALIB_FN1**
Approved By: Gary S. Varner	Print Date: 1. okt 2015	Signature:	Size: A3 H	**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**
Title: Layer 2 - GND1 (GP1)				



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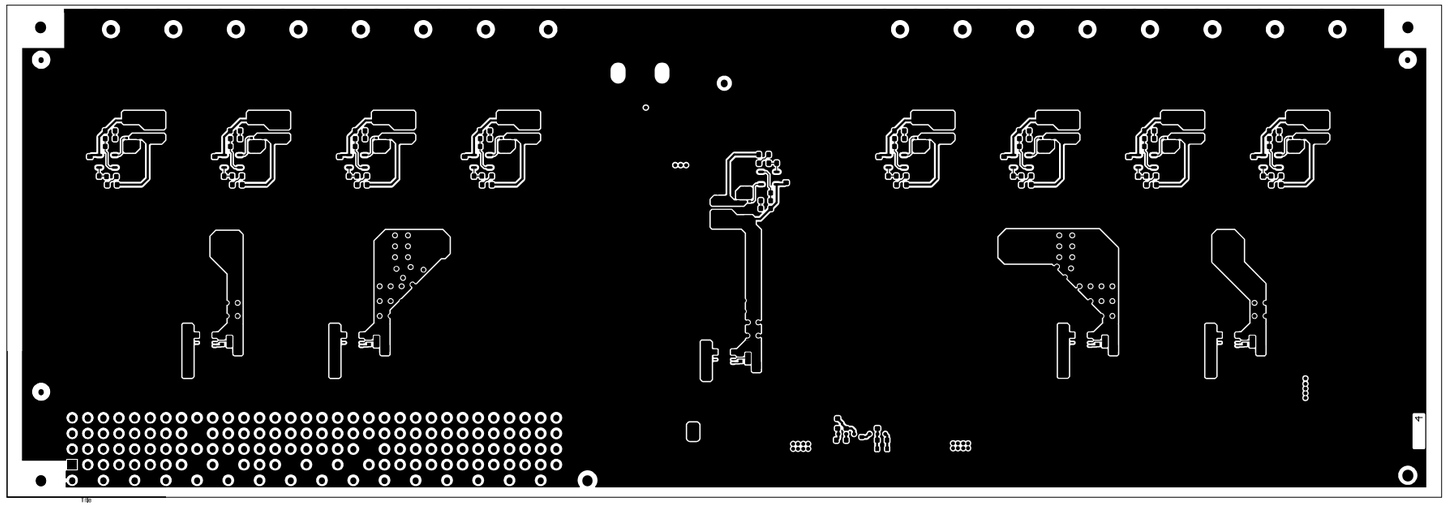
Approved By: Gary S. Varner	Print Date: 1. okt 2015	Signature:	Size: A3 H	**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**
Title: Layer 3 - SIG2 (G1)				



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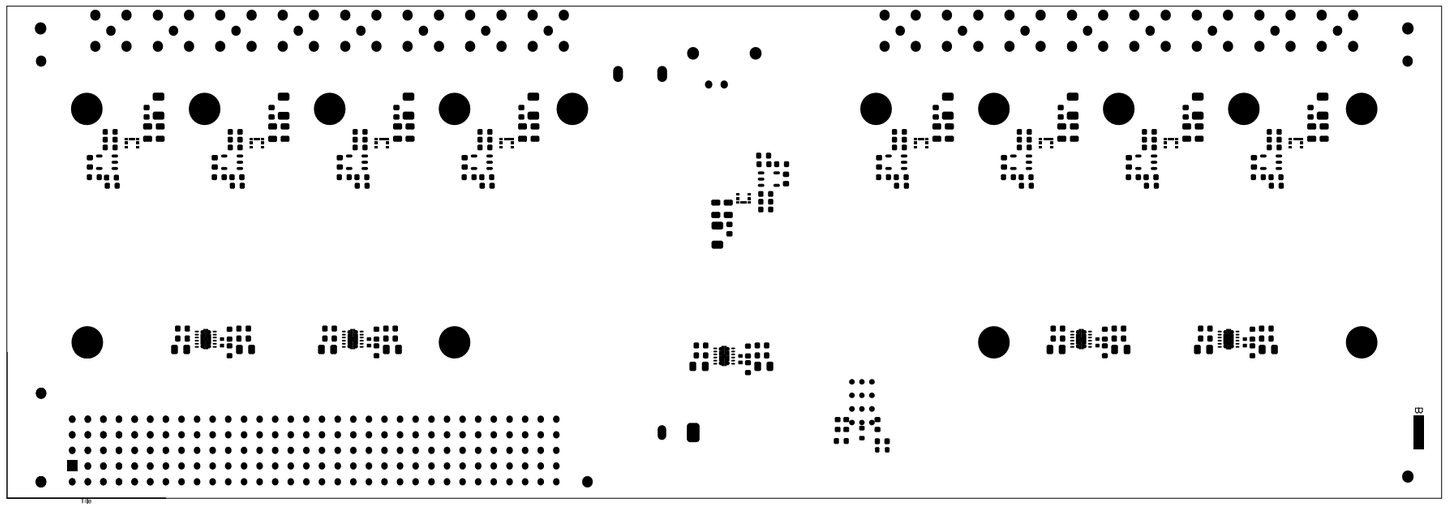
Approved By: Gary S. Varner	Print Date: 1. okt 2015	Signature:	Size: A3 H	**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**
Title: Bottom Layer - SIG3 (GBL)				



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Drawn By: Peter Orel	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **ITOP_CALIB_FN1**
Approved By: Gary S. Varner	Print Date: 1. okt 2015	Signature:	Size: A3 H	**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**
Title: Bottom Solder Mask (GBS)				