2014-11-11 notes:

Removed the 16-bit DAC,
(2) I2C Shift Register GPIO's
and associated PU resistors
PCA9534A GPIO pin 11 left floating

Free CLR nets: J4_105_W25

Free DAC nets: J3.21 & J7.71
J3.23 & J7.73

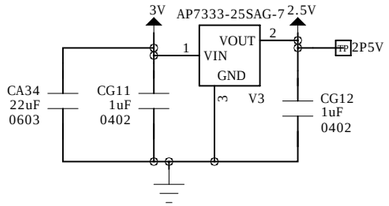
Free I2C SR nets: J2.3 & J6.53
J2.27 & J6.77

Free nets from grounding pins 67 & 126:

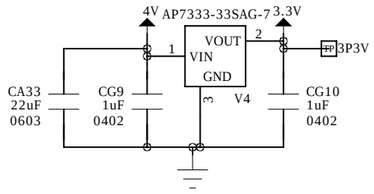
Repurposed for GCC_CKLP I/P
J2_023_AA12.J3_076_T9 J2.23 & J6.73
J2_049_Y21 J2.49 & J6.99
J3_076_T9.J2_023_AA12 J3.76 & J7.26
J4_078_L24 J4.78 & J8.18

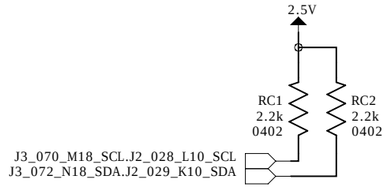
Repurposed for SSTin I/P
J2_004_W8 J2.4 & J6.54
J1_028_AE2 J1.28 & J5.88
J1_058_AC3 J1.58 & J5.118
J3_040_N19 J3.40 & J7.90

provides 2.5V for multiplexers, i2c eeprom, i2c GPIOs and i2c temperature sensors



provides 3.3V for LTC2637 DACs

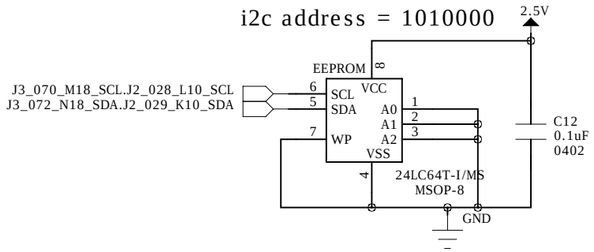




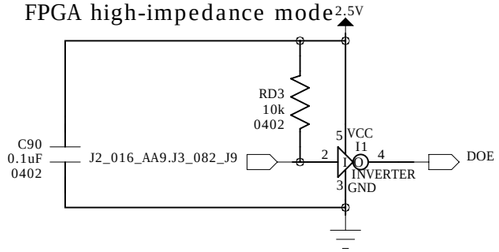
pullups for i2c for eeprom, GPIO and temperature sensors

the pullup is so all the registers are cleared (even when FPGA not present)

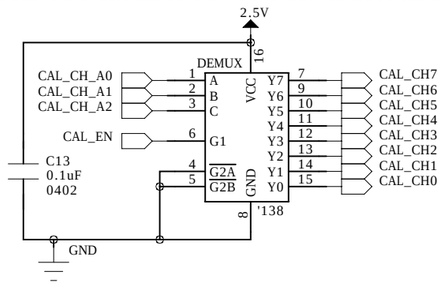
i2c eeprom for carrier identification
i2c address = 1010000

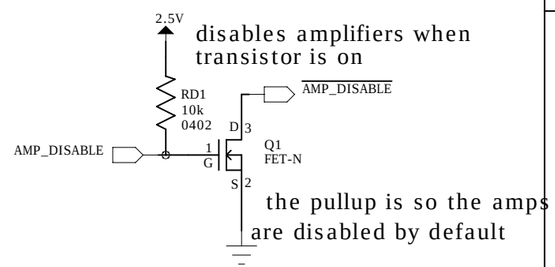


disables DOE by default
ensures all four DOE (active high) signals are not driven during FPGA high-impedance mode

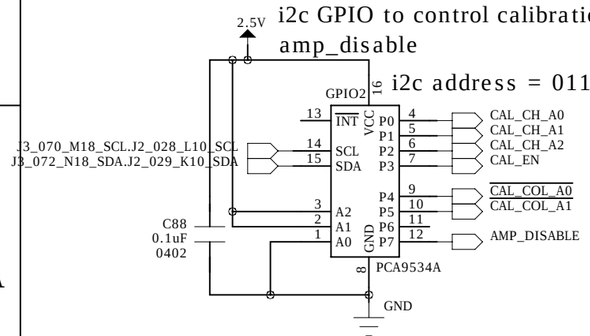


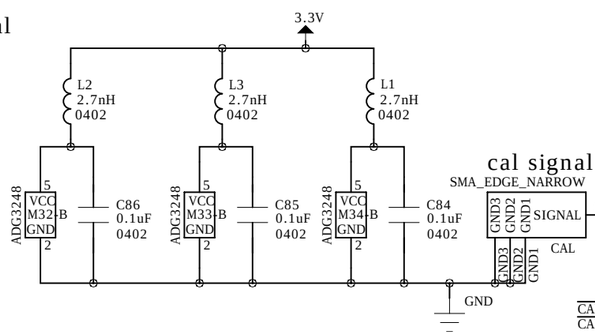
selects one channel out of 8 for calibration signal



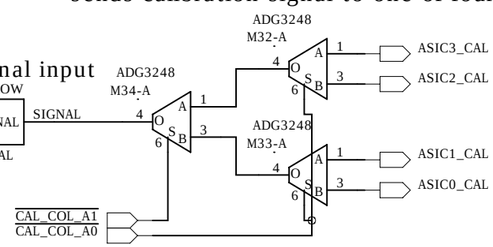


i2c GPIO to control calibration signal amp_disable
i2c address = 0111110

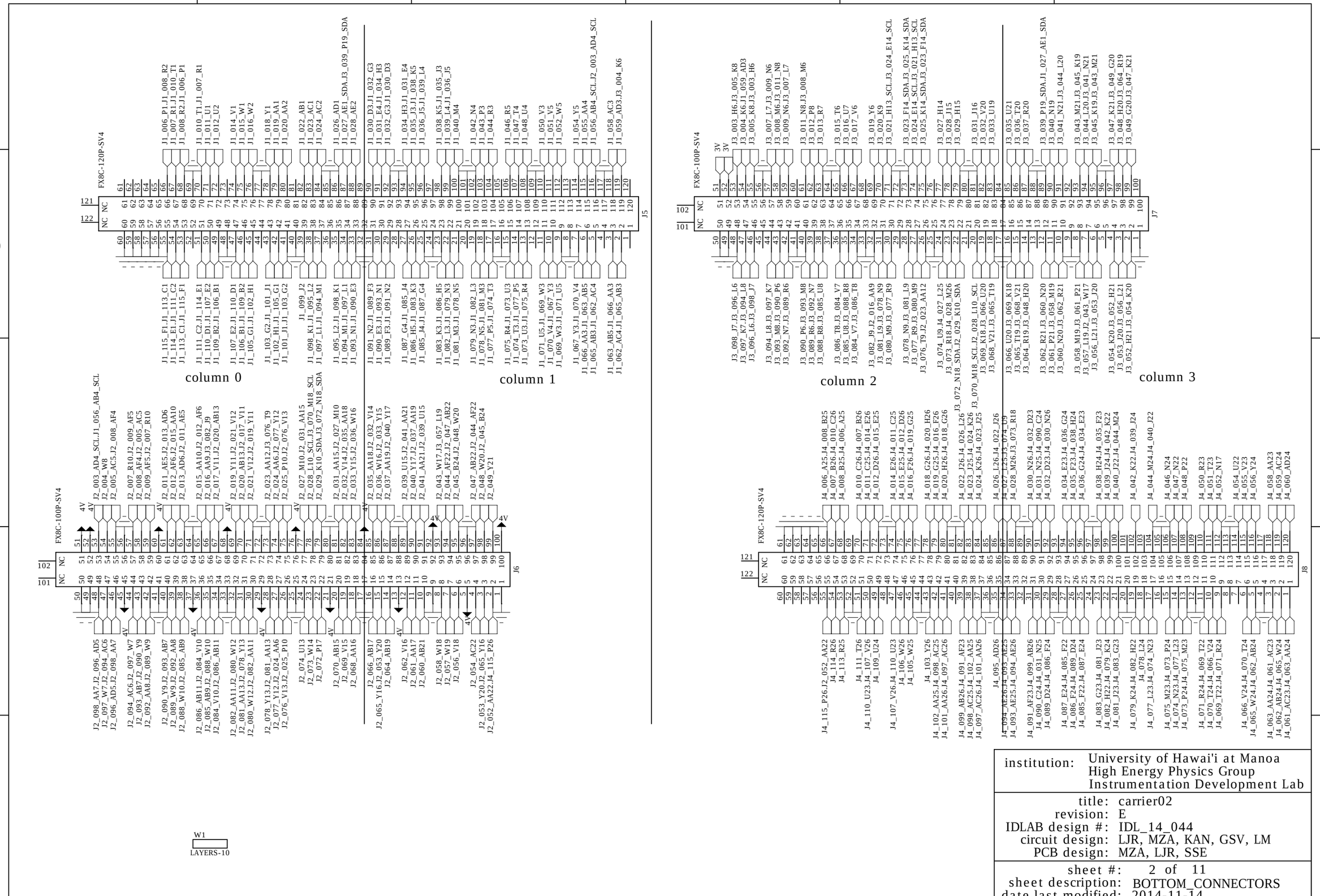




sends calibration signal to one of four ASICs



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier02
revision:	E
IDLAB design #:	IDL_14_044
circuit design:	LJR, MZA, KAN, GSV, LM
PCB design:	MZA, LJR, SSE
sheet #:	1 of 11
sheet description:	POWER_CAL_I2C_FET_DAC_GPIO_EPROM
date last modified:	2014-11-14



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier02
revision:	E
IDLAB design #:	IDL_14_044
circuit design:	LJR, MZA, KAN, GSV, LM
PCB design:	MZA, LJR, SSE
sheet #:	2 of 11
sheet description:	BOTTOM_CONNECTORS
date last modified:	2014-11-14

data bus 0

data bus 1

data bus 2

mon

data bus 3

column 0

column 1

column 2

column 3

global
carrier3
carrier1
carrier2
carrier0

carrier0
carrier2
carrier1
carrier3
global

3V

4V

AMP_5V

5V

spare

J4_113_R25

R25

remote clock enable

general purpose I/Os

provides 3V for 2.5V regulators
provides 4V for 3.3V regulators
provides 5V for amplifiers

3.3V

4PIN_MON

J3_027_H14
J3_028_J15
J3_029_H15
J3_031_J16

A
B
C
D

GND1
GND6

J13

GND

TEST_POINT

6PIN_RA_MOLEX

J15

FX8C-120S-SV

FX8C-100S-SV

NC

J1

J2

J3

J4

i2c

E
IDL_14_044
LJR, MZA, KAN, GSV, LM
MZA, LJR, SSE

3 of 11
TOP_CONNECTORS
2014-11-14

IMPORTANT SCROD pin mapping page

provides power to ASIC
320mV max dropout

3V
VA0
LT1963
IN
OUT
TAB-GND
GND
CB1 100uF 1206
CB2 100uF 1206
2.5V_0
2V5_0
0_2V5

C76 0.1uF 0402
C1 0.1uF 0402
C2 0.1uF 0402
C3 0.1uF 0402
C4 0.1uF 0402
C5 0.1uF 0402
C6 0.1uF 0402
C7 0.1uF 0402
C8 0.1uF 0402
CA35 22uF 0603
CA1 22uF 0603
CA2 22uF 0603
CA3 22uF 0603
CA4 22uF 0603
CA5 22uF 0603
CA6 22uF 0603
CA7 22uF 0603
CA8 22uF 0603

global row column p2p

p2p column row global

VDD33 VDD41 VDD47 VDD54 VDD58 VDD60 VDD64 VDD72 VDD75 VDD81 VDD92 VDD96 VDD101 VDD111 VDD117 VDD123

J1_008_R2.J1_006_P1
J2_057_W19
J2_056_V18
J2_054_AC22
PCLK
SIN
SCLK
REGCLR

2.5V_0
VDD1
VDD9
VDD17
VDD25
RL4 10k 0402
SHIN
0402 10uF C107
VADJP
GND
0402 10uF C108
VADJN

ASIC1_CAL
CAL_CH0
CAL_CH1
CAL_CH2
CAL_CH3
CAL_CH4
CAL_CH5
CAL_CH6
CAL_CH7

AMP_DISABLE
ASIC0_RAW_RF0
ASIC0_RAW_RF1
ASIC0_RAW_RF2
ASIC0_RAW_RF3
ASIC0_RAW_RF4
ASIC0_RAW_RF5
ASIC0_RAW_RF6
ASIC0_RAW_RF7
ASIC0_AMPED_RF0
ASIC0_AMPED_RF1
ASIC0_AMPED_RF2
ASIC0_AMPED_RF3
ASIC0_AMPED_RF4
ASIC0_AMPED_RF5
ASIC0_AMPED_RF6
ASIC0_AMPED_RF7
RFIN_0
RFIN_1
RFIN_2
RFIN_3
RFIN_4
RFIN_5
RFIN_6
RFIN_7
J9
2MM_EDGE_16PIN_CONN
ASIC0_AMPS
SHEET-5

VPED_0A
VPED_0B
VPED_1A
VPED_1B
VPED_2B
VPED_2A
VPED_3A
VPED_3B
VPED_4A
VPED_4B
VPED_5B
VPED_5A
VPED_6B
VPED_6A
VPED_7B
VPED_7A

ASIC0
IRS3D

SHOUT
RD_ENA
J2_013_AD6.J2_011_AE5

TRG_0 J1_113_C1.J1_115_F1
TRG_1 J1_110_D1.J1_107_E2
TRG_2 J2_096_AD5.J2_098_AA7
TRG_3 J2_090_Y9.J2_093_AB7
TRG_4 J2_085_AB9.J2_088_W10
TRG_5 J2_080_W12.J2_082_AA11
TRG_6 J2_024_AA6.J2_077_Y12
TRG_7 J1_102_H1.J1_105_G1

TIMING2 J2_008_AF4.J2_005_AC5
TIMING1 J2_027_M10.J2_031_AA15

SAMPSEL_ANY
DO_SCLK
DO_SIN
DO_DIR
DOE
J2_073_W14
J2_068_AA16
J2_066_AB17

DO_0 J1_026_AD1
DO_1 J1_024_AC2
DO_2 J1_023_AC1
DO_3 J1_022_AB1
DO_4 J1_020_AA2
DO_5 J1_019_AA1
DO_6 J1_018_Y1
DO_7 J1_016_W2
DO_8 J1_015_W1
DO_9 J1_014_V1
DO_10 J1_012_U2
DO_11 J1_011_U1

DO_SHOUT
DONE_IN
DONE
J2_020_AB13.J2_017_V11

GCC_CLKN
GCC_CLKP
SSTINN
SSTINP
GCC_CLKN_0
J2_023_AA12.J3_076_T9
SSTINN_0
J2_004_W8

GCC_RESET
RD_DIR
RD_SCLK
RD_SIN
RD_SHOUT
J2_060_AB21
J2_064_AB19
J2_062_V16
J2_061_AA17

provides pedestal voltage for ASIC

2.5V_0
1.25V_0
VB0
VIN VOUT
GND
1P2V_0
CG1 1uF 0402
CG2 1uF 0402
C93 0.1uF 0402
C92 0.1uF 0402
MCP1700T-1202E

J4_103_Y26
J4_106_W26
J4_109_U24
J4_111_T26
J4_114_R26
J4_095_AD26
WR_CS_S0
WR_CS_S1
WR_CS_S2
WR_CS_S3
WR_CS_S4
WR_CS_S5

J2_072_P17
J2_070_AB15
J2_069_V15
WR_RS_S1
WR_RS_S2
WR_RS_S3

ISEL
J2_074_U13
RAMP
CMPBIAS0
CMPBIAS
PUBIAS0
PUBIAS
DO NOT INSTALL
RL0 14k 0402
CC2 200pF 0402 NP0 or C0G
RAMP0
C106 10nF 0402

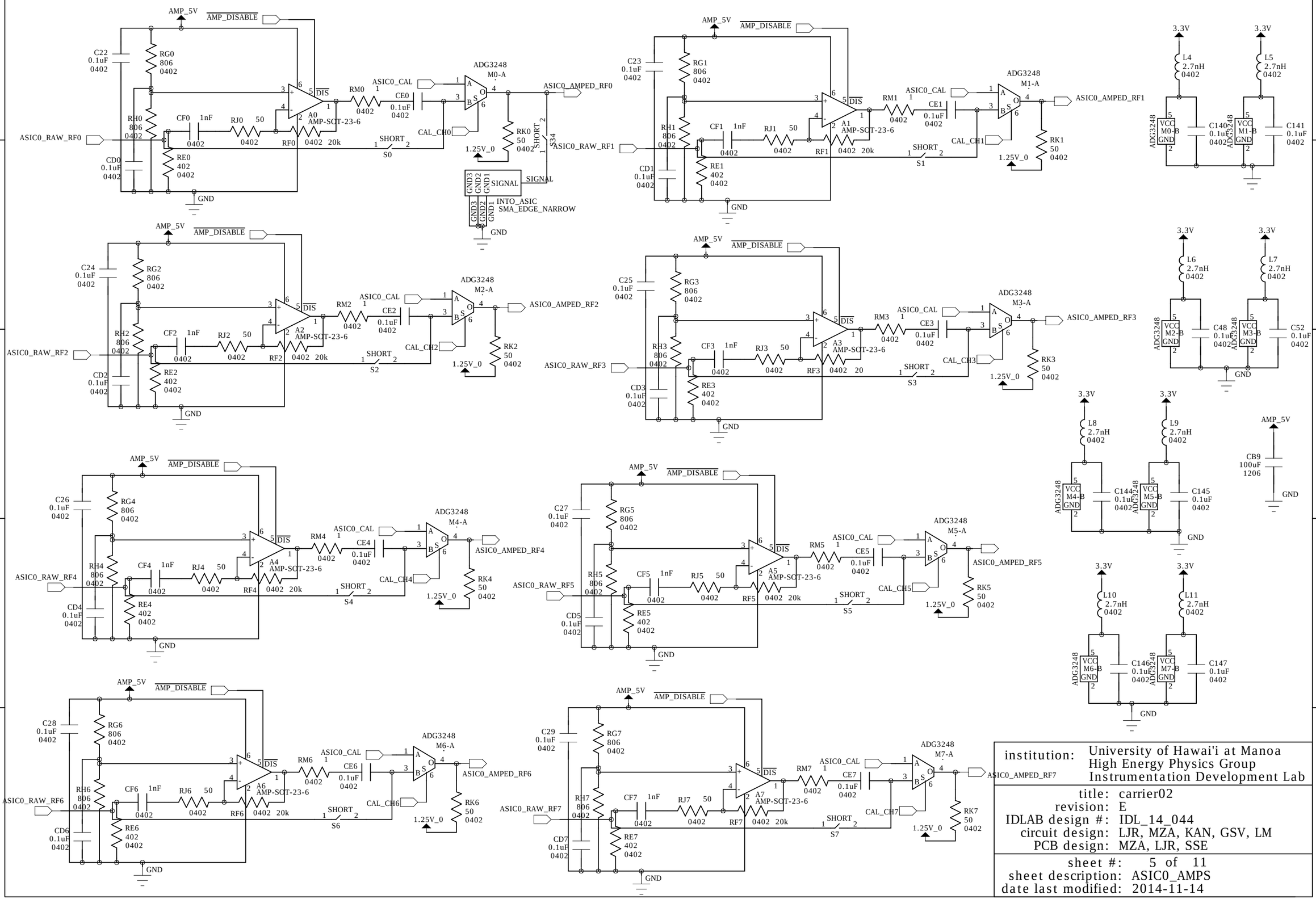
VRAMPREF RAMPMON GND5 GND13 GND21 GND29 GND34 GND46 GND57 GND61 GND67 GND73 GND76 GND87 GND93 GND97 CMP_VSS GND105 VDISCHARGE GND112 GND118 GND122 GND126

Voltage dividers for SSTinN & GCC_CLKN

2.5V_0
SSTINN_0
RS01 10k 0402
C10 100nF 0402
RS02 10k 0402
GND

2.5V_0
GCC_CLKN_0
RGC03 10k 0402
C11 100nF 0402
RGC04 10k 0402
GND

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier02
revision:	E
IDLAB design #:	IDL_14_044
circuit design:	LJR, MZA, KAN, GSV, LM
PCB design:	MZA, LJR, SSE
sheet #:	4 of 11
sheet description:	ASIC0
date last modified:	2014-11-14



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier02
revision:	E
IDLAB design #:	IDL_14_044
circuit design:	LJR, MZA, KAN, GSV, LM
PCB design:	MZA, LJR, SSE
sheet #:	5 of 11
sheet description:	ASIC0_AMPS
date last modified:	2014-11-14

IMPORTANT SCROD pin mapping page

provides power to ASIC
320mV max dropout

3V
VA1 LT1963
IN OUT TAB-GND GND
CB3 100uF 1206
CB4 100uF 1206
2.5V_1
2V5_1
1_2V5
C91 0.1uF 0402
C31 0.1uF 0402
C32 0.1uF 0402
C33 0.1uF 0402
C34 0.1uF 0402
C35 0.1uF 0402
C36 0.1uF 0402
C37 0.1uF 0402
C50 0.1uF 0402
CA36 22uF 0603
CA9 22uF 0603
CA10 22uF 0603
CA11 22uF 0603
CA12 22uF 0603
CA13 22uF 0603
CA14 22uF 0603
CA15 22uF 0603
CA16 22uF 0603

global row column p2p

p2p column row global

J1_038_K5.J1_035_J3
J2_057_W19
J2_056_V18
J2_054_AC22
PCLK SIN SCLK REGCLR
VDD1 VDD9 VDD17 VDD25
SHIN
VADJP
VADJN
RL5 10K 0402
C109 10uF 0402
C110 10uF 0402
GND

ASIC1_CAL
CAL_CH0 CAL_CH1 CAL_CH2 CAL_CH3 CAL_CH4 CAL_CH5 CAL_CH6 CAL_CH7

AMP_DISABLE
16PIN_CONN
2MM_EDGE_16PIN_CONN
J10
GND

ASIC1_RAW_RF0 ASIC1_RAW_RF1 ASIC1_RAW_RF2 ASIC1_RAW_RF3 ASIC1_RAW_RF4 ASIC1_RAW_RF5 ASIC1_RAW_RF6 ASIC1_RAW_RF7
ASIC1_AMPED_RF0 ASIC1_AMPED_RF1 ASIC1_AMPED_RF2 ASIC1_AMPED_RF3 ASIC1_AMPED_RF4 ASIC1_AMPED_RF5 ASIC1_AMPED_RF6 ASIC1_AMPED_RF7
RFIN_0 RFIN_1 RFIN_2 RFIN_3 RFIN_4 RFIN_5 RFIN_6 RFIN_7
ASIC1_AMPS SHEET-7

provides pedestal voltage for ASIC
2.5V_1
VB1
VIN VOUT GND
MCP1700T-1202E
CG3 1uF 0402
CG14 1uF 0402
C95 0.1uF 0402
C94 0.1uF 0402
1.25V_1
1P2V_1
GND

VPED_0A VPED_0B VPED_1A VPED_1B VPED_2B VPED_2A VPED_3A VPED_3B VPED_4A VPED_4B VPED_5B VPED_5A VPED_6B VPED_6A VPED_7B VPED_7A

J4_103_Y26
J4_106_W26
J4_109_U24
J4_111_T26
J4_114_R26
J4_095_AD26
WR_CS_S0 WR_CS_S1 WR_CS_S2 WR_CS_S3 WR_CS_S4 WR_CS_S5

J2_072_P17
J2_070_AB15
J2_069_V15
WR_RS_S1 WR_RS_S2 WR_RS_S3

ISEL
J2_074_U13
RAMP
CMPBIAS1
CMPBIAS
PUBIAS1
PUBIAS
DO NOT INSTALL
RL1 14k 0402
VRAMPREF RAMPMON
CC1 200pF 0402 NP0 or C0G
RAMP1

GND5 GND13 GND21 GND29 GND34 GND46 GND57 GND61 GND67 GND73 GND76 GND87 GND93 GND97 CMP_VSS GND105 VDISCHARGE GND112 GND118 GND122 GND126
C105 10nF 0402

ASIC1
IRS3D

SHOUT
SHOUT1
RD_ENA
J1_097_L1.J1_094_M1

TRG_0 TRG_1 TRG_2 TRG_3 TRG_4 TRG_5 TRG_6 TRG_7
J1_091_N2.J1_089_F3
J1_086_H5.J1_083_K3
J2_033_Y15.J2_036_W16
J2_039_U15.J2_041_AA21
J1_081_M3.J1_078_N5
J1_075_R4.J1_073_U3
J1_070_V4.J1_067_Y3
J1_065_AB3.J1_062_AC4

TIMING2 TIMING1
J1_032_G3.J1_030_D3
J2_065_Y16.J2_053_Y20

SAMPSEL_ANY DO_SCLK DO_SIN DO_DIR DOE
J2_073_W14
J2_068_AA16
J2_066_AB17
DOE

DO_0 DO_1 DO_2 DO_3 DO_4 DO_5 DO_6 DO_7 DO_8 DO_9 DO_10 DO_11
J1_055_AA4
J1_054_Y5
J1_052_W5
J1_051_V5
J1_050_V3
J1_048_U4
J1_047_T4
J1_046_R5
J1_044_R3
J1_043_P3
J1_042_N4
J1_040_M4

DO_SHOUT DONE_IN DONE
J2_045_B24.J2_048_W20
DO_SHOUT1
DONE1

GCC_CLKN GCC_CLKP SSTINN SSTINP
GCC_CLKN_1
J2_049_Y21
SSTINN_1
J1_028_AE2

GCC_RESET RD_DIR RD_SCLK RD_SIN RD_SHOUT
J2_060_AB21
J2_064_AB19
J2_062_V16
J2_061_AA17
RD_SHOUT1

Voltage divider for SSTinN & GCC_CLKN

2.5V_0
SSTINN_1
RS13 10k 0402
RS14 10k 0402
C38 100nF 0402
GND

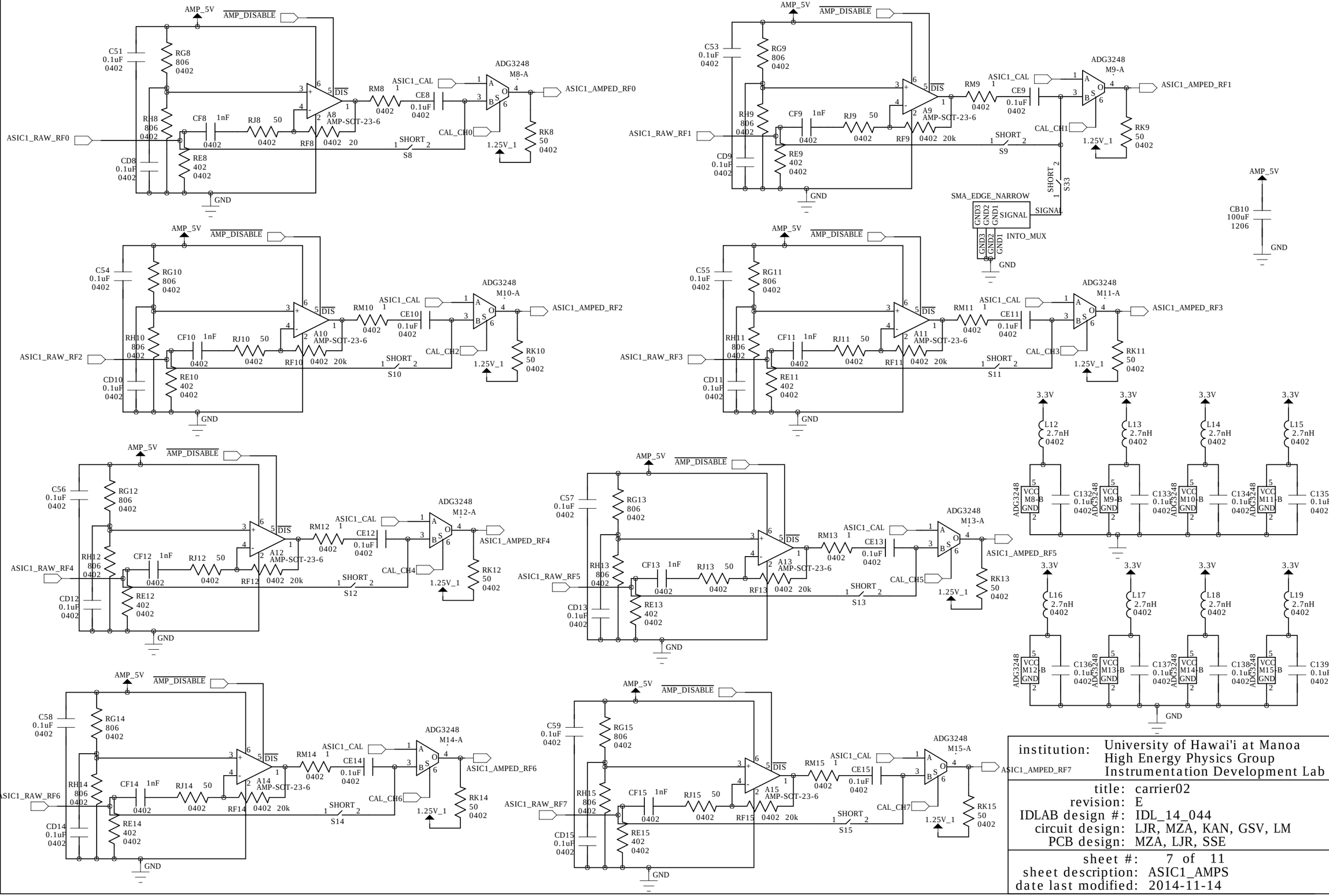
2.5V_0
GCC_CLKN_1
RGC11 10k 0402
RGC12 10k 0402
C9 100nF 0402
GND

temperature sensor for ASIC

2.5V
T1
VDD 2.25-3.6V
ADDR/THERM
SCL SDA
EVENT
GND
STTS751-0WB3F
RB2 12k 0402
RA2 7.5k 0402
C30 0.1uF 0402
J3_070_M18_SCL.J2_028_L10_SCL
J3_072_N18_SDA.J2_029_K10_SDA

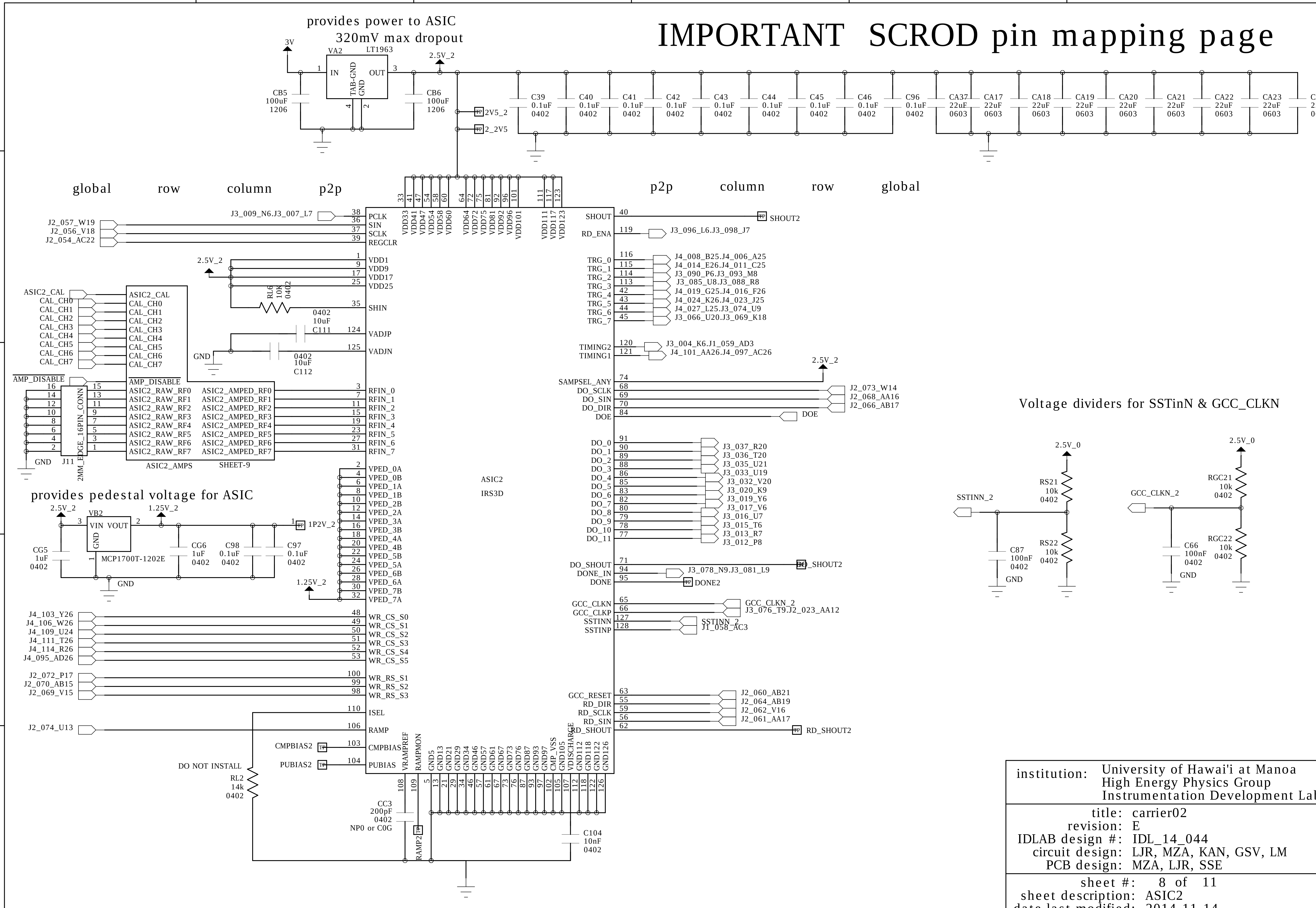
i2c address = 1001001

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier02
revision:	E
IDLAB design #:	IDL_14_044
circuit design:	LJR, MZA, KAN, GSV, LM
PCB design:	MZA, LJR, SSE
sheet #:	6 of 11
sheet description:	ASIC1
date last modified:	2014-11-14

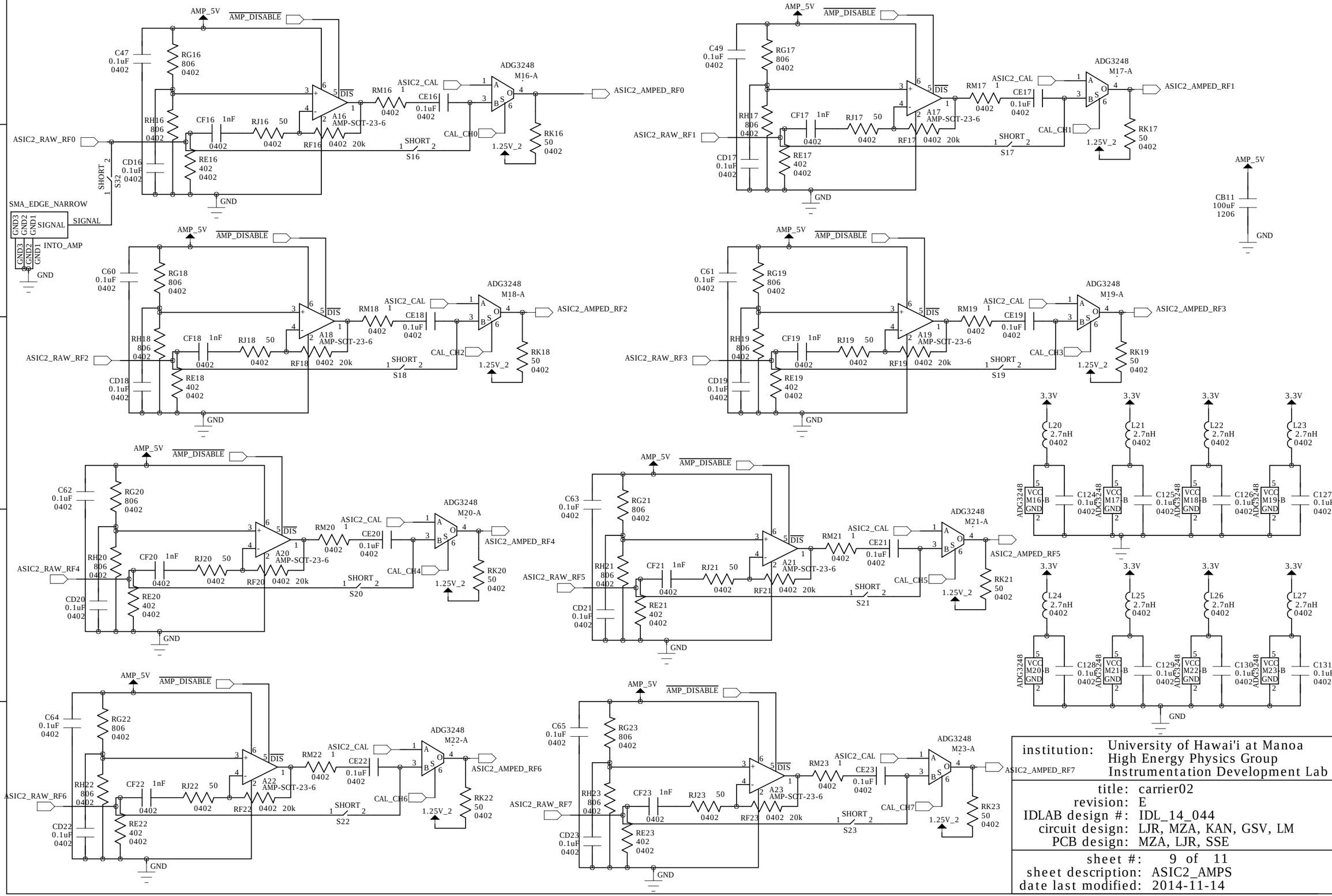


institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier02
revision:	E
IDLAB design #:	IDL_14_044
circuit design:	LJR, MZA, KAN, GSV, LM
PCB design:	MZA, LJR, SSE
sheet #:	7 of 11
sheet description:	ASIC1_AMPS
date last modified:	2014-11-14

IMPORTANT SCROD pin mapping page


provides power to ASIC
320mV max dropout
3V
VA2
LT1963
IN
OUT
TAB-GND
GND
2.5V_2
CB5
100uF
1206
CB6
100uF
1206
2V5_2
2_2V5
C39
C40
C41
C42
C43
C44
C45
C46
C96
0.1uF
0402
CA37
CA17
CA18
CA19
CA20
CA21
CA22
CA23
CA24
22uF
0603
global
row
column
p2p
ASIC2
IRS3D
PCLK
SIN
SCLK
REGCLR
J3_009_N6.J3_007_L7
J2_057_W19
J2_056_V18
J2_054_AC22
VDD1
VDD9
VDD17
VDD25
SHIN
RL6
10K
0402
VADJP
VADJN
10uF
C111
C112
GND
ASIC2_CAL
CAL_CH0
CAL_CH1
CAL_CH2
CAL_CH3
CAL_CH4
CAL_CH5
CAL_CH6
CAL_CH7
AMP_DISABLE
ASIC2_RAW_RF0
ASIC2_RAW_RF1
ASIC2_RAW_RF2
ASIC2_RAW_RF3
ASIC2_RAW_RF4
ASIC2_RAW_RF5
ASIC2_RAW_RF6
ASIC2_RAW_RF7
ASIC2_AMPED_RF0
ASIC2_AMPED_RF1
ASIC2_AMPED_RF2
ASIC2_AMPED_RF3
ASIC2_AMPED_RF4
ASIC2_AMPED_RF5
ASIC2_AMPED_RF6
ASIC2_AMPED_RF7
ASIC2_AMPS
SHEET-9
J11
2MM_EDGE_16PIN_CONN
RFIN_0
RFIN_1
RFIN_2
RFIN_3
RFIN_4
RFIN_5
RFIN_6
RFIN_7
provides pedestal voltage for ASIC
VB2
VIN
VOUT
MCP1700T-1202E
1.25V_2
1P2V_2
CG5
1uF
CG6
C98
C97
VPED_0A
VPED_0B
VPED_1A
VPED_1B
VPED_2A
VPED_2B
VPED_3A
VPED_3B
VPED_4A
VPED_4B
VPED_5A
VPED_5B
VPED_6A
VPED_6B
VPED_7A
VPED_7B
J4_103_Y26
J4_106_W26
J4_109_U24
J4_111_T26
J4_114_R26
J4_095_AD26
WR_CS_S0
WR_CS_S1
WR_CS_S2
WR_CS_S3
WR_CS_S4
WR_CS_S5
J2_072_P17
J2_070_AB15
J2_069_V15
WR_RS_S1
WR_RS_S2
WR_RS_S3
ISEL
J2_074_U13
RAMP
CMPBIAS2
CMPBIAS
PUBIAS2
PUBIAS
DO NOT INSTALL
RL2
14k
VRAMPREF
RAMPMON
CC3
200pF
NP0 or C0G
RAMP2
C104
10nF
CMP_VSS
VDISCHARGE
SHOUT
SHOUT2
RD_ENA
J3_096_L6.J3_098_J7
TRG_0
TRG_1
TRG_2
TRG_3
TRG_4
TRG_5
TRG_6
TRG_7
J4_008_B25.J4_006_A25
J4_014_E26.J4_011_C25
J3_090_P6.J3_093_M8
J3_085_U8.J3_088_R8
J4_019_G25.J4_016_F26
J4_024_K26.J4_023_J25
J4_027_L25.J3_074_U9
J3_066_U20.J3_069_K18
TIMING2
TIMING1
J3_004_K6.J1_059_AD3
J4_101_AA26.J4_097_AC26
SAMPSEL_ANY
DO_SCLK
DO_SIN
DO_DIR
DOE
J2_073_W14
J2_068_AA16
J2_066_AB17
DO_0
DO_1
DO_2
DO_3
DO_4
DO_5
DO_6
DO_7
DO_8
DO_9
DO_10
DO_11
J3_037_R20
J3_036_T20
J3_035_U21
J3_033_U19
J3_032_V20
J3_020_K9
J3_019_Y6
J3_017_V6
J3_016_U7
J3_015_T6
J3_013_R7
J3_012_P8
DO_SHOUT
DONE_IN
DONE
DO_SHOUT2
J3_078_N9.J3_081_L9
DONE2
GCC_CLKN
GCC_CLKP
GCC_CLKN_2
J3_076_T9.J2_023_AA12
SSTINN
SSTINP
SSTINN_2
J1_058_AC3
GCC_RESET
RD_DIR
RD_SCLK
RD_SIN
RD_SHOUT
J2_060_AB21
J2_064_AB19
J2_062_V16
J2_061_AA17
RD_SHOUT2
Voltage dividers for SSTinN & GCC_CLKN
2.5V_0
RS21
RS22
10k
C87
100nF
RGC21
RGC22
C66

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier02
revision:	E
IDLAB design #:	IDL_14_044
circuit design:	LJR, MZA, KAN, GSV, LM
PCB design:	MZA, LJR, SSE
sheet #:	8 of 11
sheet description:	ASIC2
date last modified:	2014-11-14



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier02
revision:	E
IDLAB design #:	IDL_14_044
circuit design:	LJR, MZA, KAN, GSV, LM
PCB design:	MZA, LJR, SSE
sheet #:	9 of 11
sheet description:	ASIC2_AMPS
date last modified:	2014-11-14

IMPORTANT SCROD pin mapping page

provides power to ASIC
320mV max dropout

3V
VA3
LT1963
IN
TAB-GND
GND
OUT
2.5V_3
CB7 100uF 1206
CB8 100uF 1206
2V5_3
3_2V5
C67 0.1uF 0402
C68 0.1uF 0402
C69 0.1uF 0402
C70 0.1uF 0402
C71 0.1uF 0402
C72 0.1uF 0402
C73 0.1uF 0402
C74 0.1uF 0402
C99 0.1uF 0402
CA38 22uF 0603
CA25 22uF 0603
CA26 22uF 0603
CA27 22uF 0603
CA28 22uF 0603
CA29 22uF 0603
CA30 22uF 0603
CA31 22uF 0603
CA32 22uF 0603

global row column p2p

p2p column row global

ASIC3
IRS3D

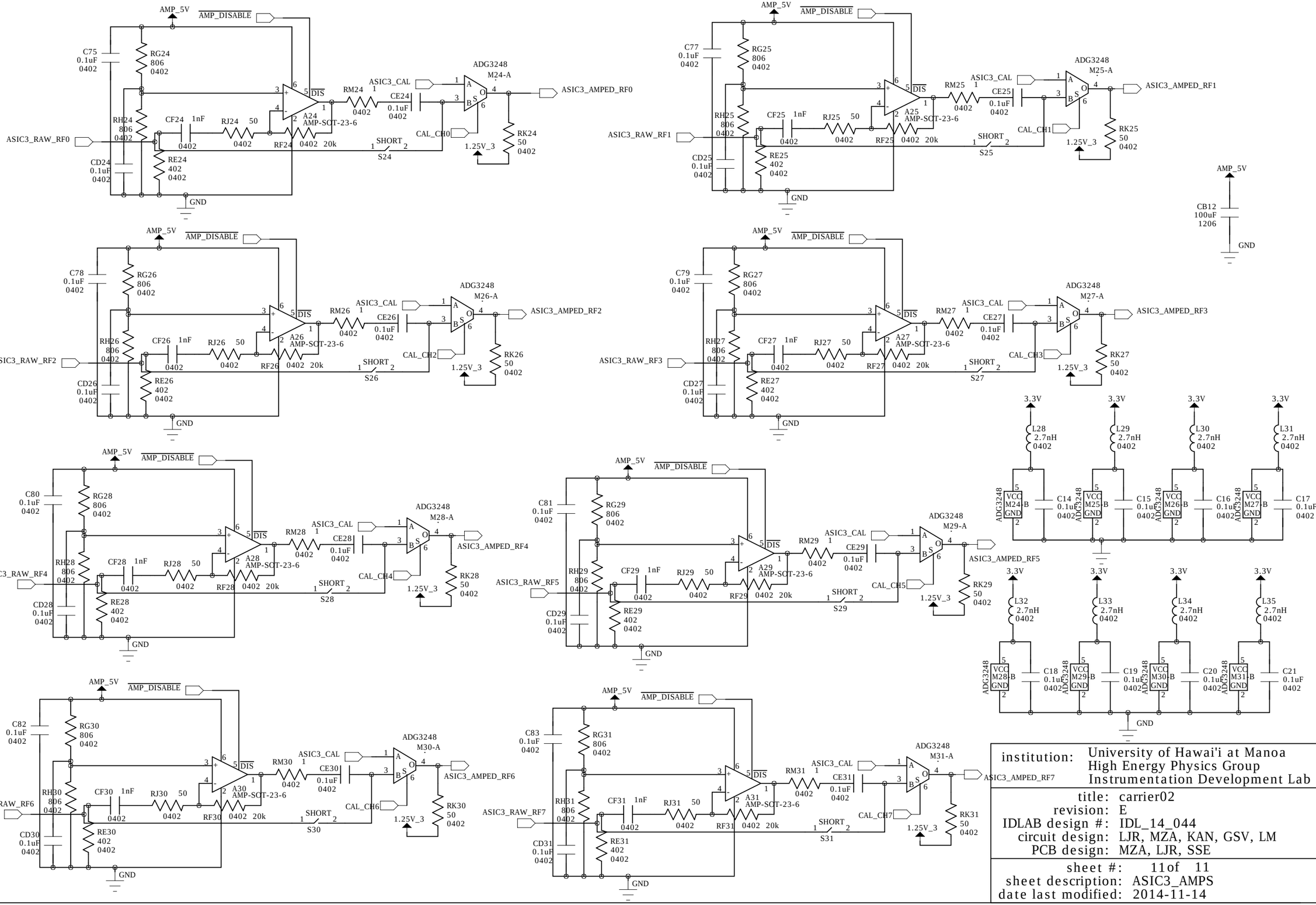
provides pedestal voltage for ASIC

2.5V_3
VB3
VIN VOUT
GND
1.25V_3
1P2V_3
CG7 1uF 0402
MCP1700T-1202E
CG8 1uF 0402
C101 0.1uF 0402
C100 0.1uF 0402

Voltage dividers for SSTinN & GCC_CLKN

2.5V_0
SSTINN_3
RS31 10k 0402
RS32 10k 0402
C102 100nF 0402
GCC_CLKN_3
RGC31 10k 0402
RGC32 10k 0402
C89 100nF 0402

institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier02
revision:	E
IDLAB design #:	IDL_14_044
circuit design:	LJR, MZA, KAN, GSV, LM
PCB design:	MZA, LJR, SSE
sheet #:	10of 11
sheet description:	ASIC3
date last modified:	2014-11-14



institution:	University of Hawai'i at Manoa High Energy Physics Group Instrumentation Development Lab
title:	carrier02
revision:	E
IDLAB design #:	IDL_14_044
circuit design:	LJR, MZA, KAN, GSV, LM
PCB design:	MZA, LJR, SSE
sheet #:	11of 11
sheet description:	ASIC3_AMPS
date last modified:	2014-11-14