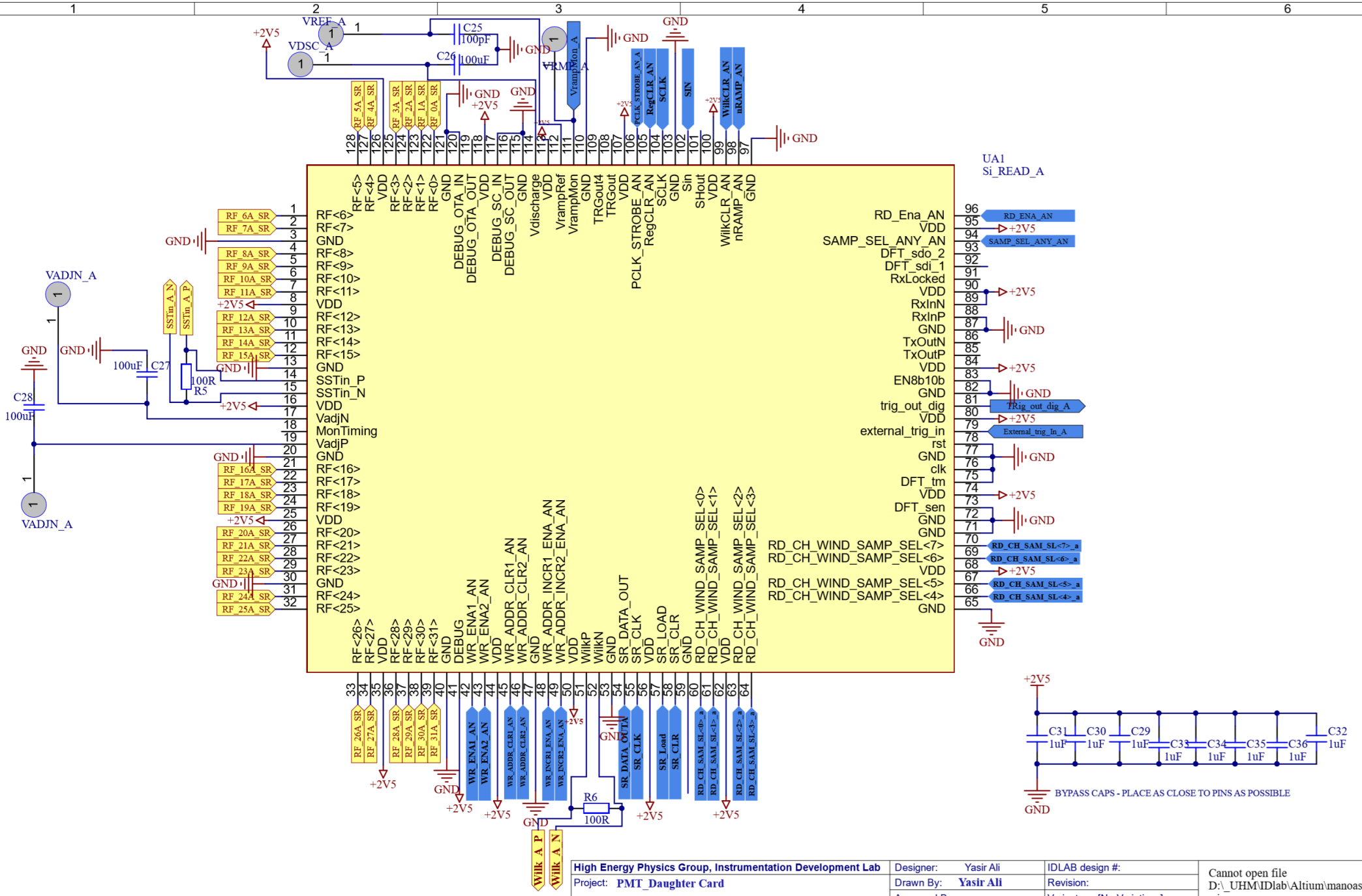
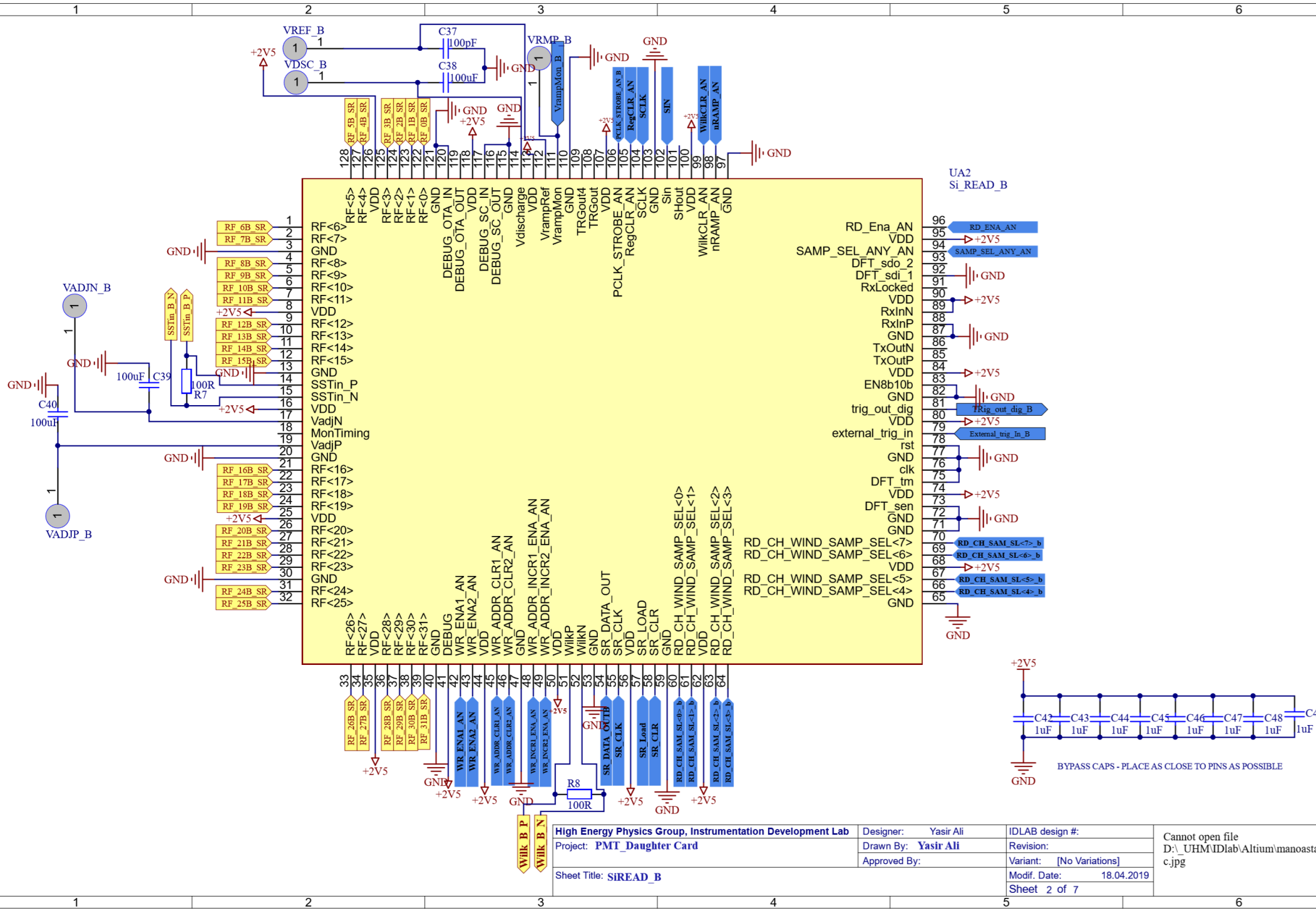
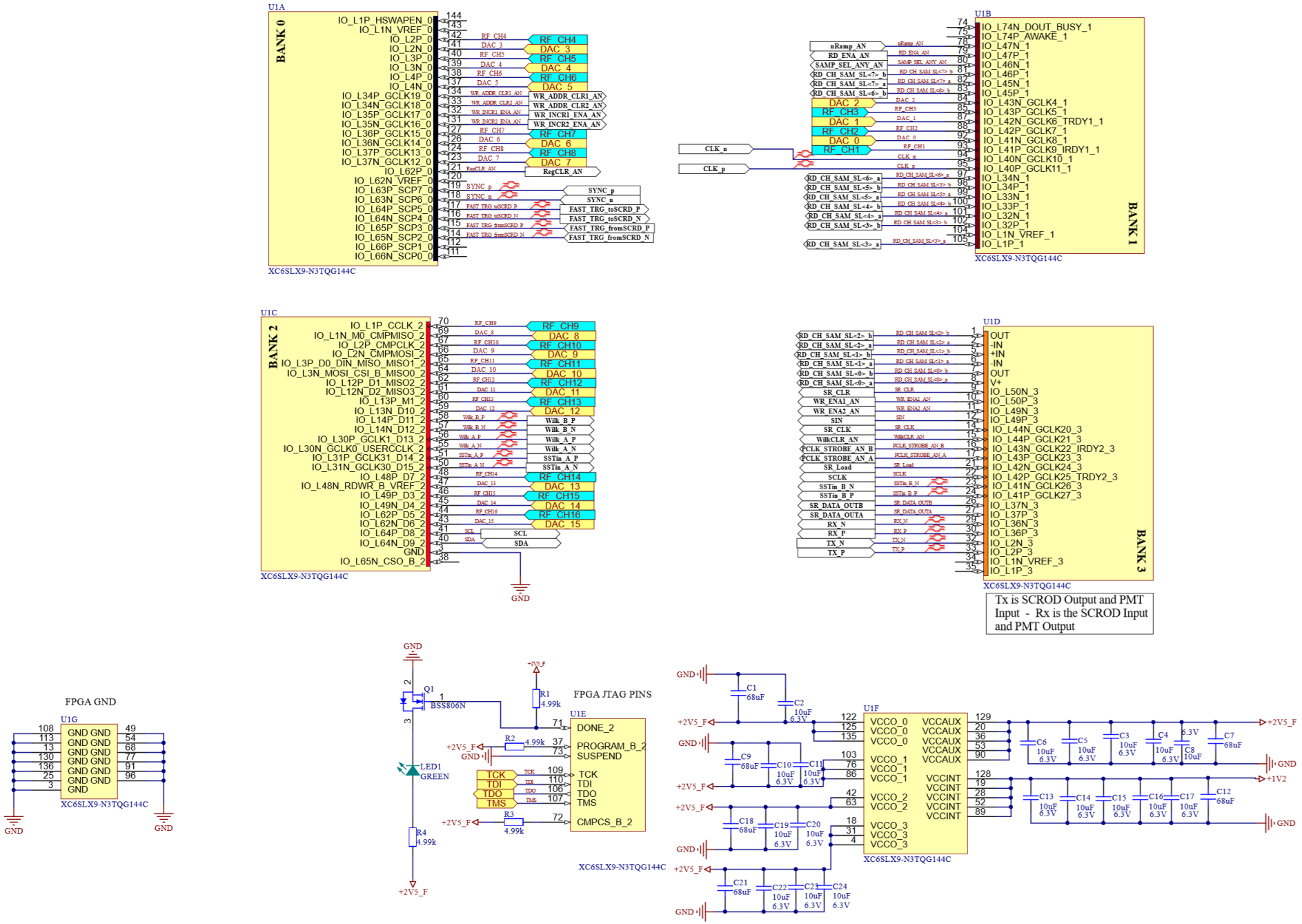


High Energy Physics Group, Instrumentation Development Lab	Designer: Yasir Ali	IDLAB design #:
Project: PMT_Daughter Card	Drawn By: Yasir Ali	Revision:
	Approved By:	Variant: [No Variations]
Sheet Title: SiREAD_A		Modif. Date: 18.04.2019
		Sheet 1 of 7

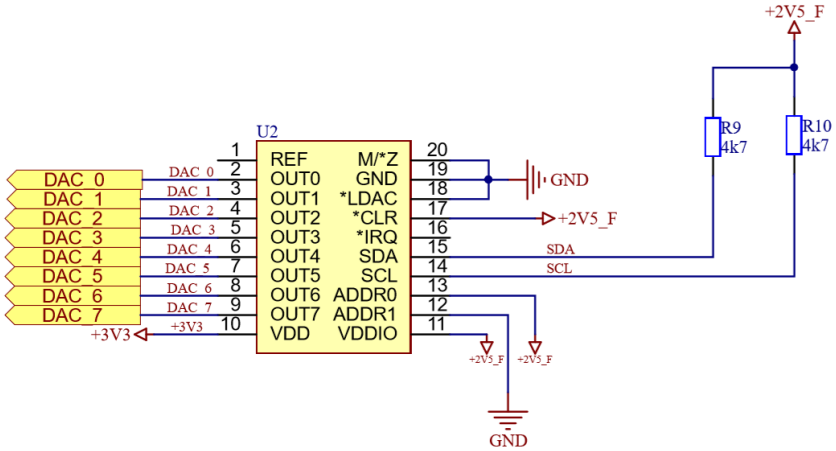
Cannot open file D:_UHM\IDlab\Altium\manoastackedc.jpg

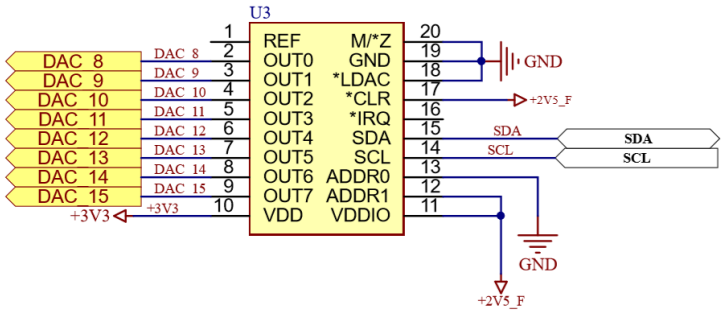

UA2
Si_READ_B
VREF_B
VDSC_B
VRMP_B
C37
100pF
C38
100uF
VadjN
MonTiming
VadjP
VADJN_B
VADJP_B
C39
100uF
C40
100uF
R7
100R
SSTin_B_N
SSTin_B_P
R8
100R
C41
1uF
C42
1uF
C43
1uF
C44
1uF
C45
1uF
C46
1uF
C47
1uF
C48
1uF
BYPASS CAPS - PLACE AS CLOSE TO PINS AS POSSIBLE
RF<0>
RF<1>
RF<2>
RF<3>
RF<4>
RF<5>
RF<6>
RF<7>
RF<8>
RF<9>
RF<10>
RF<11>
RF<12>
RF<13>
RF<14>
RF<15>
RF<16>
RF<17>
RF<18>
RF<19>
RF<20>
RF<21>
RF<22>
RF<23>
RF<24>
RF<25>
RF<26>
RF<27>
RF<28>
RF<29>
RF<30>
RF<31>
RF_0B_SR
RF_1B_SR
RF_2B_SR
RF_3B_SR
RF_4B_SR
RF_5B_SR
RF_6B_SR
RF_7B_SR
RF_8B_SR
RF_9B_SR
RF_10B_SR
RF_11B_SR
RF_12B_SR
RF_13B_SR
RF_14B_SR
RF_15B_SR
RF_16B_SR
RF_17B_SR
RF_18B_SR
RF_19B_SR
RF_20B_SR
RF_21B_SR
RF_22B_SR
RF_23B_SR
RF_24B_SR
RF_25B_SR
RF_26B_SR
RF_27B_SR
RF_28B_SR
RF_29B_SR
RF_30B_SR
RF_31B_SR
DEBUG_OTA_IN
DEBUG_OTA_OUT
DEBUG_SC_IN
DEBUG_SC_OUT
Vdischarge
VrampRef
VrampMon
TRGout4
TRGout
PCLK_STROBE_AN
RegCLR_AN
SCLK
Sin
SHout
WilkCLR_AN
nRAMP_AN
DEBUG
WR_ENA1_AN
WR_ENA2_AN
WR_ADDR_CLR1_AN
WR_ADDR_CLR2_AN
WR_ADDR_INCR1_ENA_AN
WR_ADDR_INCR2_ENA_AN
WilkP
WilkN
SR_DATA_OUT
SR_CLK
SR_LOAD
SR_CLR
RD_CH_WIND_SAMP_SEL<0>
RD_CH_WIND_SAMP_SEL<1>
RD_CH_WIND_SAMP_SEL<2>
RD_CH_WIND_SAMP_SEL<3>
RD_Ena_AN
SAMP_SEL_ANY_AN
DFT_sdo_2
DFT_sdi_1
RxLocked
RxInN
RxInP
TxOutN
TxOutP
EN8b10b
trig_out_dig
external_trig_in
rst
clk
DFT_tm
DFT_sen
RD_CH_WIND_SAMP_SEL<7>
RD_CH_WIND_SAMP_SEL<6>
RD_CH_WIND_SAMP_SEL<5>
RD_CH_WIND_SAMP_SEL<4>
RD_ENA_AN
TRig_out_dig_B
External_trig_In_B
RD_CH_SAM_SL<7>_b
RD_CH_SAM_SL<6>_b
RD_CH_SAM_SL<5>_b
RD_CH_SAM_SL<4>_b
RD_CH_SAM_SL<0>_b
RD_CH_SAM_SL<1>_b
RD_CH_SAM_SL<2>_b
RD_CH_SAM_SL<3>_b
Wilk_B_P
Wilk_B_N
+2V5
GND
High Energy Physics Group, Instrumentation Development Lab
Project: PMT_Daughter Card
Sheet Title: SiREAD_B
Designer: Yasir Ali
Drawn By: Yasir Ali
Approved By:
IDLAB design #:
Revision:
Variant: [No Variations]
Modif. Date: 18.04.2019
Sheet 2 of 7
Cannot open file
D:_UHM\IDlab\Altium\manoastacked
c.jpg

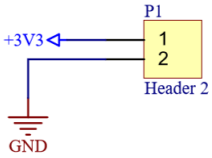


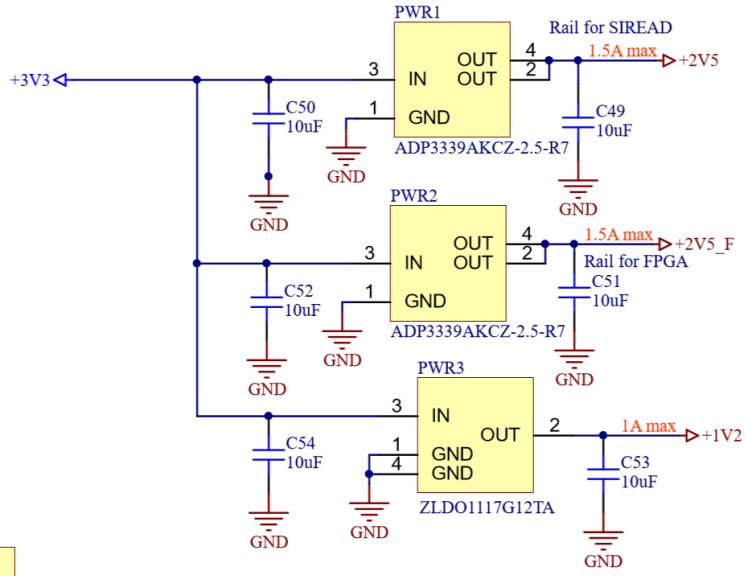
High Energy Physics Group, Instrumentation Development Lab	Designer: Yasir Ali	IDLAB design #:	
Board: PMT_Daughter Card	Drawn By: Yasir Ali	Revision:	
	Approved By:	Variant: [No Variations]	
Sheet Title: FPGA_Spartan6		Modif. Date: 18.04.2019	
		Sheet 3 of 7	

UNIVERSITY of HAWAI'I' MĀNOA

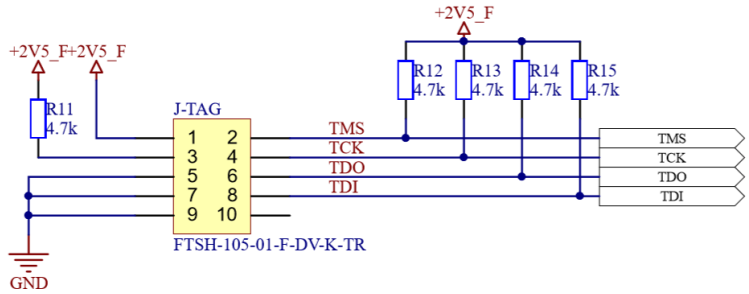




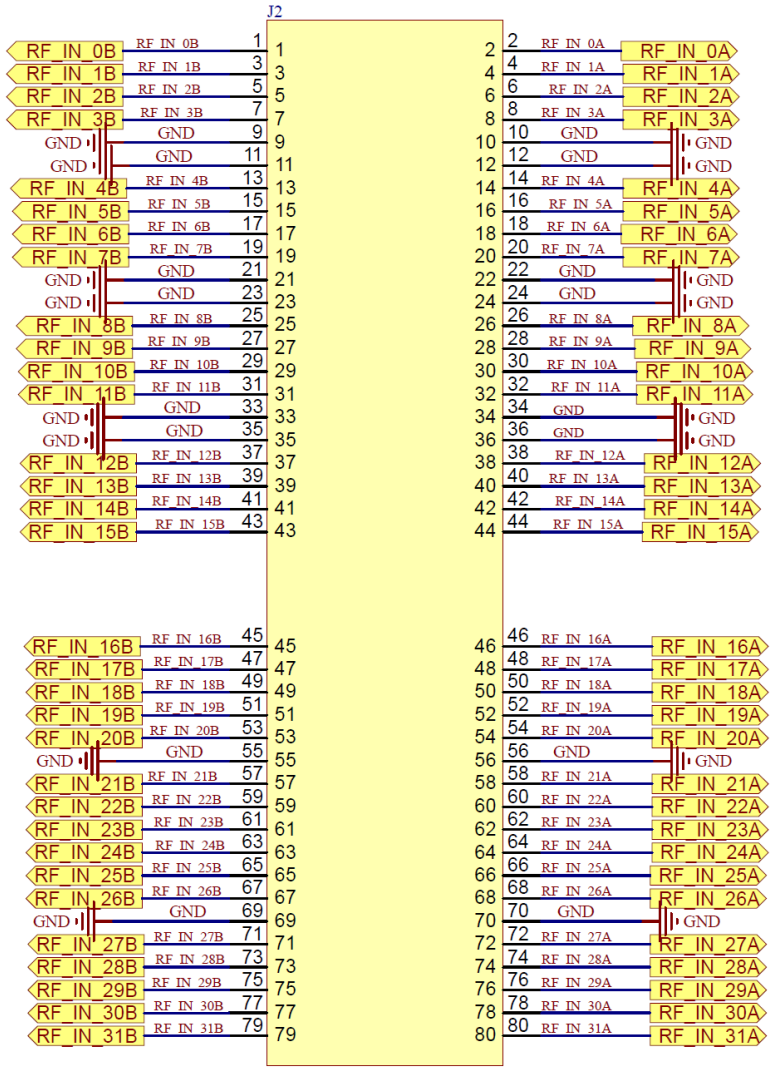




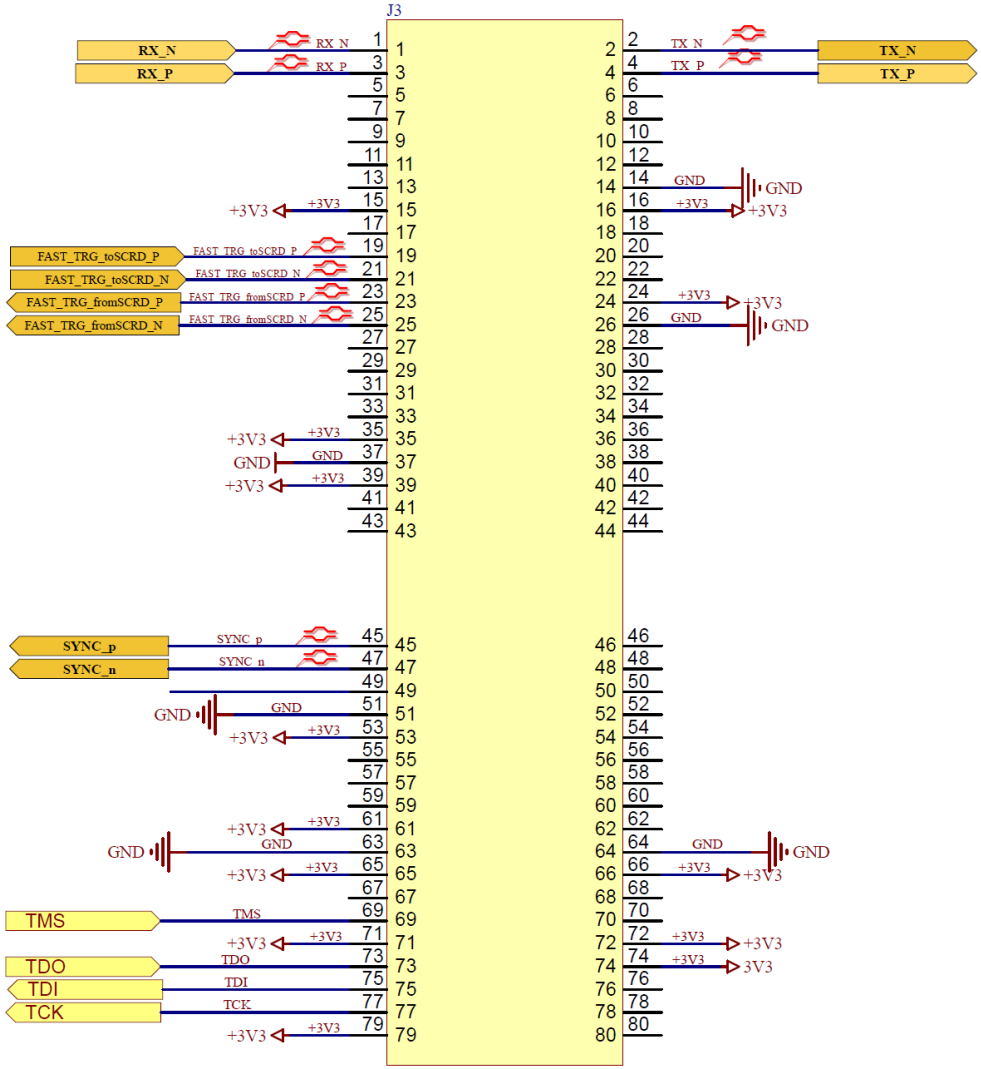
JTag



High Energy Physics Group, Instrumentation Development Lab	Designer: Yasir Ali	IDLAB design #:	Cannot open file D:_UHM\IDlab\Altium\manoastackedc.jpg
Project: PMT_Daughter Card	Drawn By: Yasir Ali	Revision:	
	Approved By:	Variant: [No Variations]	
Sheet Title: DAC and Regulators		Modif. Date: 30.04.2019	
		Sheet 4 of 7	



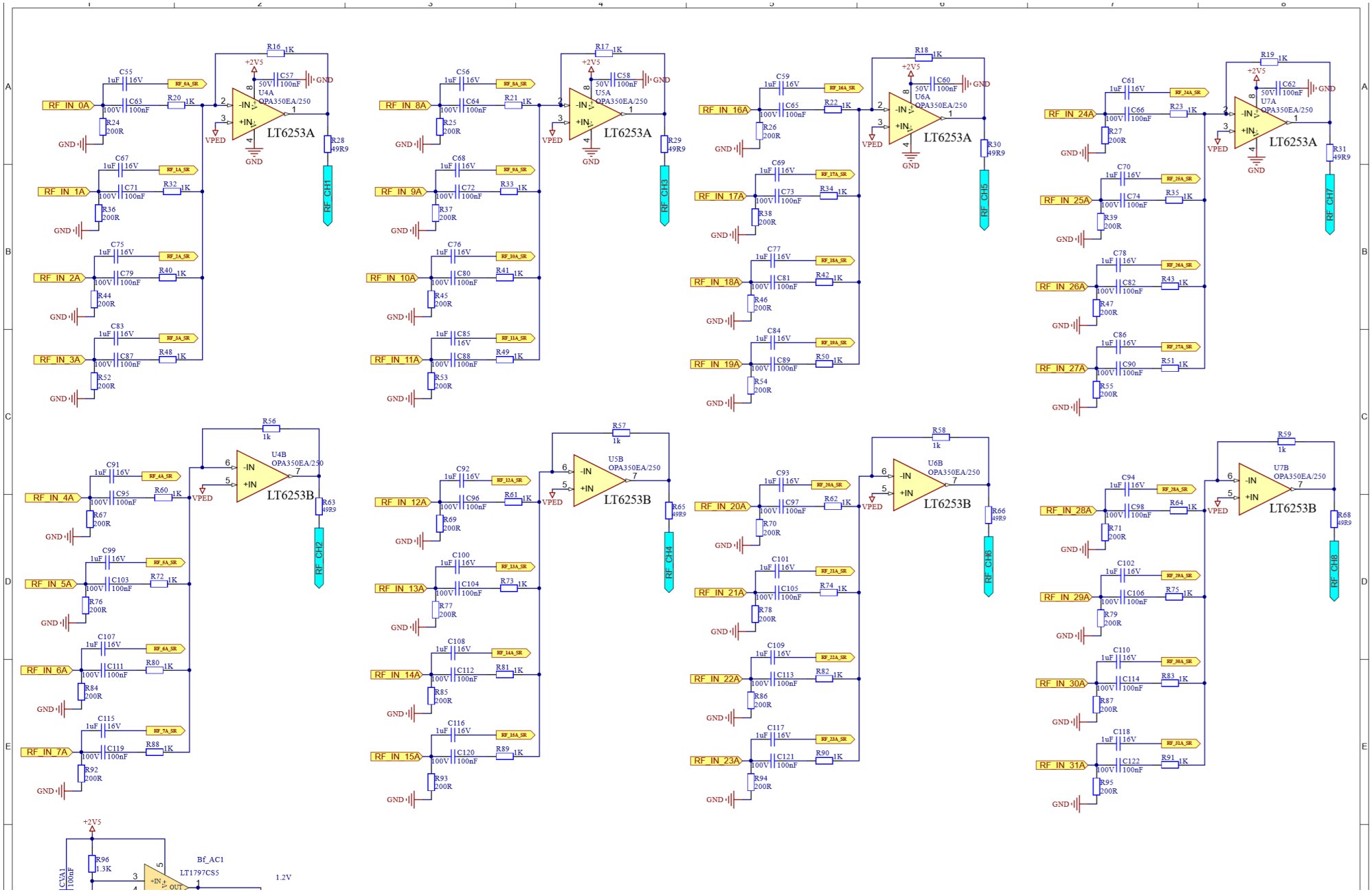
SPD08 Card Edge Connector Mating Card Layout

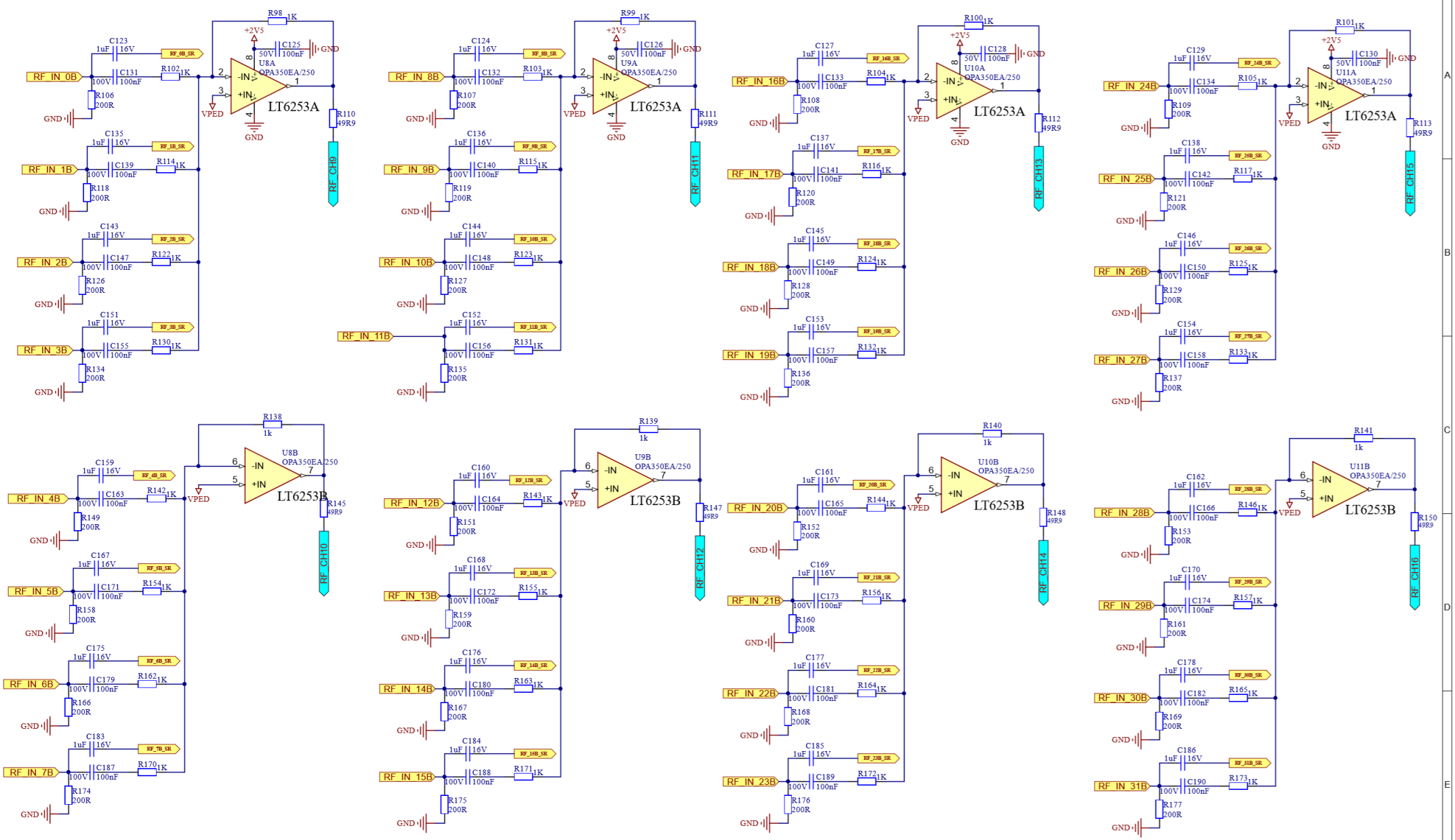


SPD08 Card Edge Connector Mating Card Layout

FAST_TRG_fromSCROD_n

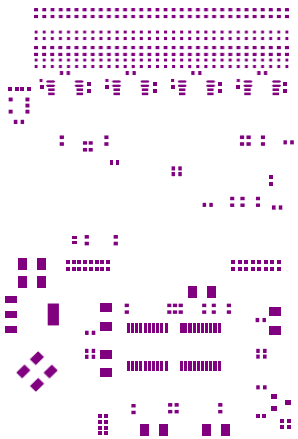
High Energy Physics Group, Instrumentation Development Lab	Designer: Yasir Ali	IDLAB design #:	Cannot open file D:_UHM\IDlab\Altium\manoastackedc.jpg
Project: PMT_Daughter Card	Drawn By: Yasir Ali	Revision:	
	Approved By:	Variant: [No Variations]	
Sheet Title: I/O Edge Connectors		Modif. Date: 5/1/2019	
		Sheet 5 of 7	

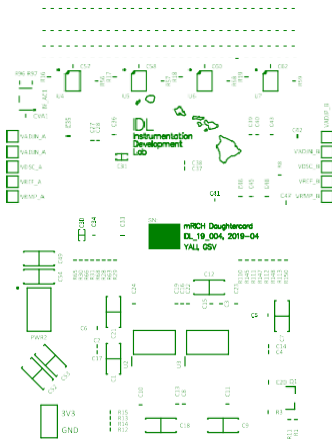

RF_IN_0A
RF_IN_1A
RF_IN_2A
RF_IN_3A
RF_IN_8A
RF_IN_9A
RF_IN_10A
RF_IN_11A
RF_IN_16A
RF_IN_17A
RF_IN_18A
RF_IN_19A
RF_IN_24A
RF_IN_25A
RF_IN_26A
RF_IN_27A
RF_IN_4A
RF_IN_5A
RF_IN_6A
RF_IN_7A
RF_IN_12A
RF_IN_13A
RF_IN_14A
RF_IN_15A
RF_IN_20A
RF_IN_21A
RF_IN_22A
RF_IN_23A
RF_IN_28A
RF_IN_29A
RF_IN_30A
RF_IN_31A
LT6253A
LT6253B
OPA350EA/250
+2V5
VPED
GND
RF_CH1
RF_CH2
RF_CH3
RF_CH4
RF_CH5
RF_CH6
RF_CH7
RF_CH8
Bf_AC1
LT1797CS5
1.2V

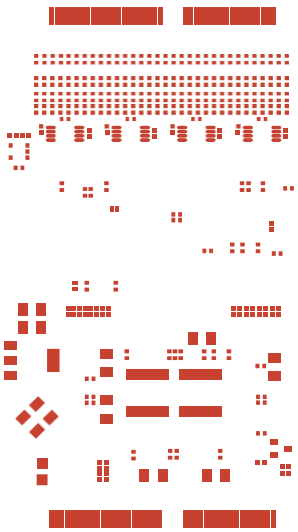


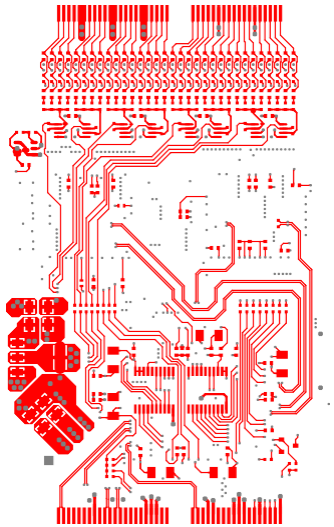
High Energy Physics Group, Instrumentation Development Lab	Designer: Yasir Ali	IDLAB design #:
Board: PMT_Daughter Card	Drawn By: Yasir Ali	Revision:
	Approved By:	Variant: [No Variations]
Sheet Title: Summing Amplifier_II		Modif. Date: 16.04.2019
		Sheet 7 of 7

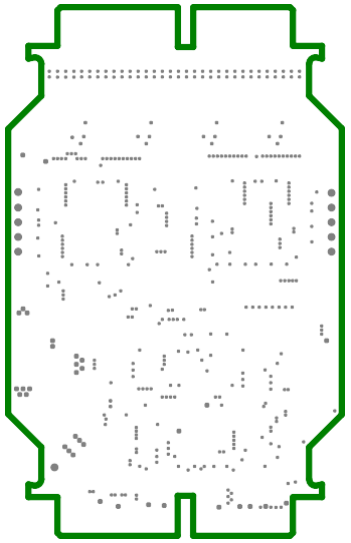
UNIVERSITY of HAWAI'I MĀNOA

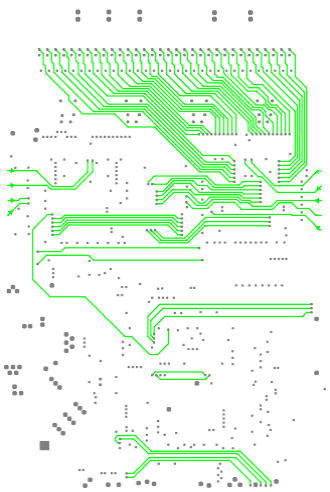


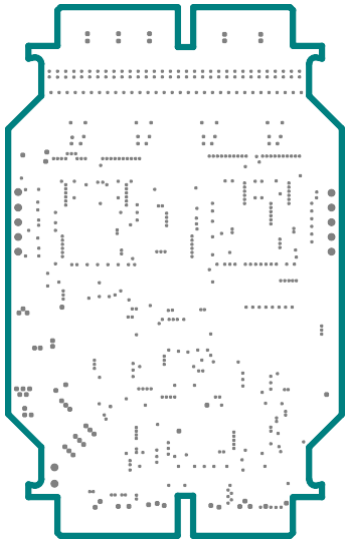

IDL
Instrumentation
Development
Lab
mRICH Daughtercard
IDL_19_004, 2019-04
YALL QSV

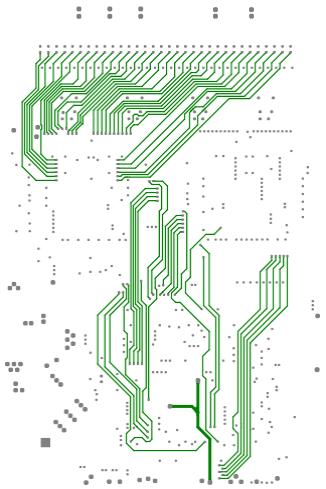


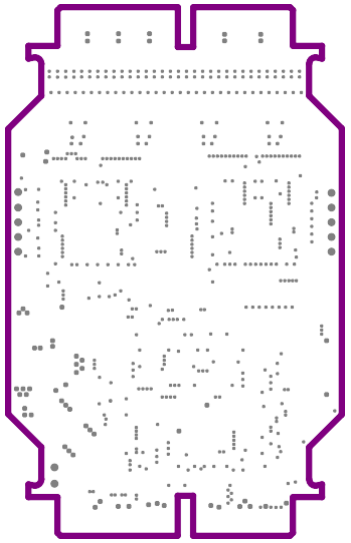


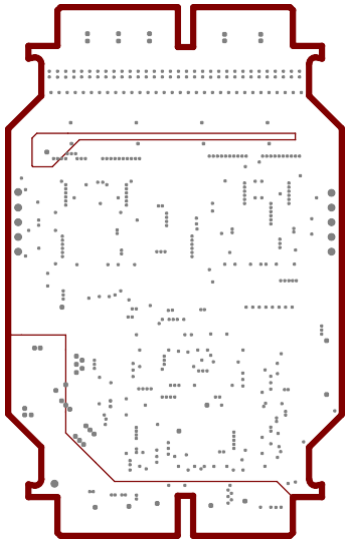


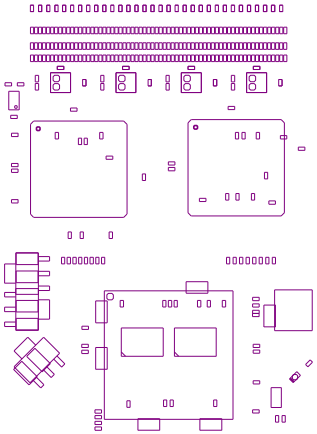


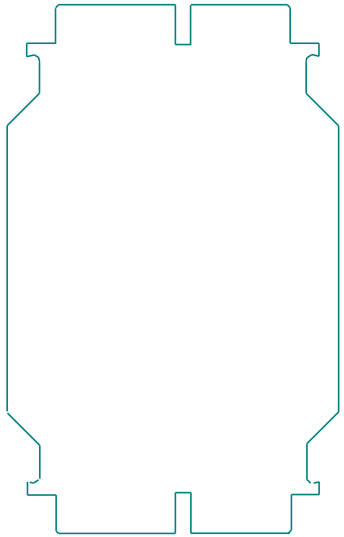


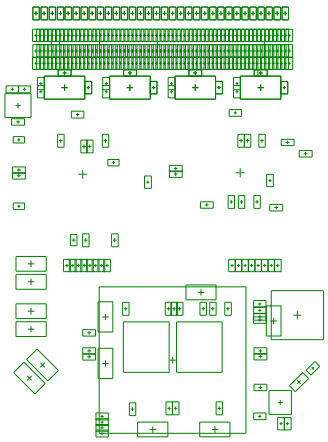


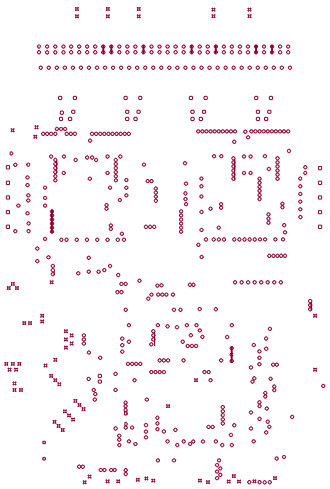












Notes:

1. Board shall be fabricated - performace class II as per IPC-6011 and IPC6012
2. PCB manufacturer logo, P/N, revision and/or date code of manufacturing
   shall be printed in top solder mask (not over pcb traces, allowed over copper plane).
   The date code shall be in the format: "WWYY" where WW=week and YY= year, max height 0.15 inches
3. Material: high temperature FR4 class epoxy glass rated UL94V-0. UL symbol and rating shall be marked farside
   35um copper for external layers and 18um for all internal layers
   Must be RoHS compliant and survive a lead-free assembly max reflow of 260 deg C (5 passes)
   Td rating: >340 deg C
   Tg = 150 deg C (min)
4. Solder mask: SMOBC per IPC-SM-840C, class T must be Rohs compliant, 0.001" max measured over bare copper plating,
   must clear all lands as indicated on gerber solder mask layers, color= GREEN
5. Finish: electro-less nickel immersion gold (ENIG), 0.05-0.125um Au over 3-6um Ni - over bare copper only
6. Solderability test: Category 2 of J-STD-003
7. Finished boards shall not have nicks, scratches, voids, exposed copper, poor plating or misdrilled holes
8. All holes sizes are after plating
9. PCB manufacturer may add copper thieving as needed to improve manufacturability,
   thieving to be 0.030" round pads at 0.050" spacing.
   Thieving will have a minimum of 0.100" clearance from existing copper and should not be placed under surface mounted devices
10. All via connections to power and ground planes are solid
11. All unconnected pads on inner signal layers are removed
12. All finished boards are to be 100% electrically tested
13. Unless otherwise indicated, all linear toleracnes shall be XX.X +/-0.2mm and XX.XX +/- 0.1mm
14. Gerber file GM14 shows board outline (milling line)
15. Table 1 shows Layer stack details
16. Gerber file GM4 shows the chamfer outline. Chamfer both sides 30 degrees as per figure 1
17. All Vias must be tented with soldermask.

Additional notes:

A1. Finished board thickness = 61.2 mils +/- 0.1mil; measured over top/bottom copper and solder mask

Table 1: Layer Stack Details for IDL_19_004 Rev.B (Imperial Units)

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,40mil	3,5	
3	Top Layer	Copper	1,40mil		
4	Dielectric 1	FR-4	10,00mil	4,2	
5	GND	Copper	1,42mil		
6	Dielectric 2	FR-4	5,00mil	4,2	
7	AUX Route Horz	Copper	1,42mil		
8	Dielectric 5	FR-4	5,00mil	4,2	
9	2.5VF	Copper	1,42mil		
10	Dielectric 9		10,00mil	4,2	
11	AUX Route Vert	Copper	1,42mil		
12	Dielectric 3	FR-4	10,00mil	4,2	
13	1.2V	Copper	1,42mil		
14	Dielectric 10		5,00mil	4,2	
15	2.5V	Copper	1,42mil		
16	Dielectric 8	FR-4	10,00mil	4,2	
17	Bottom Layer	Copper	1,40mil		
18	Bottom Solder	Solder Resist	0,40mil	3,5	
19	Bottom Overlay				

Figure 1: Board edge chamfer specifications. Chamfer location specified in gerber file GM4.

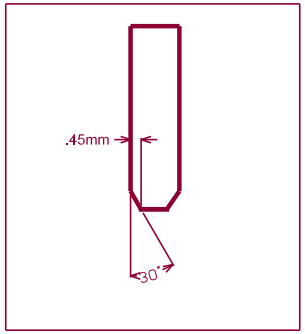
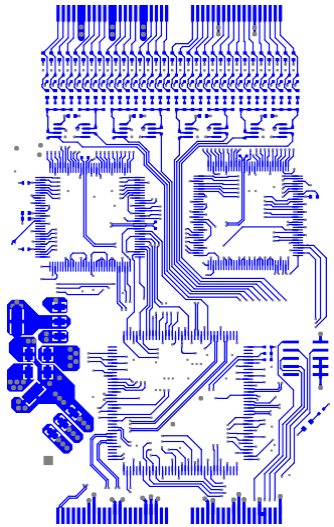
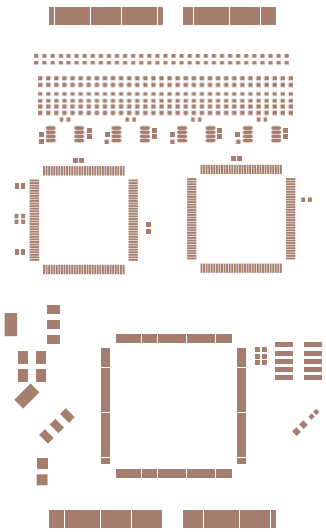
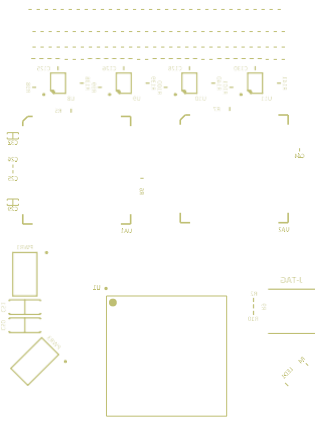


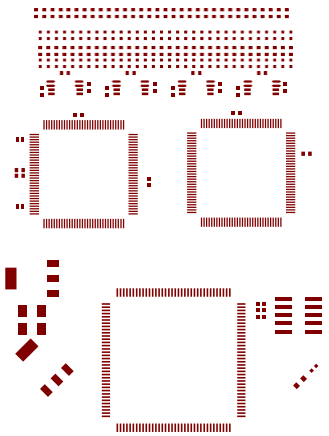
Table 2: NC Drill Details for IDL_19_004 Rev.B

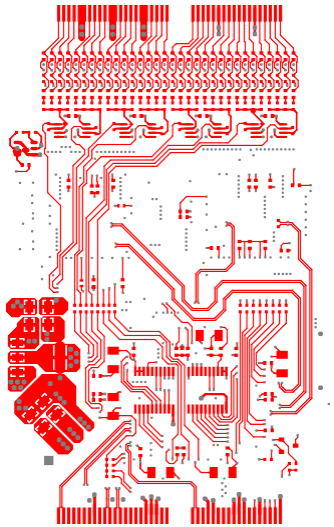
Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Description	Hole Tolerance (+)	Hole Tolerance (-)
☼	2	0,900mm (35,43mil)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
□	10	0,889mm (35,00mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	(Mixed)			
○	26	0,200mm (7,87mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v50h20m0mx0			
⌑	66	0,400mm (15,75mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v75h40m0mx0			
◌	484	0,150mm (5,91mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	(Mixed)			
	588 Total										

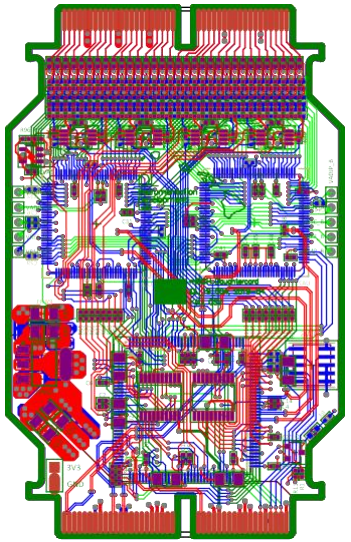












Notes:

1. Board shall be fabricated - performace class II as per IPC-6011 and IPC6012
2. PCB manufacturer logo, P/N, revision and/or date code of manufacturing
   shall be printed in top solder mask (not over pcb traces, allowed over copper plane).
   The date code shall be in the format: "WWYY" where WW=week and YY= year, max height 0.15 inches
3. Material: high temperature FR4 class epoxy glass rated UL94V-0. UL symbol and rating shall be marked farside
   35um copper for external layers and 18um for all internal layers
   Must be RoHS compliant and survive a lead-free assembly max reflow of 260 deg C (5 passes)
   Td rating: >340 deg C
   Tg = 150 deg C (min)
4. Solder mask: SMOBC per IPC-SM-840C, class T must be Rohs compliant, 0.001" max measured over bare copper plating,
   must clear all lands as indicated on gerber solder mask layers, color= GREEN
5. Finish: electro-less nickel immersion gold (ENIG), 0.05-0.125um Au over 3-6um Ni - over bare copper only
6. Solderability test: Category 2 of J-STD-003
7. Finished boards shall not have nicks, scratches, voids, exposed copper, poor plating or misdrilled holes
8. All holes sizes are after plating
9. PCB manufacturer may add copper thieving as needed to improve manufacturability,
   thieving to be 0.030" round pads at 0.050" spacing.
   Thieving will have a minimum of 0.100" clearance from existing copper and should not be placed under surface mounted devices
10. All via connections to power and ground planes are solid
11. All unconnected pads on inner signal layers are removed
12. All finished boards are to be 100% electrically tested
13. Unless otherwise indicated, all linear toleracnes shall be XX.X +/-0.2mm and XX.XX +/- 0.1mm
14. Gerber file GM14 shows board outline (milling line)
15. Table 1 shows Layer stack details
16. Gerber file GM4 shows the chamfer outline. Chamfer both sides 30 degrees as per figure 1
17. All Vias must be tented with soldermask.

Additional notes:

A1. Finished board thickness = 61.2 mils +/- 0.1mil; measured over top/bottom copper and solder mask

Table 1: Layer Stack Details for IDL_19_004 Rev.B (Imperial Units)

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,40mil	3,5	
3	Top Layer	Copper	1,40mil		
4	Dielectric 1	FR-4	10,00mil	4,2	
5	GND	Copper	1,42mil		
6	Dielectric 2	FR-4	5,00mil	4,2	
7	AUX Route Horz	Copper	1,42mil		
8	Dielectric 5	FR-4	5,00mil	4,2	
9	2.5VF	Copper	1,42mil		
10	Dielectric 9		10,00mil	4,2	
11	AUX Route Vert	Copper	1,42mil		
12	Dielectric 3	FR-4	10,00mil	4,2	
13	1.2V	Copper	1,42mil		
14	Dielectric 10		5,00mil	4,2	
15	2.5V	Copper	1,42mil		
16	Dielectric 8	FR-4	10,00mil	4,2	
17	Bottom Layer	Copper	1,40mil		
18	Bottom Solder	Solder Resist	0,40mil	3,5	
19	Bottom Overlay				

Figure 1: Board edge chamfer specifications. Chamfer location specified in gerber file GM4.

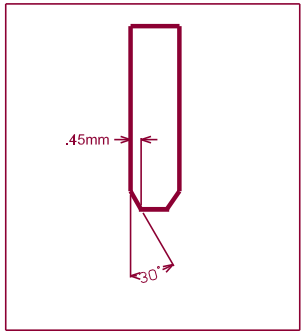


Table 2: NC Drill Details for IDL_19_004 Rev.B

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Description	Hole Tolerance (+)	Hole Tolerance (-)
☼	2	0,900mm (35,43mil)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)			
□	10	0,889mm (35,00mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	(Mixed)			
○	26	0,200mm (7,87mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v50h20m0mx0			
⌑	66	0,400mm (15,75mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v75h40m0mx0			
○	484	0,150mm (5,91mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	(Mixed)			
	588 Total										