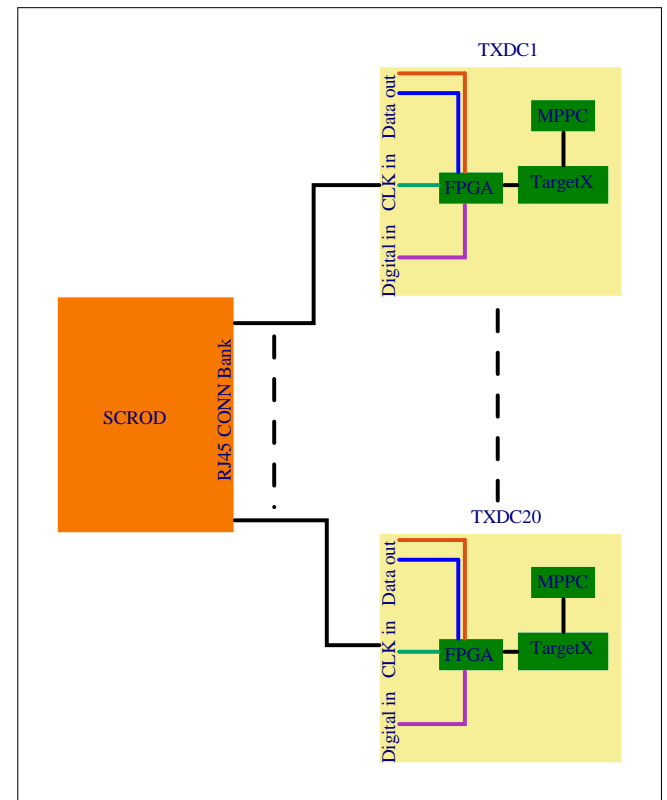
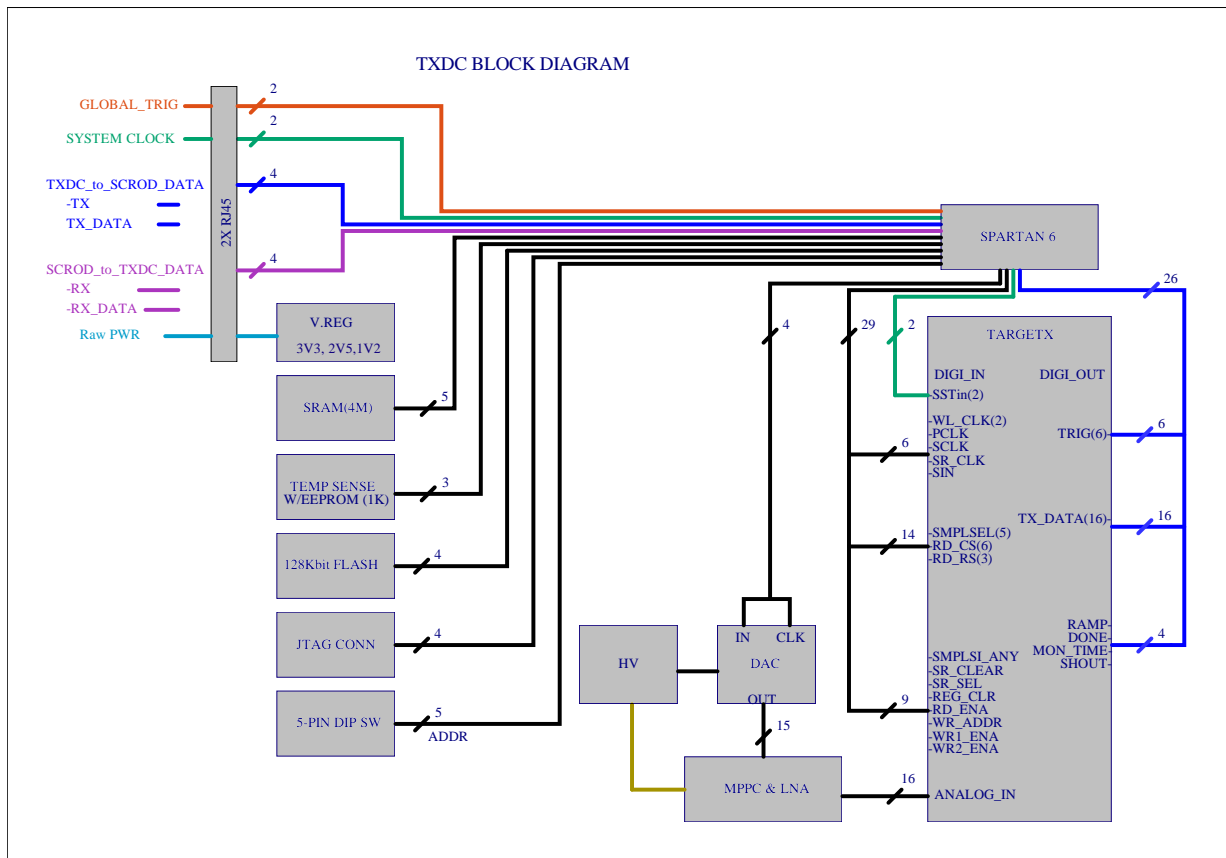


BMD OVERVIEW DIAGRAM (New version is reconfigured for the tracker planes on the HMB)





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**High Energy Physics Group  
Instrumentation Development Laboratory**  
2505 Correa Road, Honolulu, HI 96822

**Production Documentation for:**

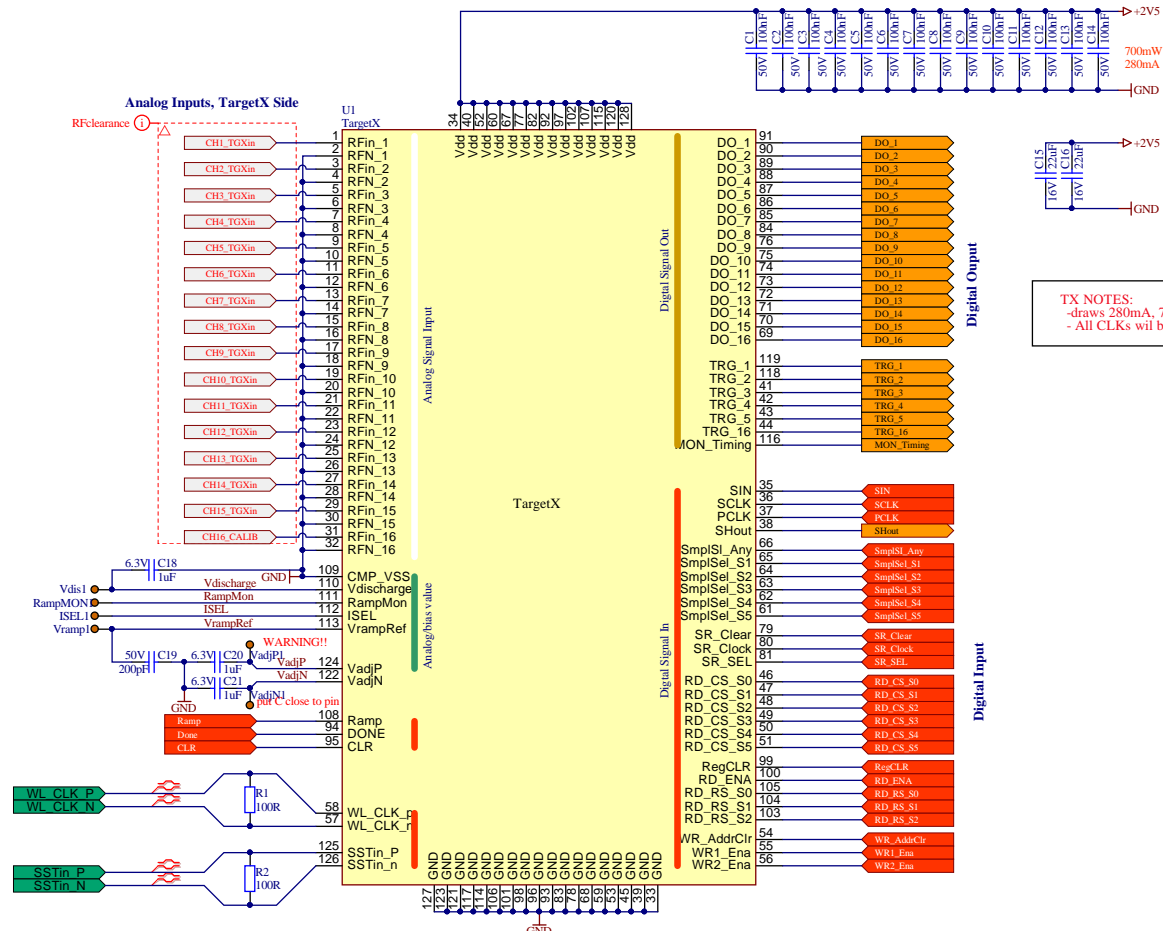
**Project Name:** BMD\_RevB  
**Board Name:** BMD Center Daughtercard  
**IDL num:** IDL\_18\_014  
**Revision:** B  
**Variant:** [No Variations]

**Designer:** KPL/PO  
**Drawn by:** KPL/PO  
**Approved by:** Gary S. Varner

High Energy Physics Group, Instrumentation Development Lab	Designer: KPL/PO	IDLAB design #: IDL_18_014
Project name: <b>BMD_RevB</b>	Drawn By: KPL/PO	Revision: B
Board name: <b>BMD Center Daughtercard</b>	Approved By: Gary S. Varner	Variant: [No Variations]
	Modif. Date: 7/6/2018	Sheet 1 of 3

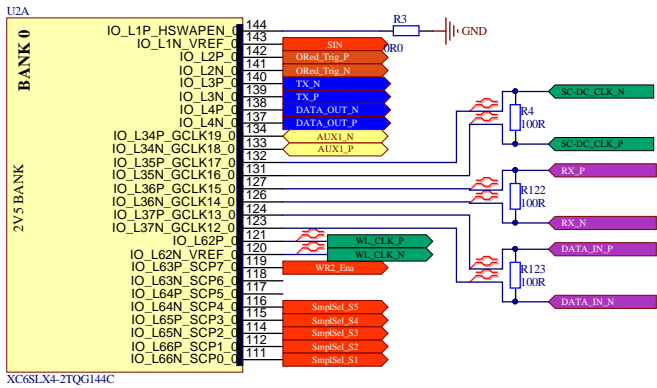


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**TX NOTES:**  
 - draws 280mA, 700mW  
 - All CLKs will be generated on FPGA

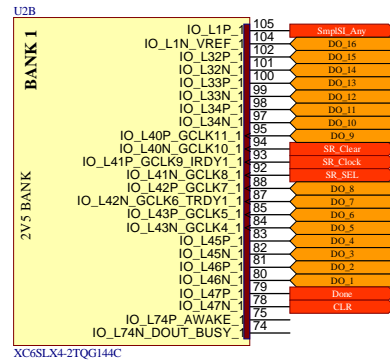
Xilinx Spartan 6(XC6SLX4-2TQG144C)



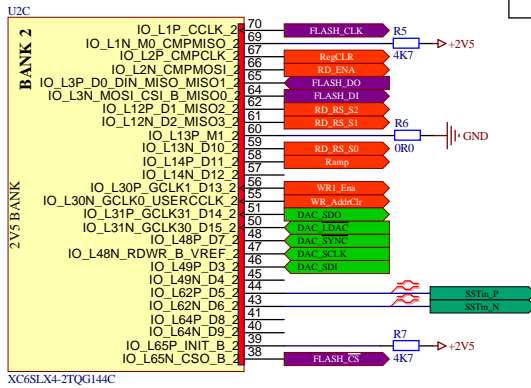
To match the incoming signals on the SCROD Rev A5, we had to permute some of the signals on the oscilloscope DC side. (note that this should now be consistent with the oscilloscope DC's uct).

AUX1\_N (133->134)  
 AUX1\_P (134 -> 133)  
 TX\_N (139->140)  
 TX\_P (140->139)  
 SC-DC\_CLK\_N (131->132)  
 SC-DC\_CLK\_P (132->131)  
 DATA\_OUT\_N  
 DATA\_OUT\_P(A3 ->A6)

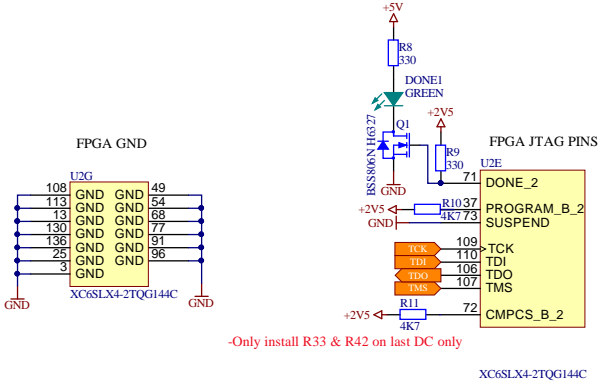
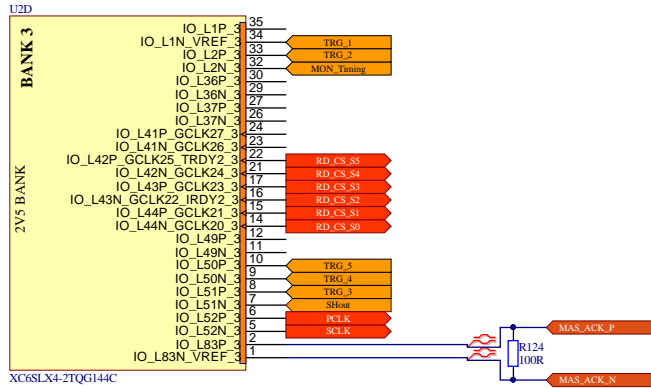
Tommy Lam  
 7/6/2018



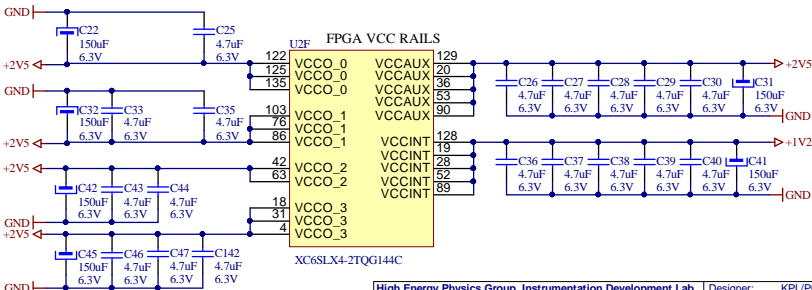
FPGA setup notes:  
 -FPGA set to master mode (pin 60 to GND 69 set to VCCO3)  
 -FPGA set serially for JTAG programming  
 -FPGA set to load image from flash memory

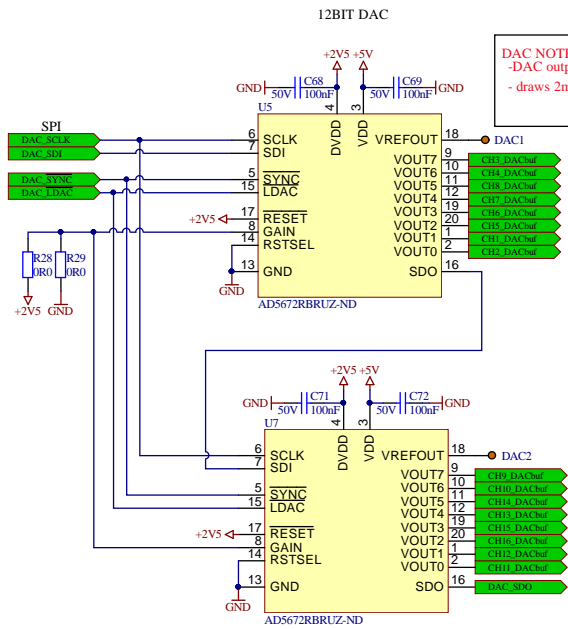
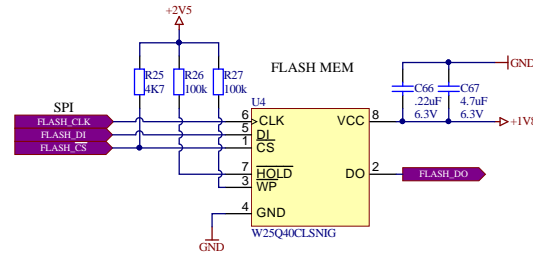
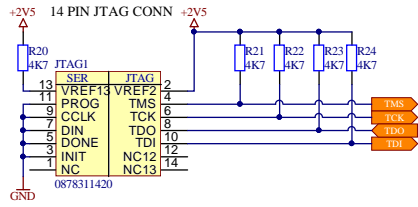


TRG\_16 not used

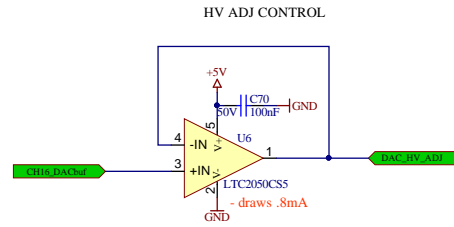


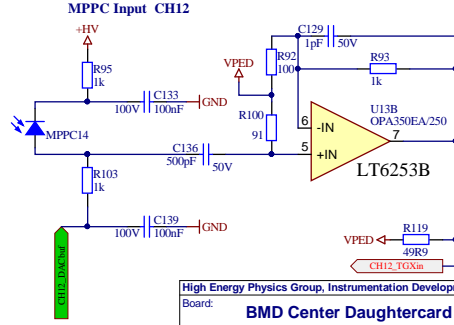
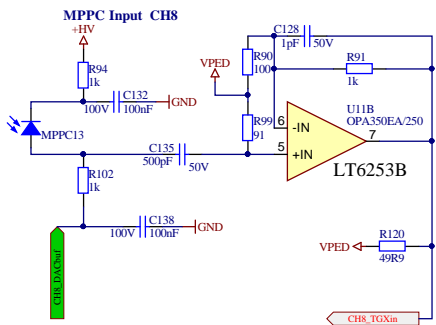
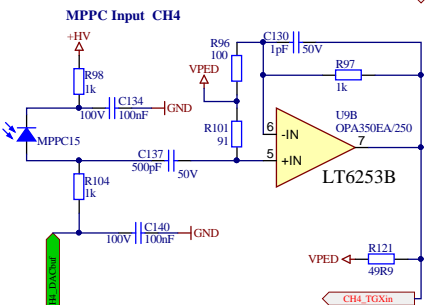
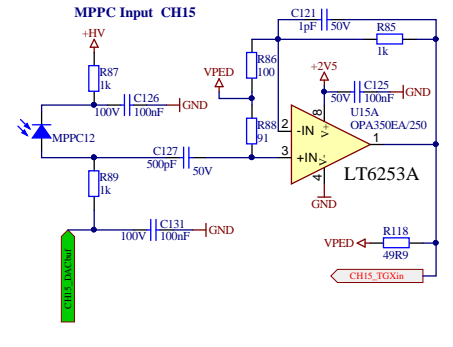
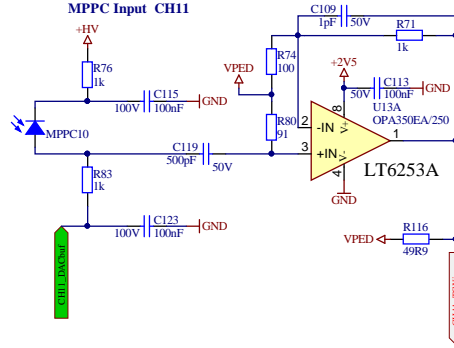
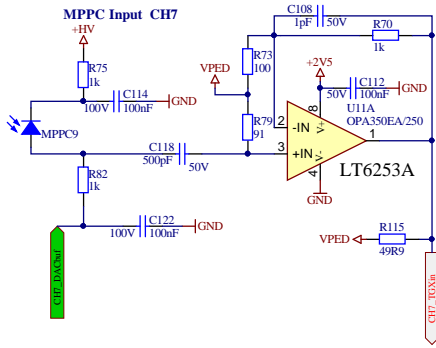
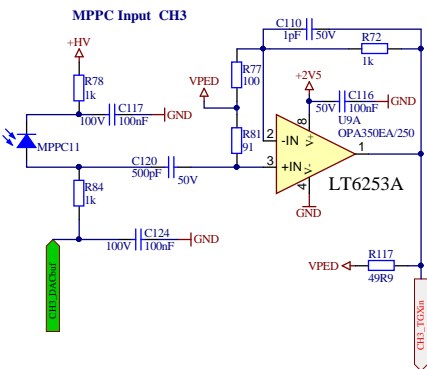
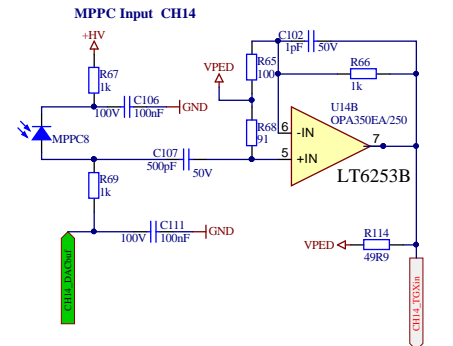
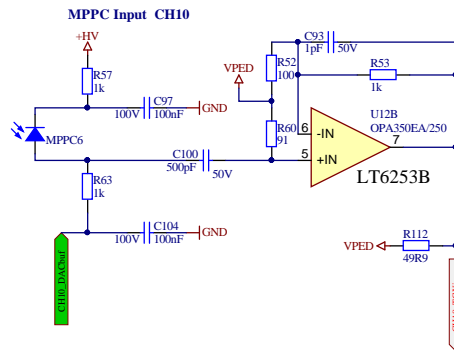
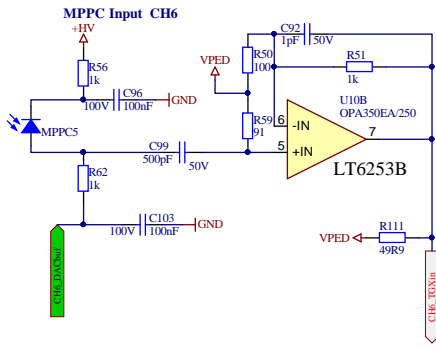
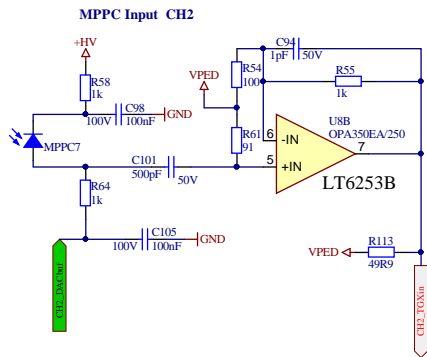
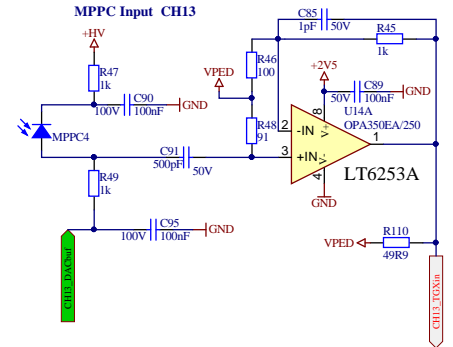
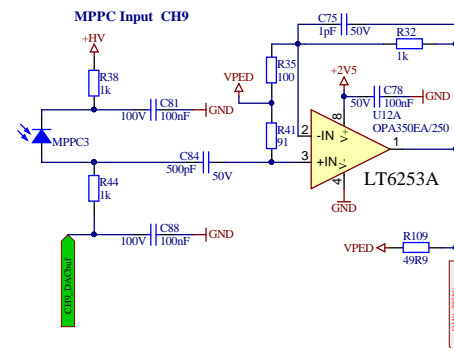
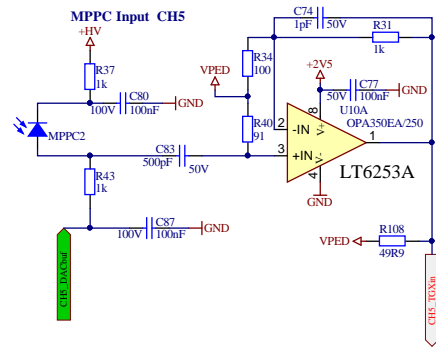
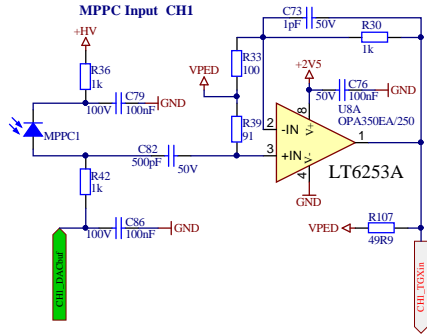
-Only install R33 & R42 on last DC only

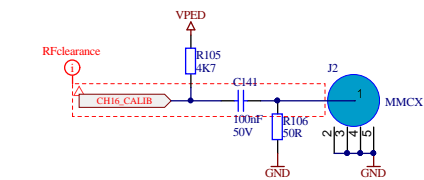




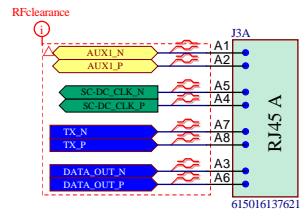
**DAC NOTES:**  
 -DAC output: 5V install R?, 2V5 install R?  
 - draws 2mA, 40mA SC current, 15mA output







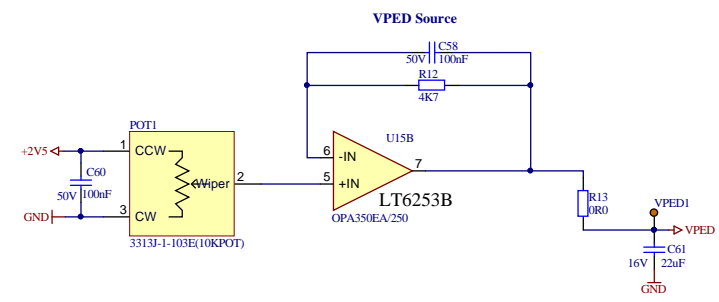
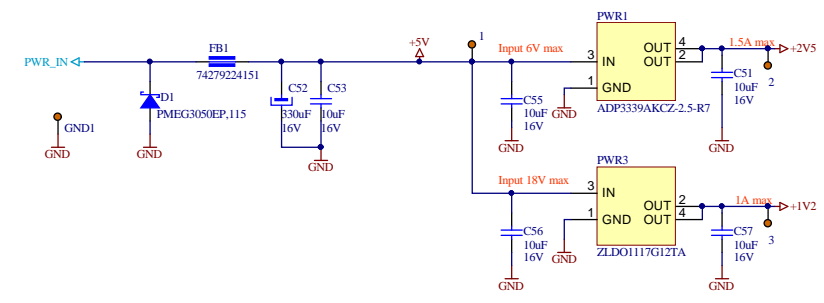
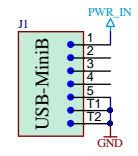
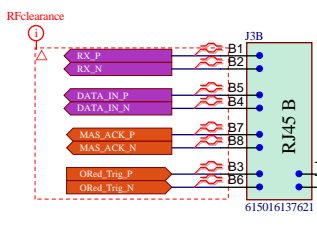
**INPUT CONNECTOR**



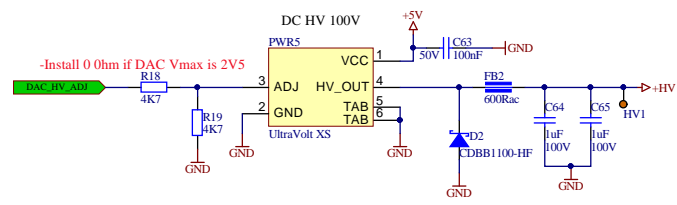
To match the incoming signals on the SCROD Rev A5, we had to permute some of the signals on the hodoscope DC side. (note that this should now be consistent with the hodoscope DC's ucf).

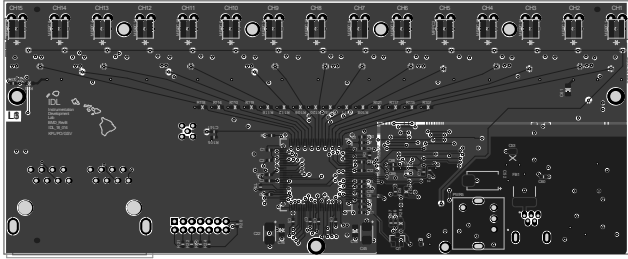
AUX1\_N (A2->A1)  
 AUX1\_P (A1->A2)  
 TX\_N (A8->A7)  
 TX\_P (A7->A8)  
 SC-DC\_CLK\_N (A4->A5)  
 SC-DC\_CLK\_P (A5->A4)  
 DATA\_OUT\_N (A6->A3)  
 DATA\_OUT\_P (A3->A6)

Tommy Lam  
 7/6/2018



**CALIB VPED NOTES:**  
 -VPED = 0V8 at up to 500mA  
 -VPED = .8(1+(R66/R67))





Designer: KPL/PO	Revision: B	File: BMD_RevB_PCB.PcbDoc	Sheet 1 of 1
Drawn By: KPL/PO	Modif. Date: Date	Variant: [No Variations]	ASSEMBLY
Approved By: Gary S. Varner	Print Date: 7/6/2018	Signature:	Size: A3 H
Title: Multilayer Composite Print Instrumentation Development Laboratory High Energy Physics Group University of Hawaii at Manoa			
ID: <b>IDL_18_014</b>	Code: <b>ASSEMBLY</b>	File: BMD_RevB_PCB.PcbDoc	Sheet 1 of 1

Designer: KPL/PO	Revision: B	File: BMD_RevB_PCB.PcbDoc	Sheet 1 of 1	Code: <b>IDL_18_014</b>
Drawn By: KPL/PO	Modif. Date: Date	Variant: [No Variations]	ASSEMBLY	ID: <b>BMD Center Daughtercard</b>
Approved By: Gary S. Varner	Print Date: 7/6/2018	Signature:	Size: A3 H	
Title: Multilayer Composite Print Instrumentation Development Laboratory High Energy Physics Group University of Hawaii at Manoa				