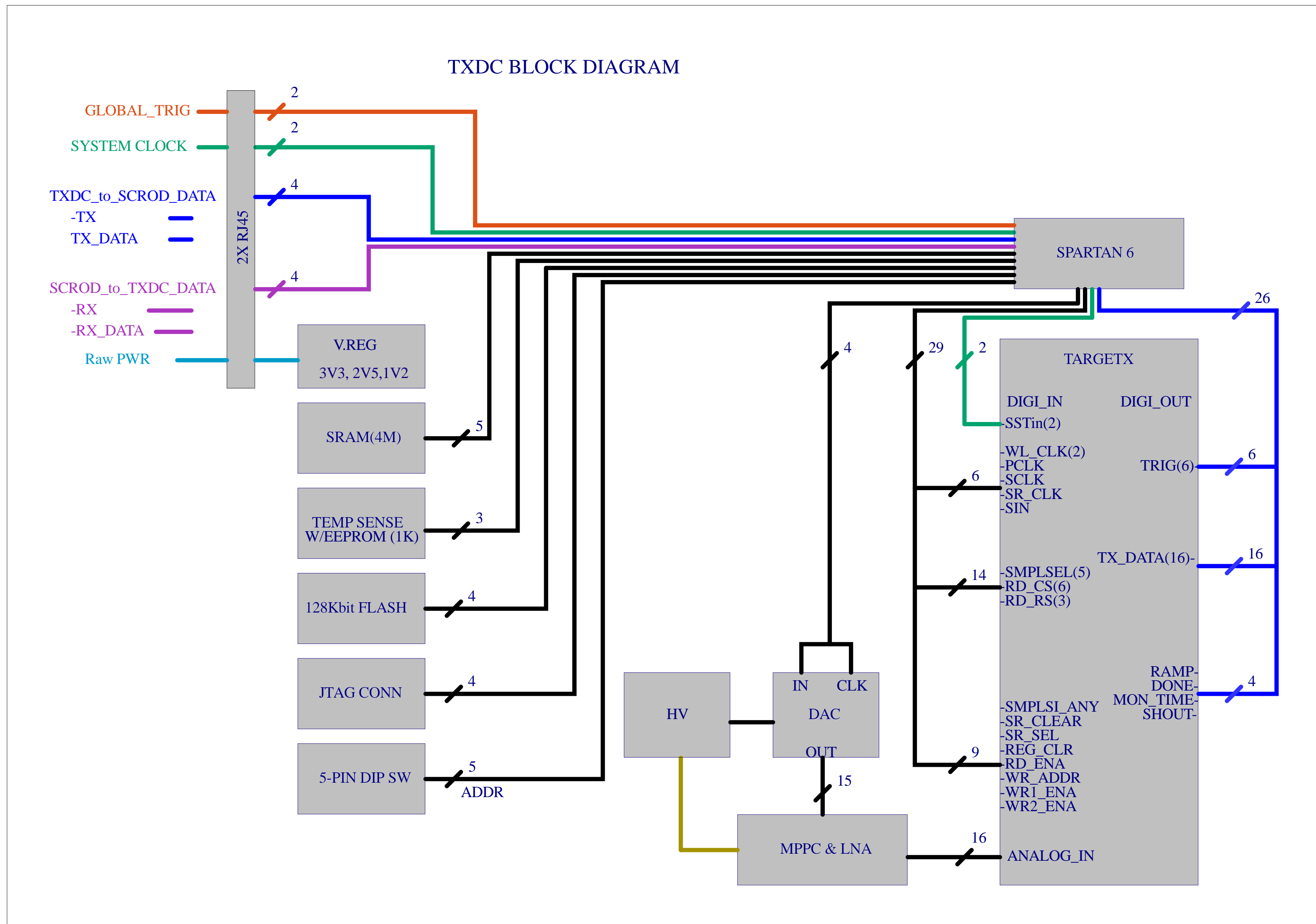
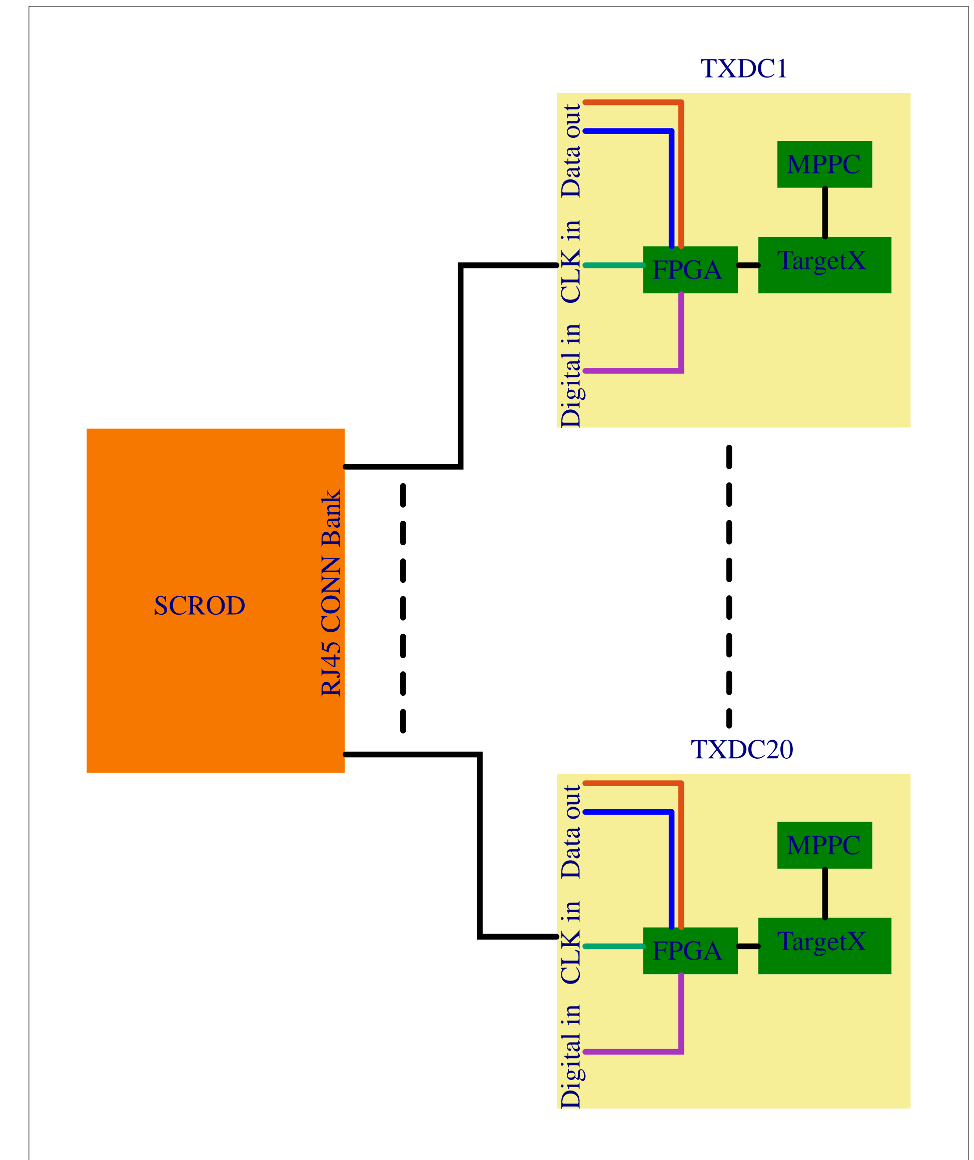
BMD OVERVIEW DIAGRAM (New version is reconfigured for the tracker planes on the HMB)





High Energy Physics Group, Instrumentation Development Lab	Designer: KPL/PO	IDLAB design #: IDL_18_014
Board: **BMD Center Daughtercard**	Drawn By: KPL/PO	Revision: B
	Approved By: Gary S. Varner	Variant: [No Variations]
Sheet Title: **Block Diagram**		Modif. Date: 4/4/2018
		Sheet 1 of 6

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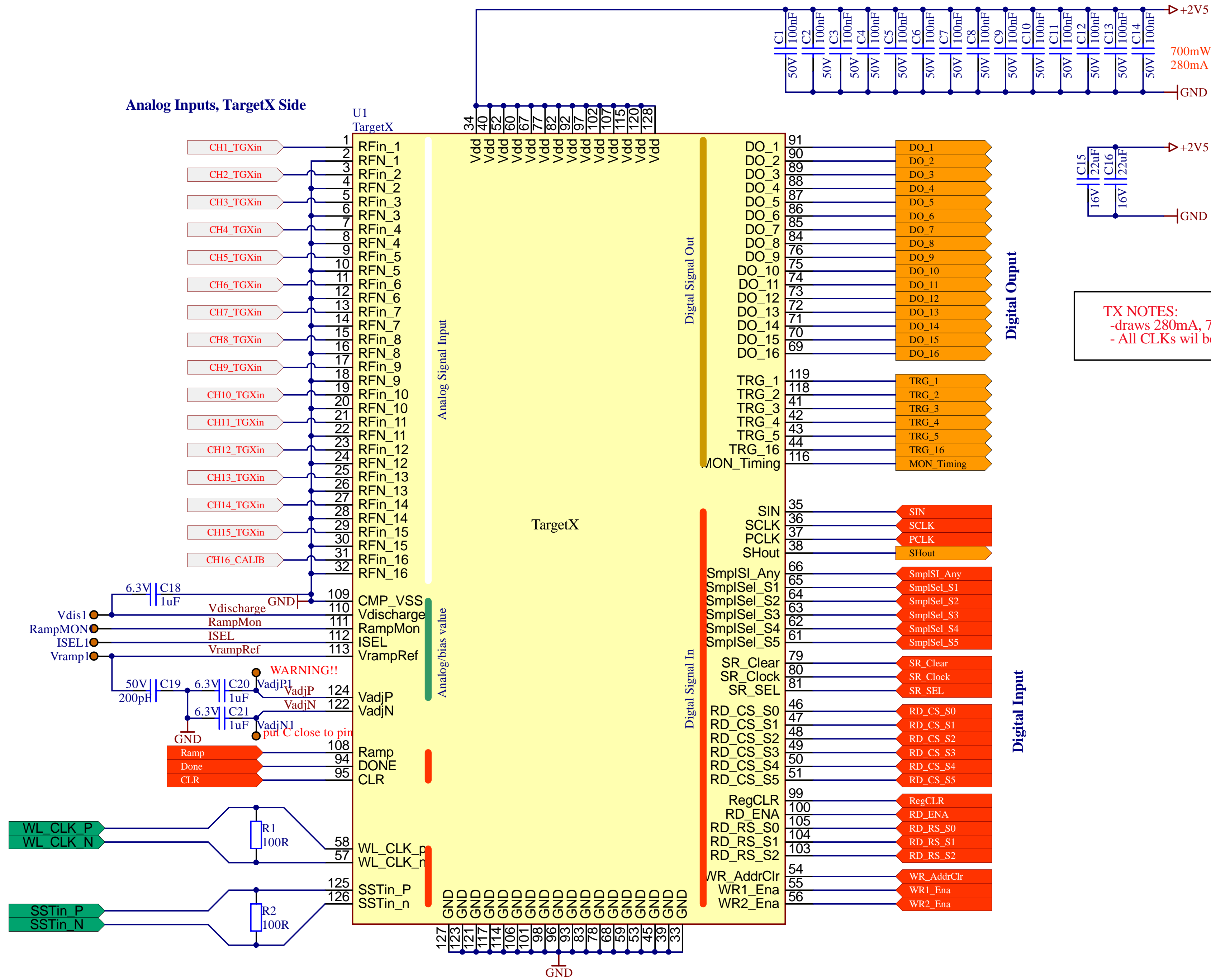
High Energy Physics Group
Instrumentation Development Laboratory
2505 Correa Road, Honolulu, HI 96822

Production Documentation for:

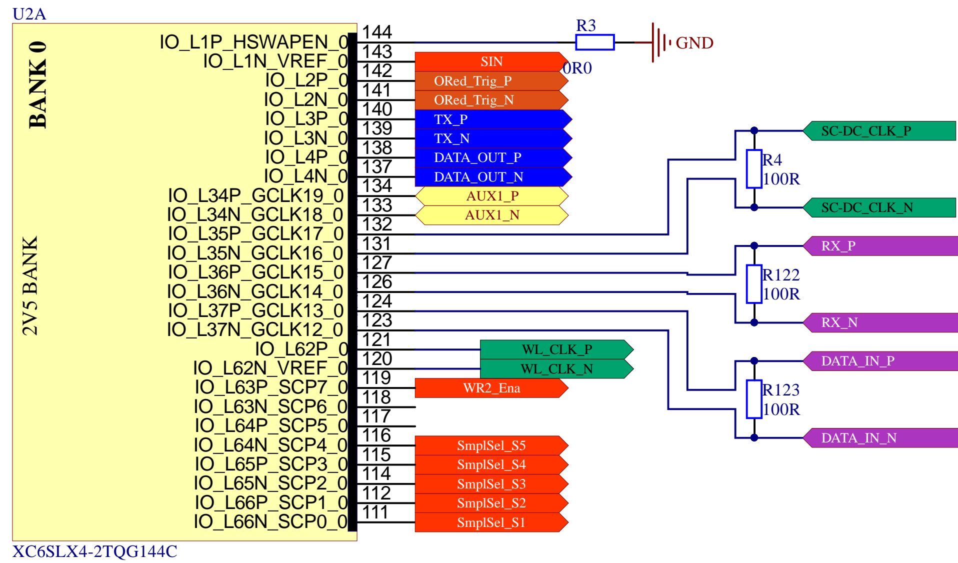
Project Name: BMD_RevB
Board Name: BMD Center Daughtercard
IDL num: IDL_18_014
Revision: B
Variant: [No Variations]

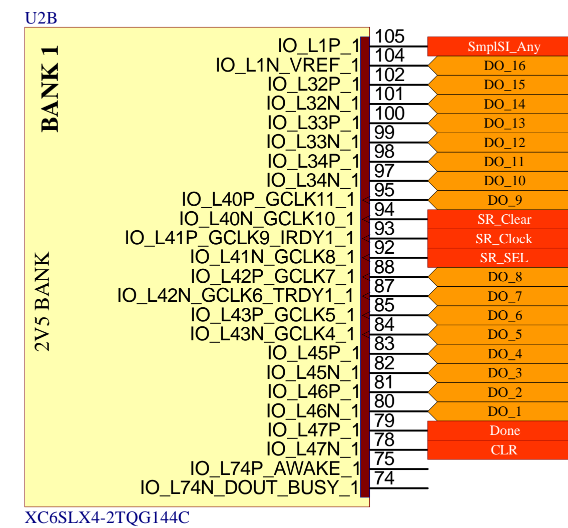
Designer: KPL/PO
Drawn by: KPL/PO
Approved by: Gary S. Varner



High Energy Physics Group, Instrumentation Development Lab	Designer: KPL/PO	IDLAB design #: IDL_18_014
Board: **BMD Center Daughtercard**	Drawn By: KPL/PO	Revision: B
	Approved By: Gary S. Varner	Variant: [No Variations]
Sheet Title: **TargetX**		Modif. Date: 4/6/2018
		Sheet 2 of 6

Xilinx Spartan 6(XC6SLX4-2TQG144C)

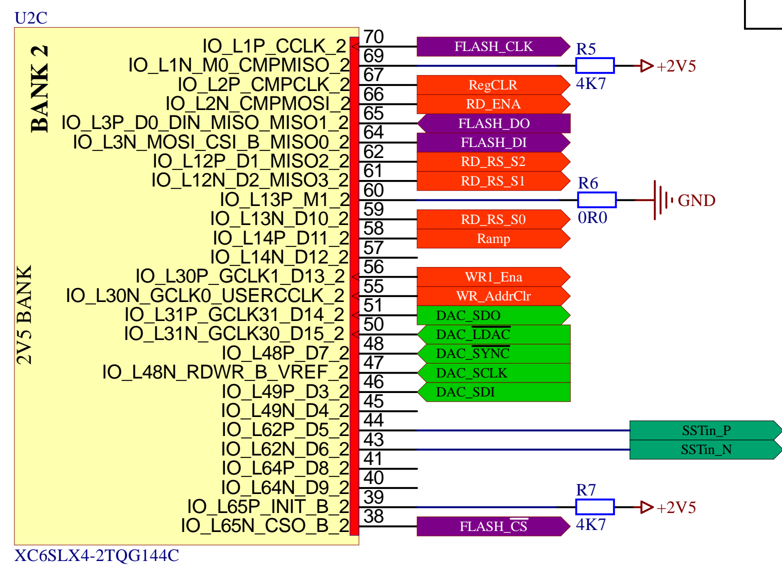


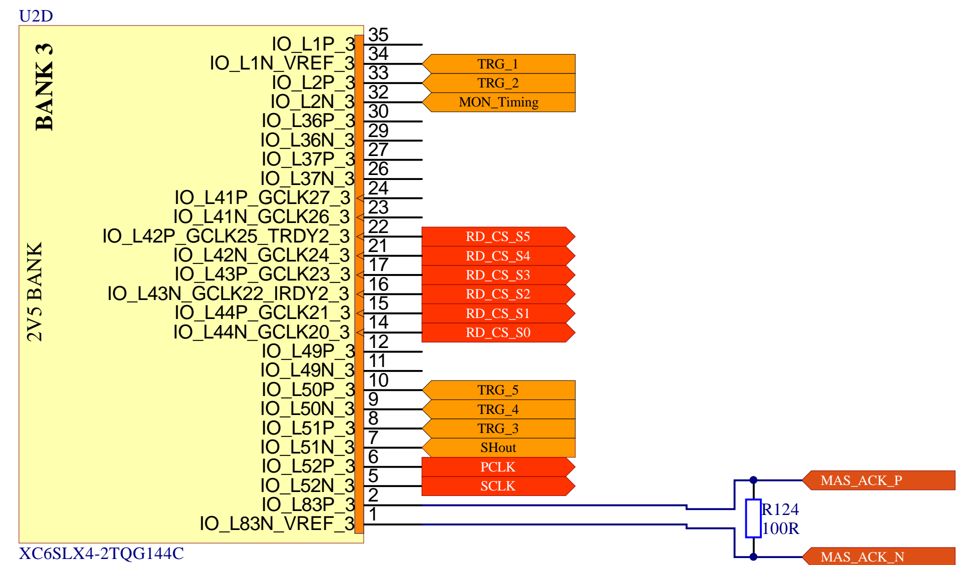


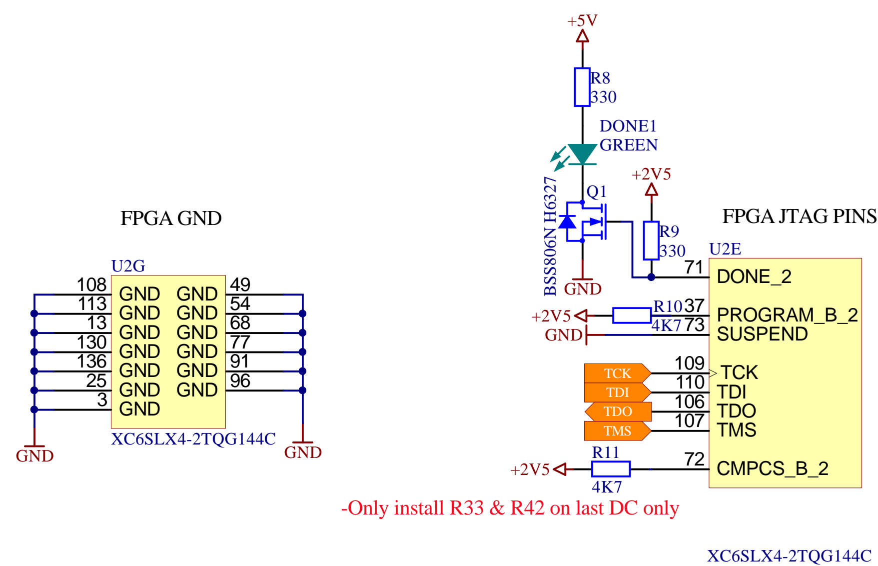
FPGA setup notes:
- -FPGA set to master mode (pin 60 to GND 69 set to VCCO3)
- -FPGA set serially for JTAG programing
- -FPGA set to load image from flash memory

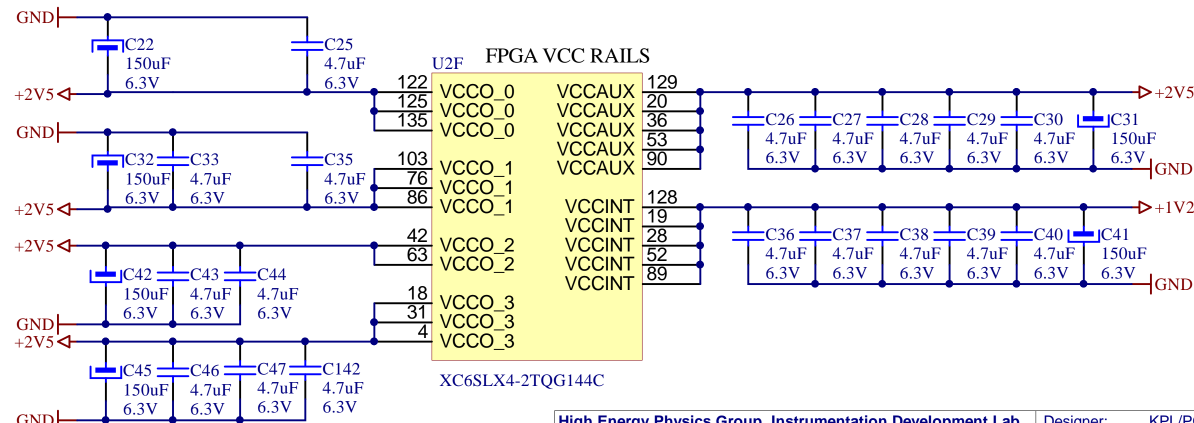
TRG_16 not used

TRG_16









High Energy Physics Group, Instrumentation Development Lab	Designer: KPL/PO	IDLAB design #: IDL_18_014
Board: **BMD Center Daughtercard**	Drawn By: KPL/PO	Revision: B
	Approved By: Gary S. Varner	Variant: [No Variations]
Sheet Title: **FPGA**		Modif. Date: 4/14/2018
		Sheet 3 of 6

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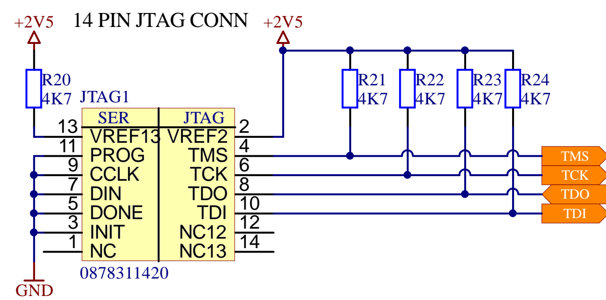
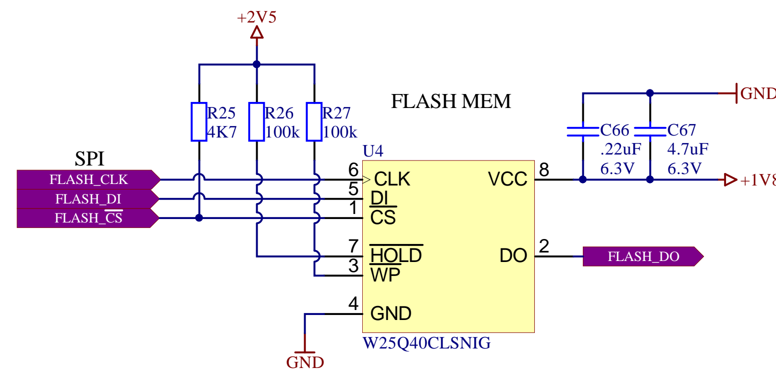
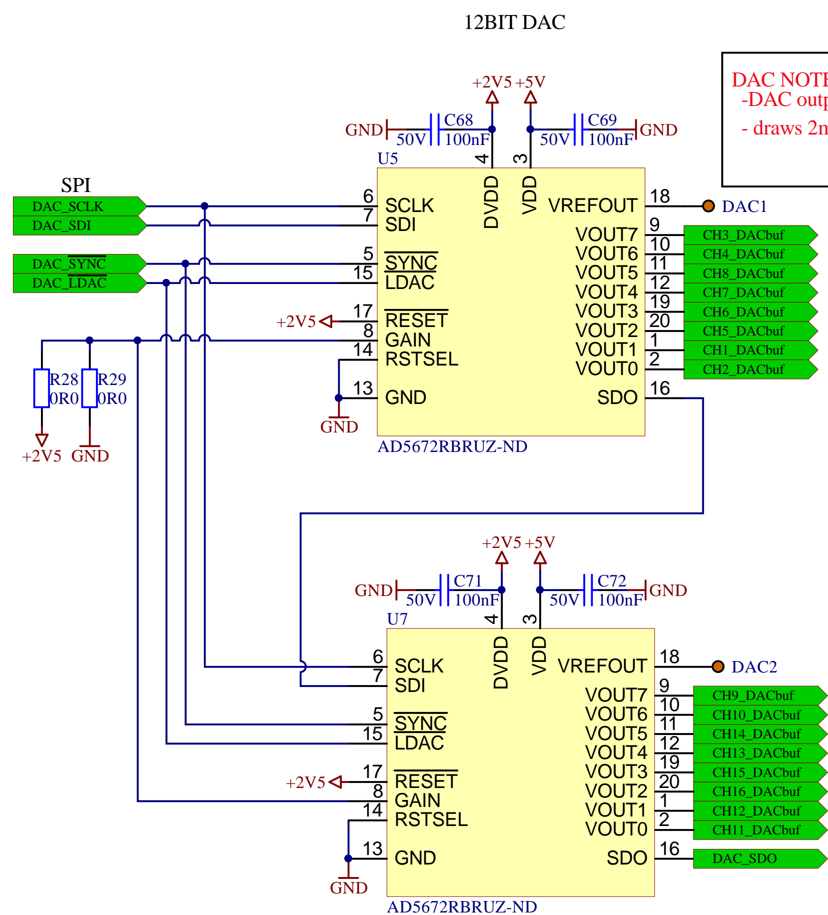
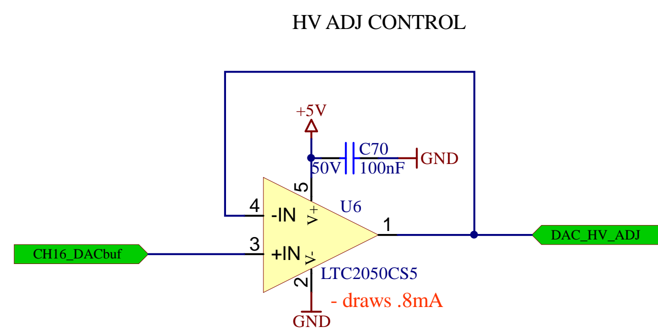


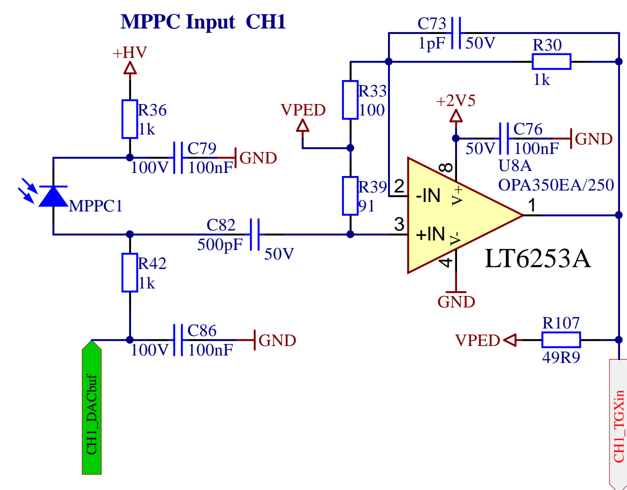


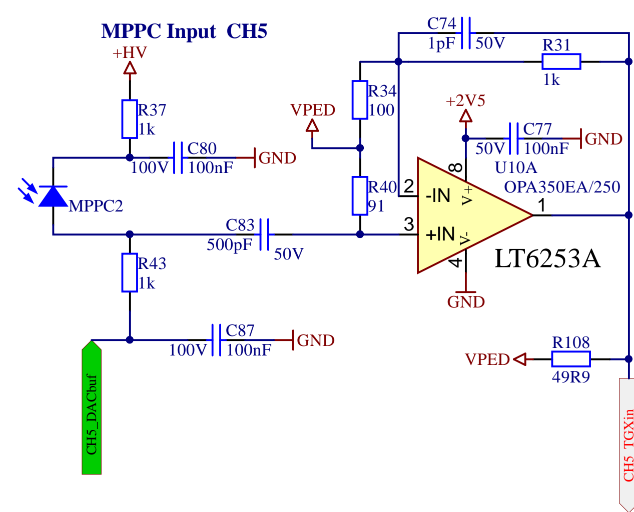
DAC NOTES:
-DAC output: 5V install R?, 2V5 install R?
- draws 2mA, 40mA SC current, 15mA output

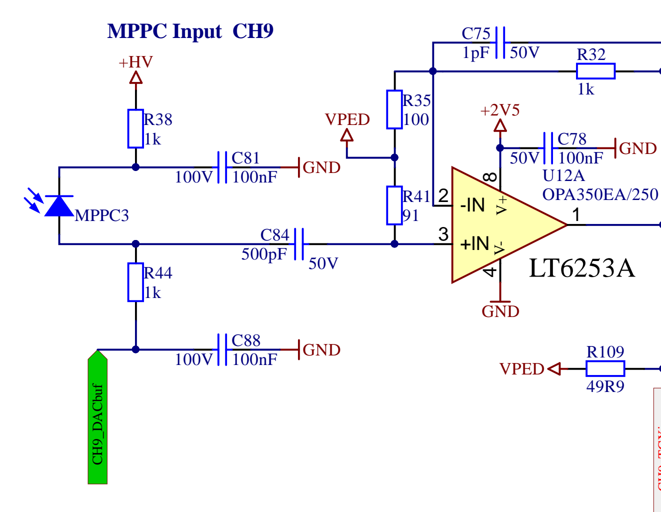


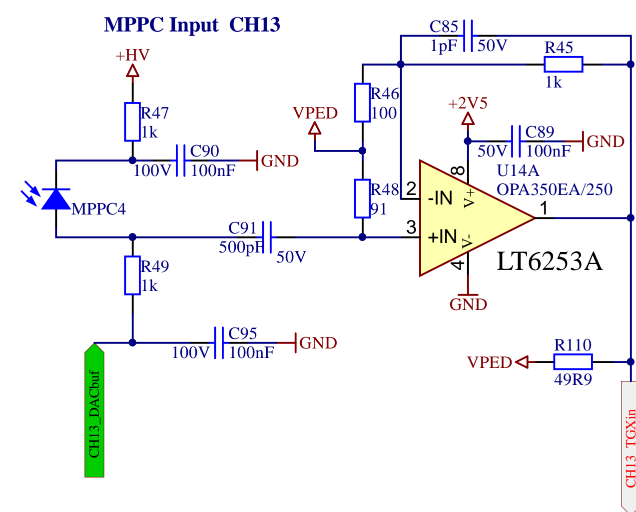


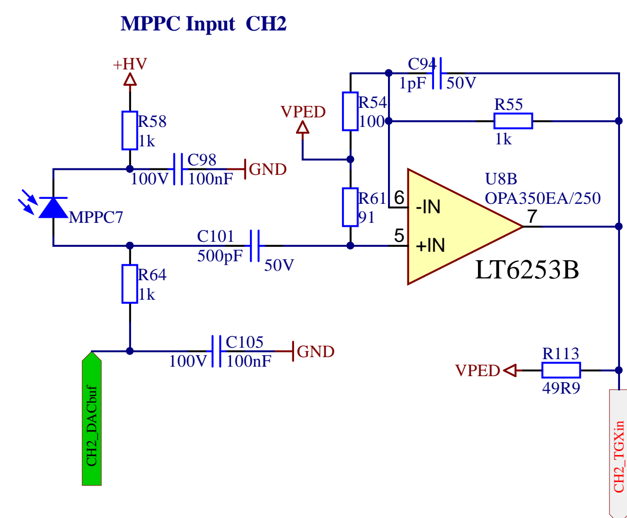
High Energy Physics Group, Instrumentation Development Lab	Designer: KPL/PO	IDLAB design #: IDL_18_014	UNIVERSITY of HAWAIʻI® MĀNOA
Board: BMD Center Daughtercard	Drawn By: KPL/PO	Revision: B	
	Approved By: Gary S. Varner	Variant: [No Variations]	
Sheet Title: FPGA2		Modif. Date: 4/5/2018	
		Sheet 4 of 6	

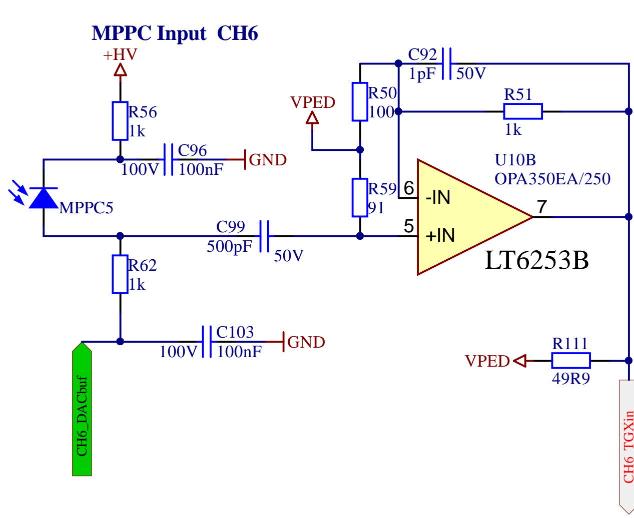


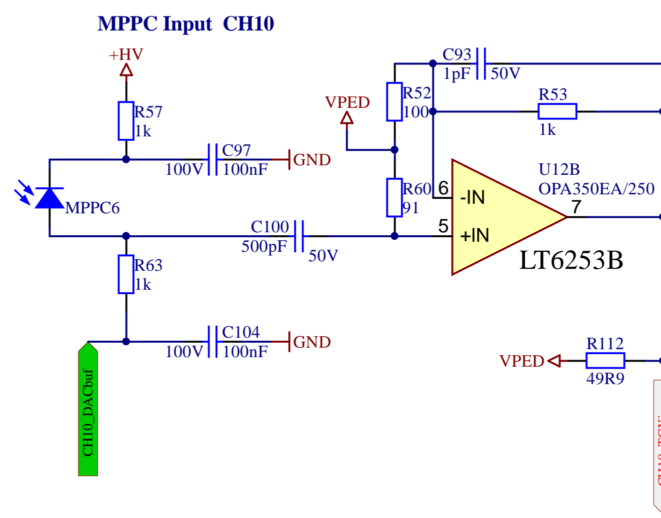


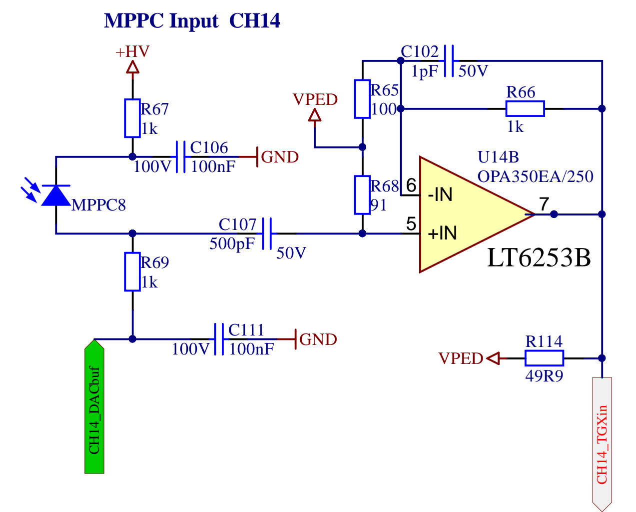


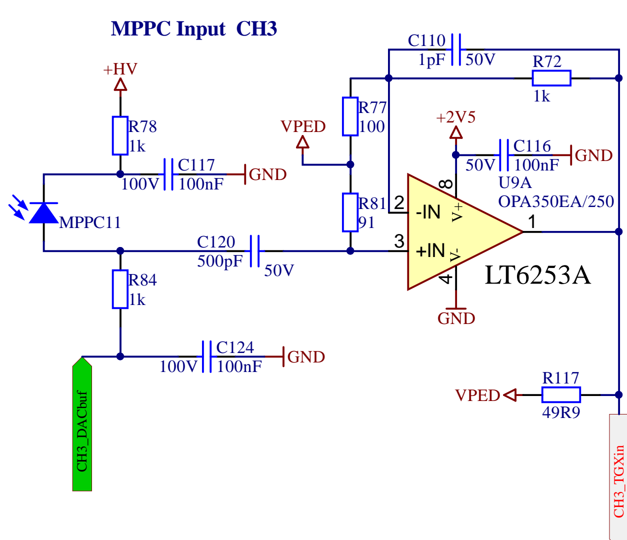


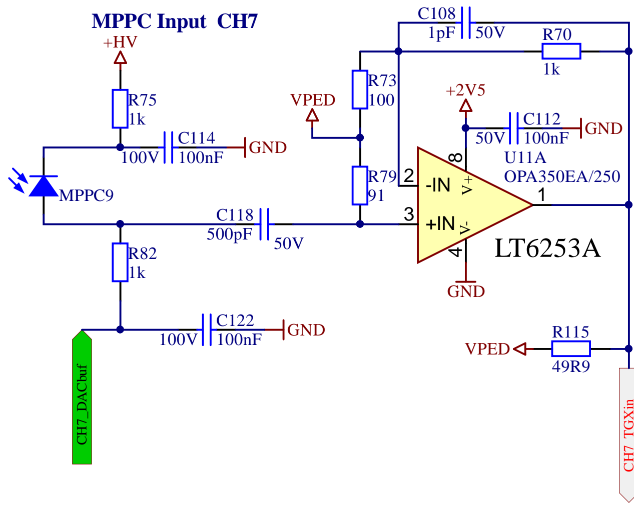


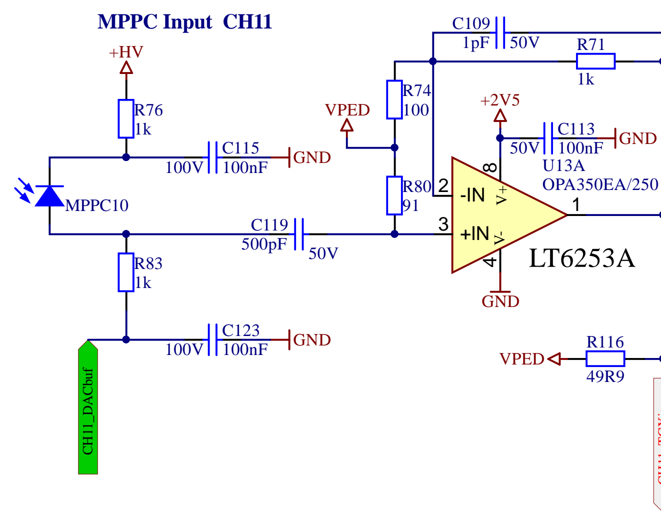


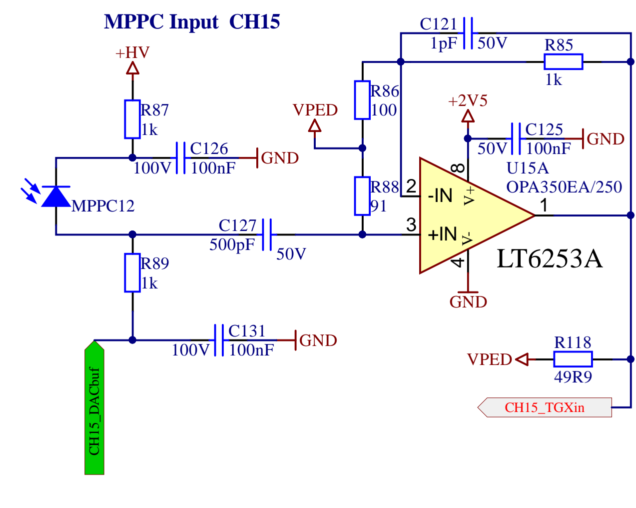


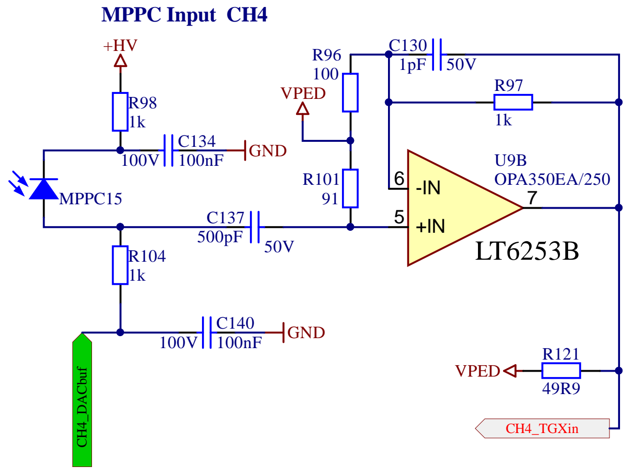


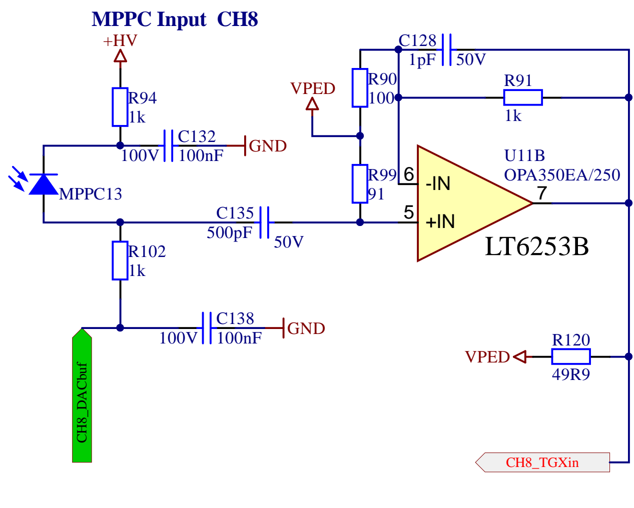


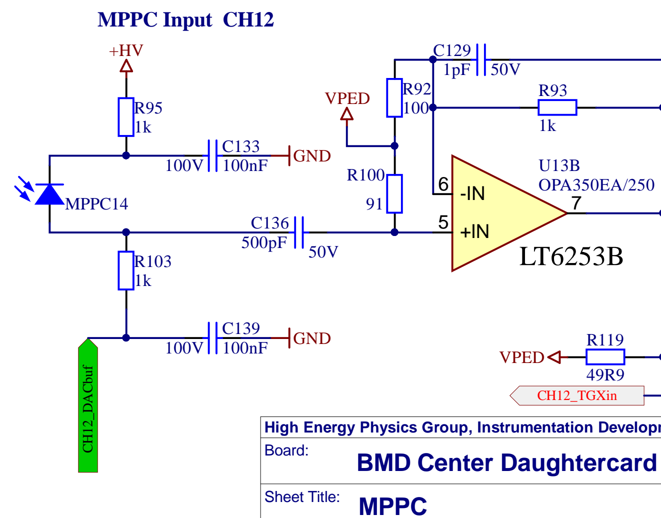












High Energy Physics Group, Instrumentation Development Lab	Designer: KPL/PO	IDLAB design #: IDL_18_014
Board: BMD Center Daughtercard	Drawn By: KPL/PO	Revision: B
	Approved By: Gary S. Varner	Variant: [No Variations]
Sheet Title: MPPC		Modif. Date: 4/16/2018
		Sheet 5 of 6

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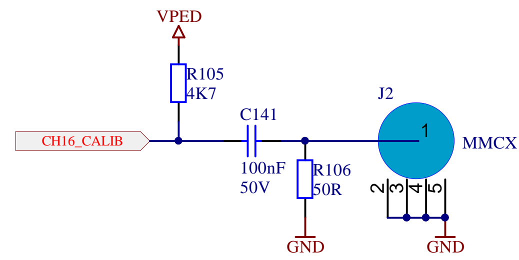
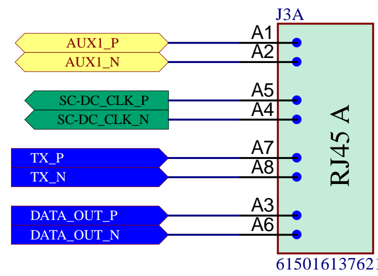
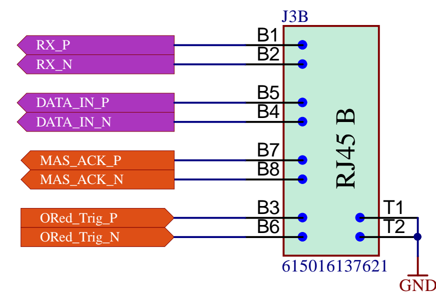
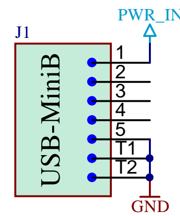
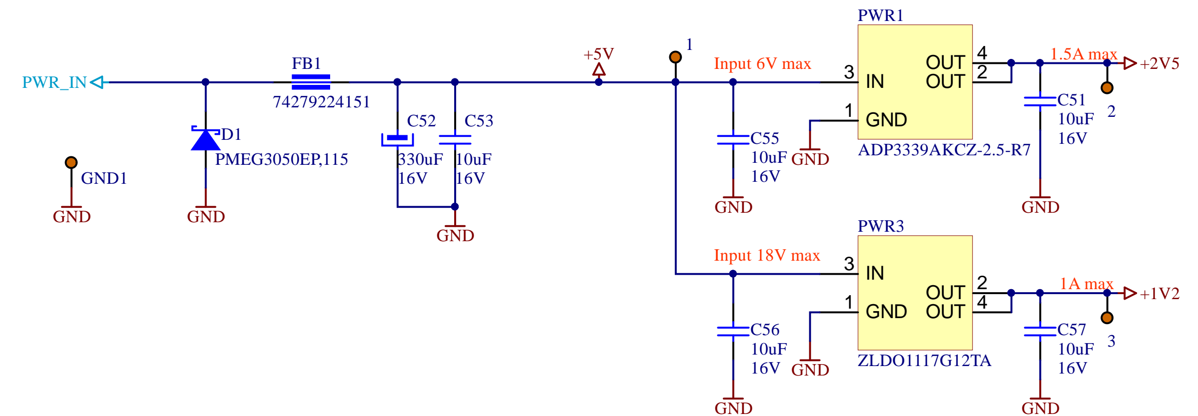


INPUT CONNECTOR

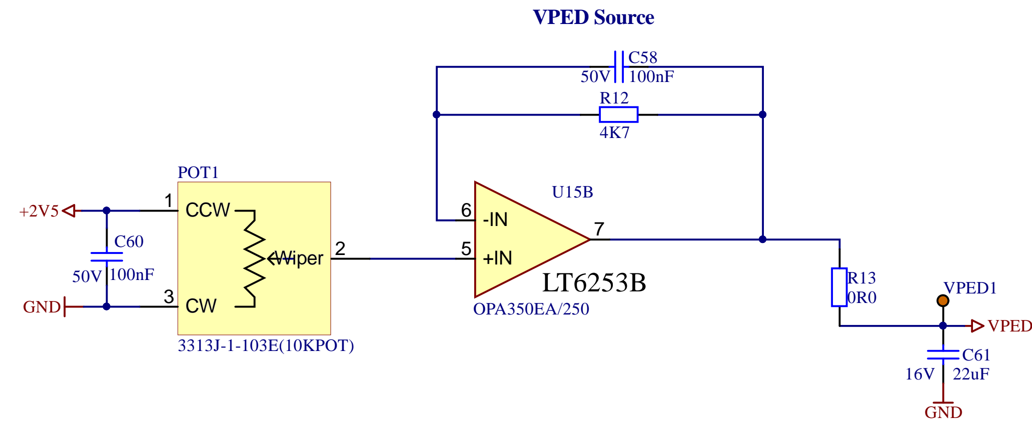






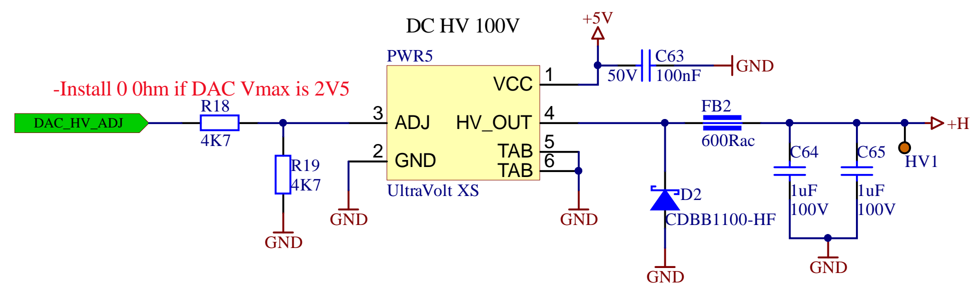


VPED Source



CALIB VPED NOTES:
-VPED = 0V8 at up to 500mA
-VPED = .8(1+(R66/R67))

DC HV 100V



FID1 PCB-FIDRT
FID2 PCB-FIDRT
FID3 PCB-FIDRT

L1
IDLab Logo
IDLab Logo

High Energy Physics Group, Instrumentation Development Lab	Designer: KPL/PO	IDLAB design #: IDL_18_014
Board: BMD Center Daughtercard	Drawn By: KPL/PO	Revision: B
	Approved By: Gary S. Varner	Variant: [No Variations]
Sheet Title: IN/OUT & MISC		Modif. Date: 4/16/2018
		Sheet 6 of 6

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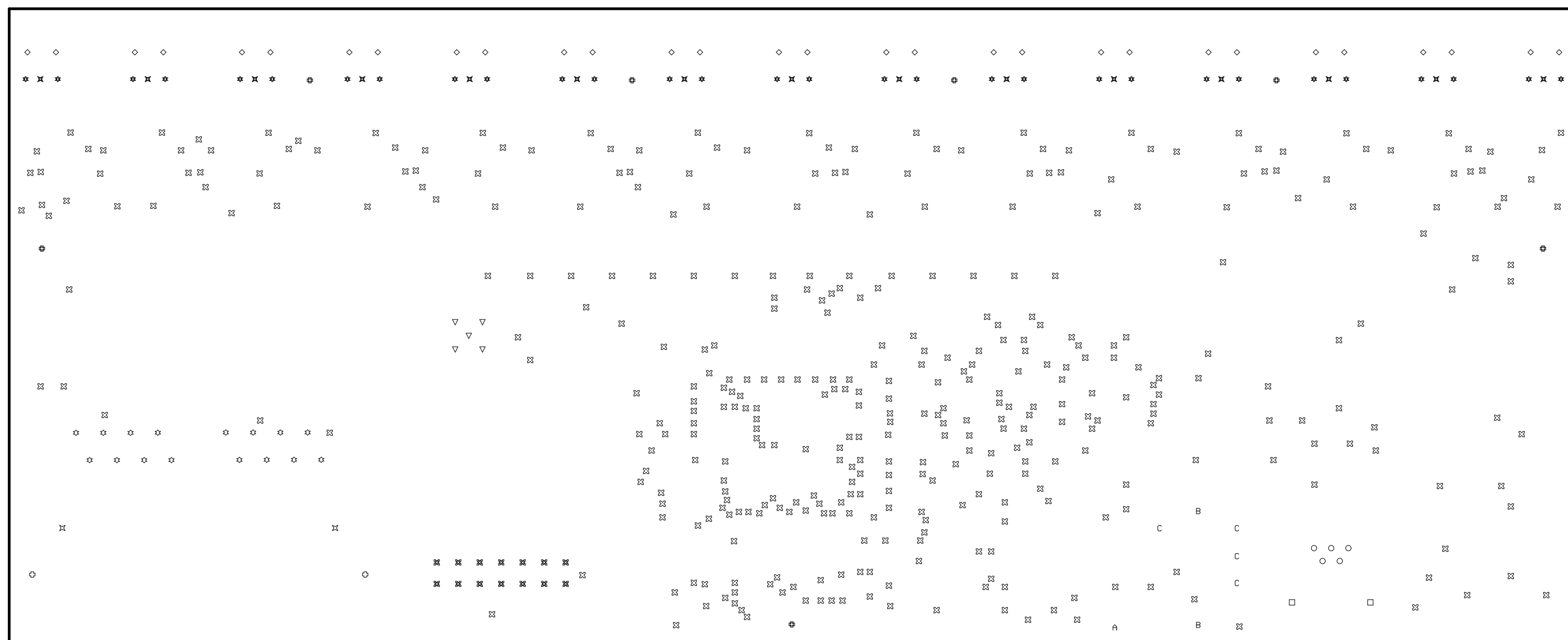

Notes:

1. Board shall be fabricated - performace class II as per IPC-6011 and IPC6012
2. Silkscreen printed on both sides
3. Material: high temperature FR4 class epoxy glass rated UL94V-0. UL symbol and rating shall be marked farside
   35um copper for external and internal layers
   Must be RoHS compliant and survive a lead-free assembly max reflow of 260 deg C (5 passes)
   Td rating: >340 deg C
   Tg = 150 deg C (min)
4. Solder mask: SMOBC per IPC-SM-840C, class T must be Rohs compliant, 0.001" max measured over bare copper plating, must clear all lands as indicated on gerber solder mask layers, color= GREEN
5. Finish: electro-less nickel immersion gold (ENIG), 0.05-0.125um Au over 3-6um Ni - over bare copper only
6. Solderability test: Category 2 of J-STD-003
7. Finished boards shall not have nicks, scratches, voids, exposed copper, poor plating or misdrilled holes
8. All holes sizes are after plating
9. PCB manufacturer may add copper thieving as needed to improve manufacturability,
   thieving to be 0.030" round pads at 0.050" spacing.
   Thieving will have a minimum of 0.100" clearance from existing copper and should not be placed under surface mounted devices
10. PCB manufacturer may use tear drops to improve annular rings as long as DRC rules are followed
11. All via connections to power and ground planes are solid
12. All unconnected pads on inner signal layers are removed
13. All finished boards are to be 100% electrically tested
14. Unless otherwise indicated, all linear toleracnes shall be XX.X +/-0.2mm and XX.XX +/- 0.1mm
15. Gerber file GM1 shows board outline (milling line)
16. Table 1 shows Layer stack details
17. Gerber files GTP ans DBP shows stencil cut out, stencil should be flat with no bent tabs on sides.

Table 1a: Layer Stack Details for IDL_16_010 Rev.B (Imperial Units)

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	L1-Top	Copper	1.38mil		
4	Dielectric 1	FR-4	8.00mil	4.65	
5	L2-GND	Copper	1.38mil		
6	Dielectric 2	FR-4	12.00mil	4.65	
7	L3-MID	Copper	1.38mil		
8	Dielectric 3	FR-4	12.00mil	4.65	
9	L4-PWR	Copper	1.38mil		
10	Dielectric 4	FR-4	12.00mil	4.65	
11	L5-PWR5V	Copper	1.38mil		
12	Dielectric 5	FR-4	8.00mil	4.65	
13	L6-Bottom	Copper	1.38mil		
14	Bottom Solder	Solder Resist	0.40mil	3.5	
15	Bottom Overlay				

Table 1b: Layer Stack Details for IDL_16_010 Rev.B (Metric Units)

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.010mm	3.5	
3	L1-Top	Copper	0.035mm		
4	Dielectric 1	FR-4	0.203mm	4.65	
5	L2-GND	Copper	0.035mm		
6	Dielectric 2	FR-4	0.305mm	4.65	
7	L3-MID	Copper	0.035mm		
8	Dielectric 3	FR-4	0.305mm	4.65	
9	L4-PWR	Copper	0.035mm		
10	Dielectric 4	FR-4	0.305mm	4.65	
11	L5-PWR5V	Copper	0.035mm		
12	Dielectric 5	FR-4	0.203mm	4.65	
13	L6-Bottom	Copper	0.035mm		
14	Bottom Solder	Solder Resist	0.010mm	3.5	
15	Bottom Overlay				

Table 2: NC Drill Details for IDL_16_010 Rev.B

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type	Hole Length
A	1	70.00mil (1.778mm)	PTH	Round	-
□	2	29.53mil (0.750mm)	PTH	Slot	74.80mil (1.900mm)
B	2	39.37mil (1.000mm)	PTH	Slot	78.74mil (2.000mm)
[illegible]	2	66.93mil (1.700mm)	PTH	Slot	118.11mil (3.000mm)
¤	2	127.95mil (3.250mm)	NPTH	Round	-
C	4	45.28mil (1.150mm)	PTH	Round	-
O	5	27.56mil (0.700mm)	PTH	Round	-
∇	5	33.07mil (0.840mm)	PTH	Round	-
✪	7	100.00mil (2.540mm)	PTH	Round	-
✖	14	33.00mil (0.838mm)	PTH	Round	-
✖	15	9.84mil (0.250mm)	NPTH	Round	-
✡	16	35.43mil (0.900mm)	PTH	Round	-
✡	30	19.69mil (0.500mm)	PTH	Round	-
◇	30	29.53mil (0.750mm)	PTH	Round	-
⊠	391	12.00mil (0.305mm)	PTH	Round	-
	526 Total				

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Designer: KPL/PO	Revision: B	File: BMD_RevB_PCB.PcbDoc	Sheet 1 of 1	Code: **IDL_18_014**
Drawn By: KPL/PO	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **BMD Center Daughtercard**
Approved By: Gary S. Varner	Print Date: 4/17/2018	Signature:	Size: A3 H	

Title: Drill Drawing and Dimensions GD1

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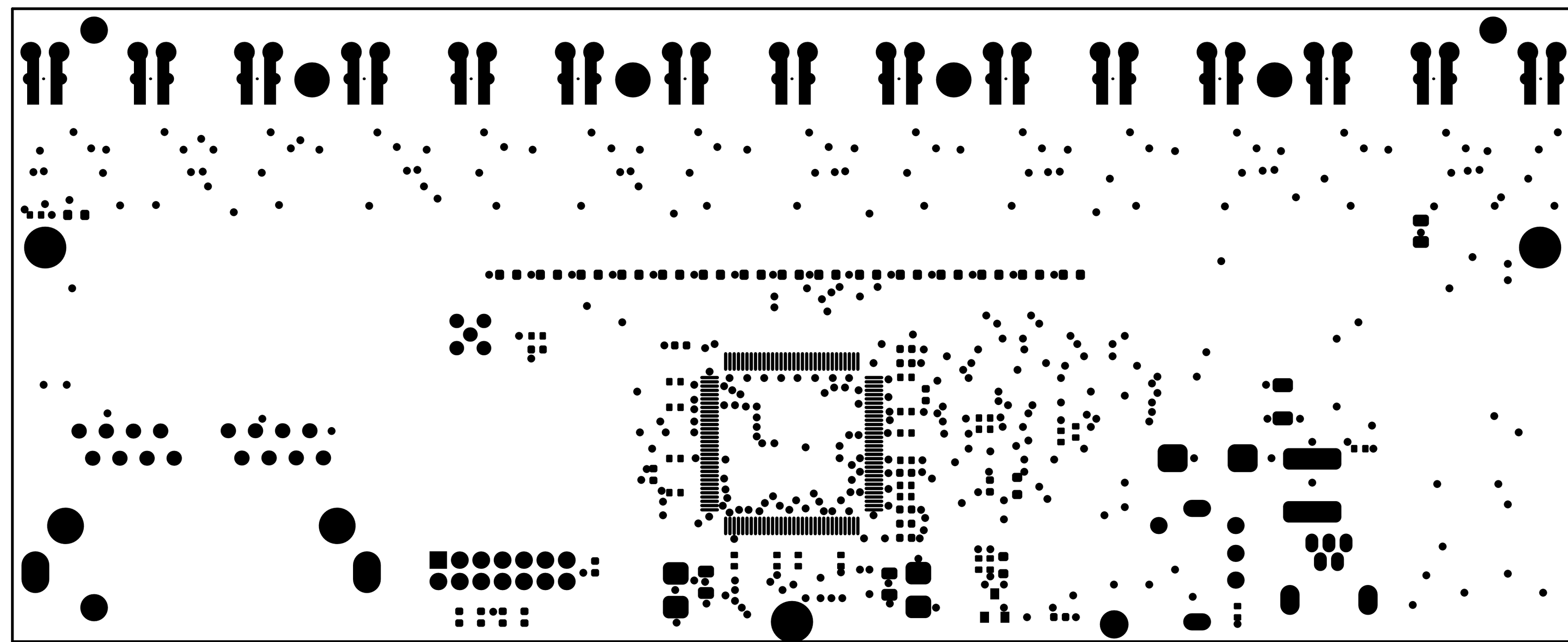

Designer: KPL/PO	Revision: B	File: BMD_RevB_PCB.PcbDoc	Sheet 1 of 1	Code: **IDL_18_014**
Drawn By: KPL/PO	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **BMD Center Daughtercard**
Approved By: Gary S. Varner	Print Date: 4/17/2018	Signature:	Size: A3 H	

Title:

Top Solder Mask GTS

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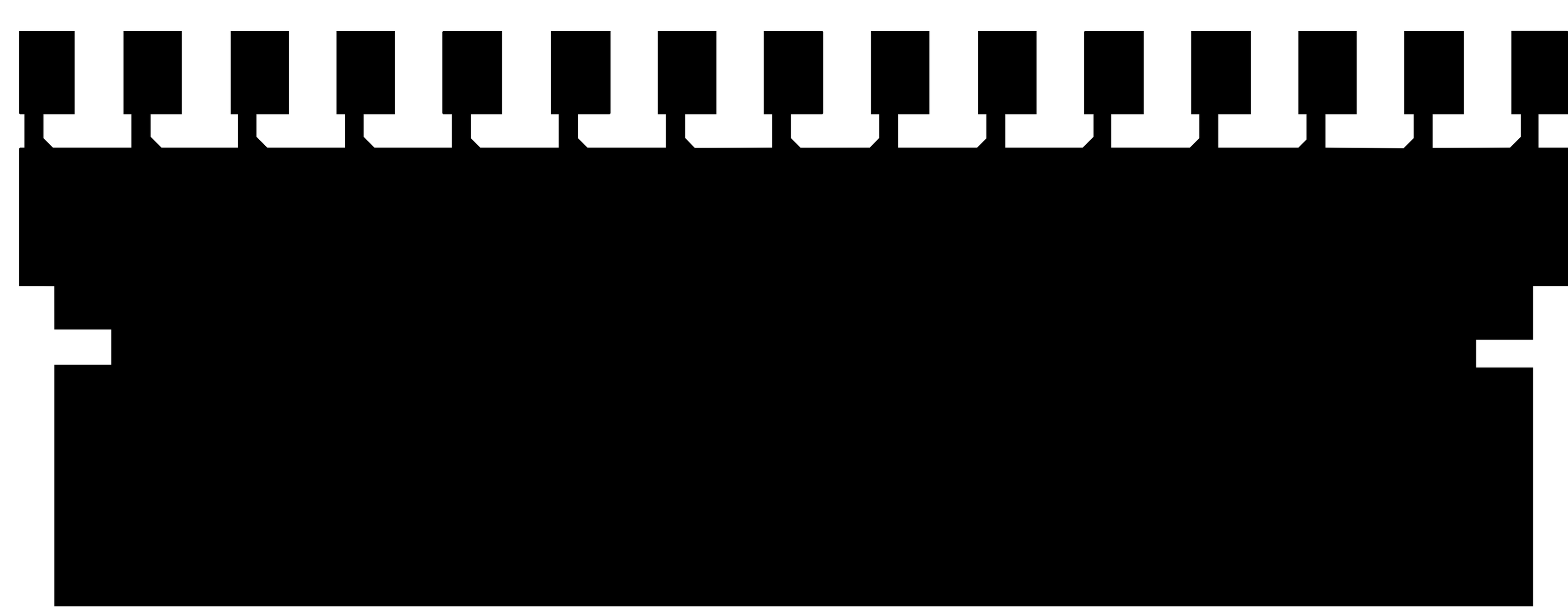
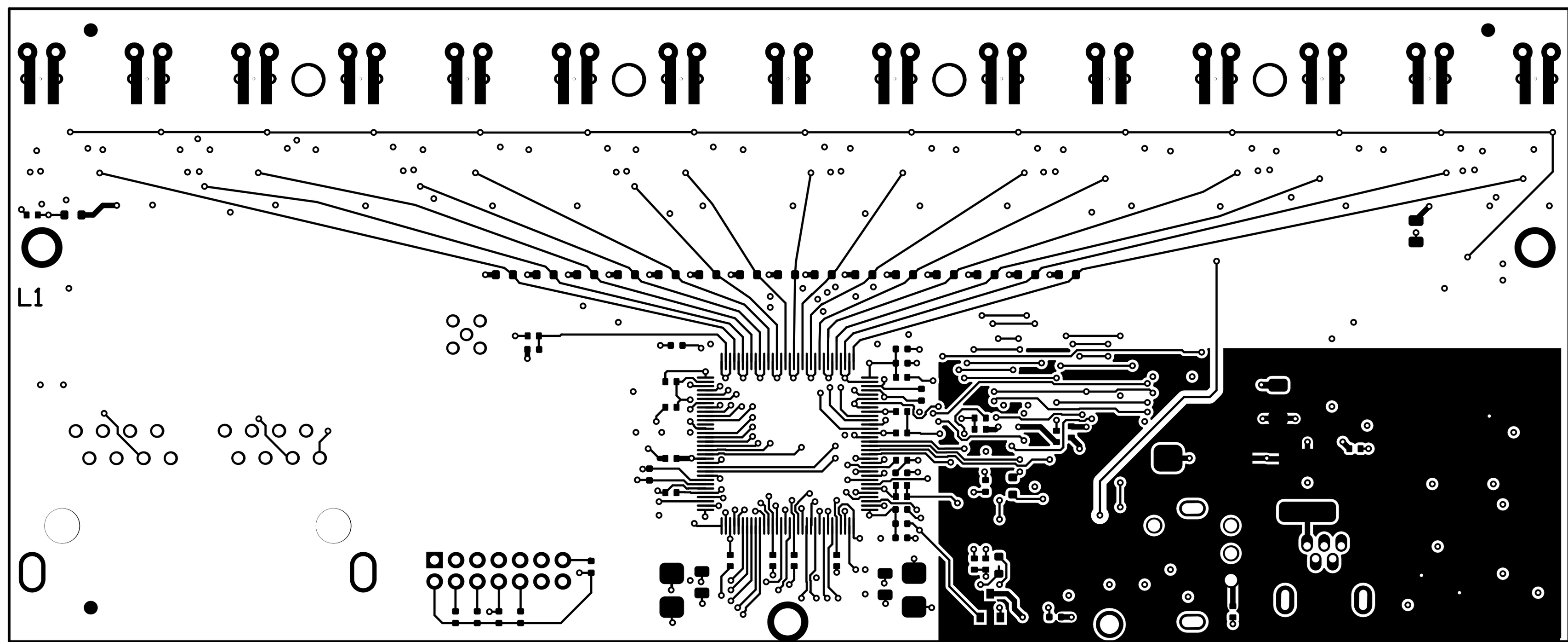
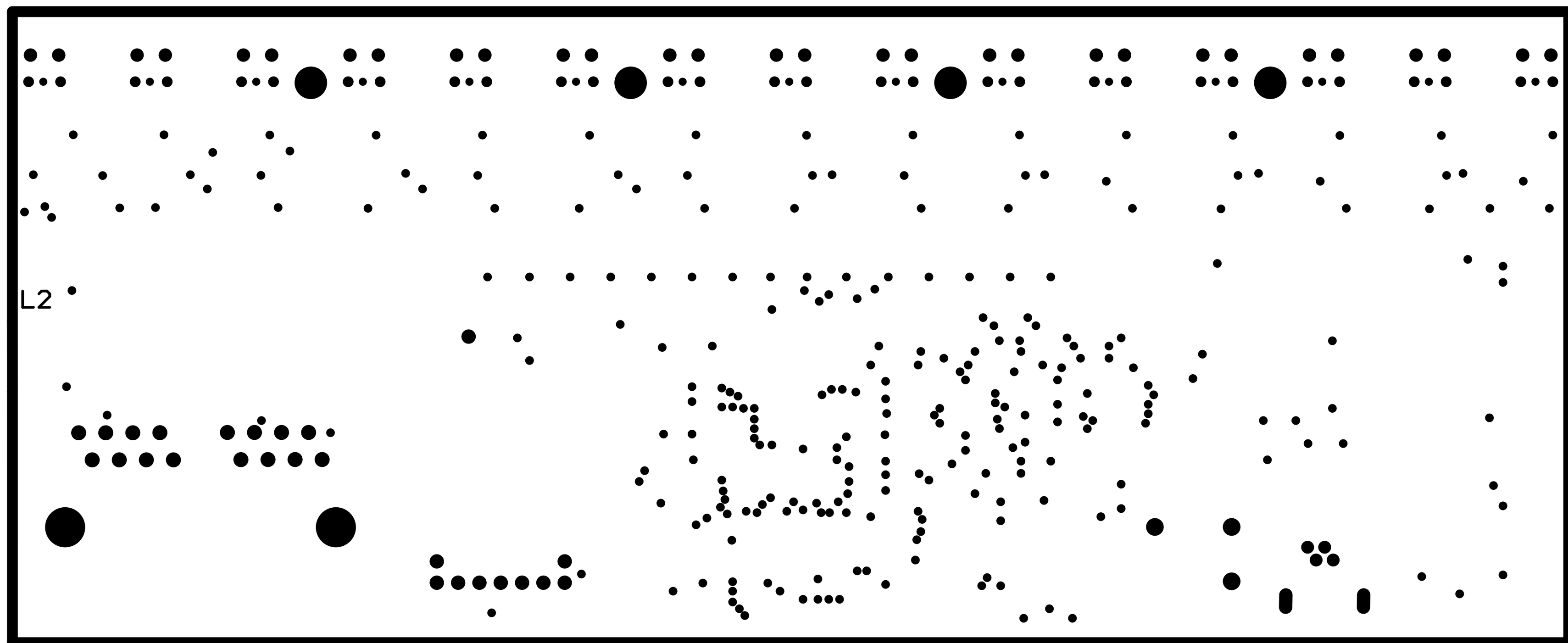
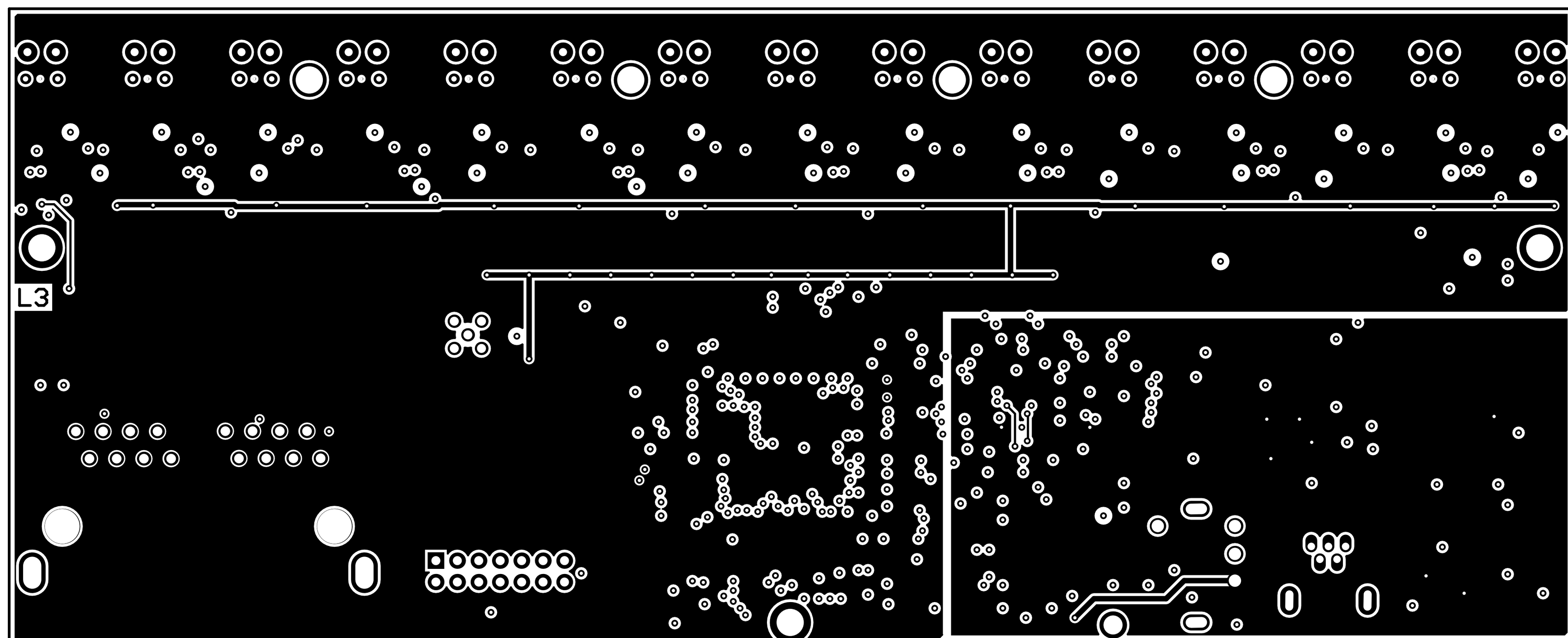




Designer: KPL/PO	Revision: B	File: BMD_RevB_PCB.PcbDoc	Sheet 1 of 1	Code: **IDL_18_014**
Drawn By: KPL/PO	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **BMD Center Daughtercard**
Approved By: Gary S. Varner	Print Date: 4/17/2018	Signature:	Size: A3 H	
Title: Top Layer 1 GTL				**University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory**



Designer: KPL/PO	Revision: B	File: BMD_RevB_PCB.PcbDoc	Sheet 1 of 1	Code: **IDL_18_014**
Drawn By: KPL/PO	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **BMD Center Daughtercard**
Approved By: Gary S. Varner	Print Date: 4/17/2018	Signature:	Size: A3 H	
Title: PWR Plane Layer 2 GP1				**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**



Designer: KPL/PO	Revision: B	File: BMD_RevB_PCB.PcbDoc	Sheet 1 of 1	Code: **IDL_18_014**
Drawn By: KPL/PO	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **BMD Center Daughtercard**
Approved By: Gary S. Varner	Print Date: 4/17/2018	Signature:	Size: A3 H	

Title: MID SIG Layer 3 GML1

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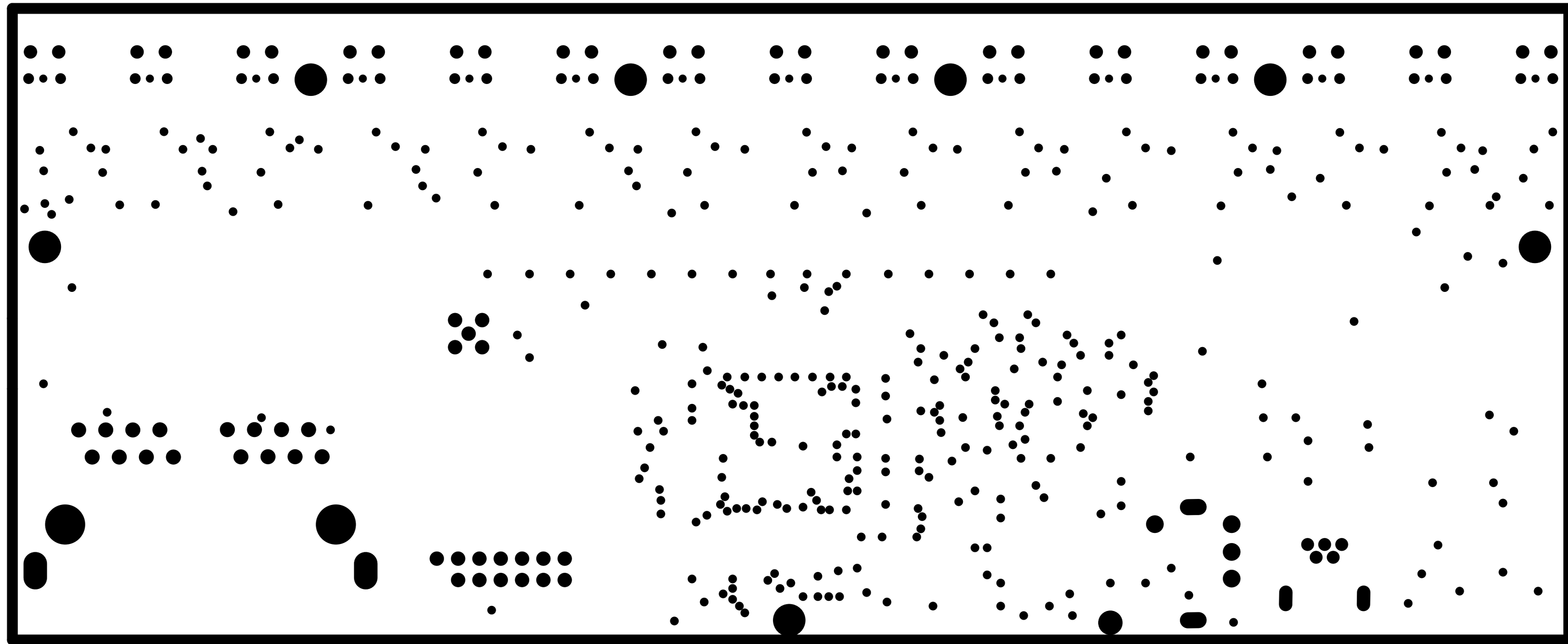
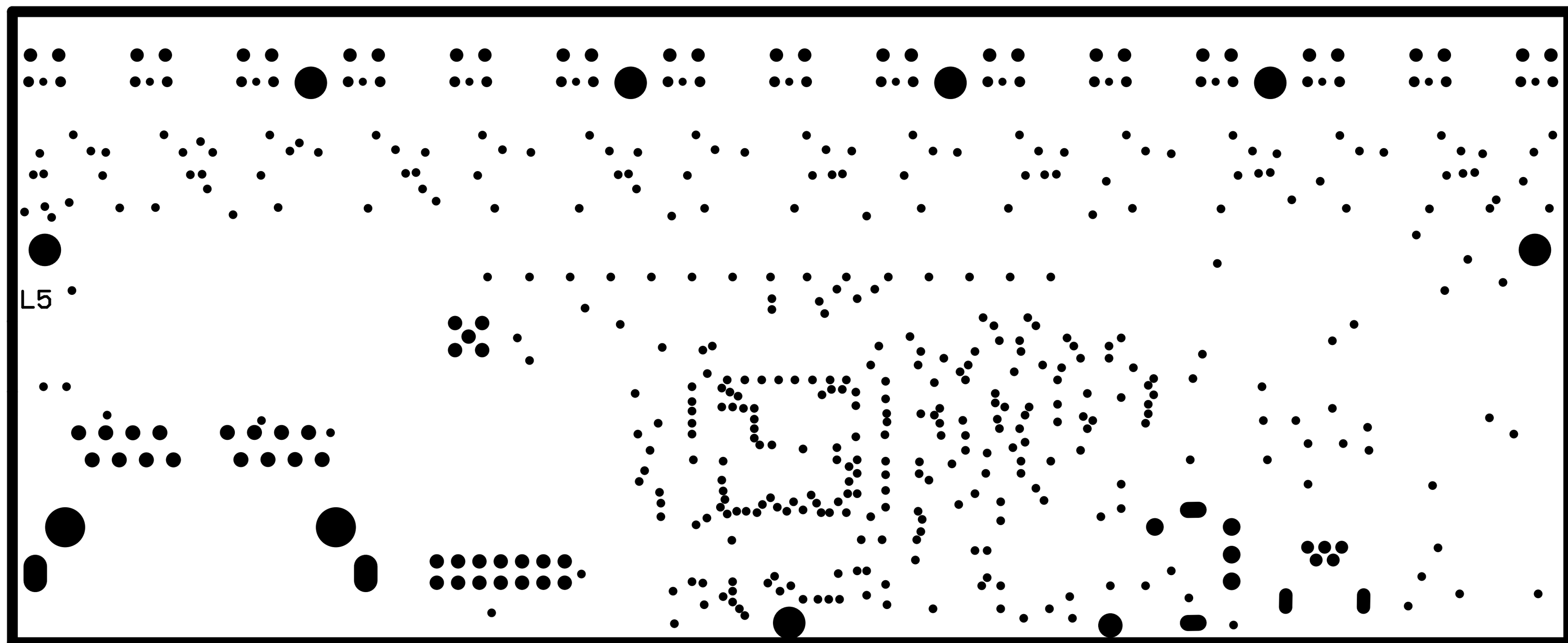


Designer: KPL/PO	Revision: B	File: BMD_RevB_PCB.PcbDoc	Sheet 1 of 1	Code: **IDL_18_014**
Drawn By: KPL/PO	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **BMD Center Daughtercard**
Approved By: Gary S. Varner	Print Date: 4/17/2018	Signature:	Size: A3 H	
Title: PWR Plane Layer 4 GP2				**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**



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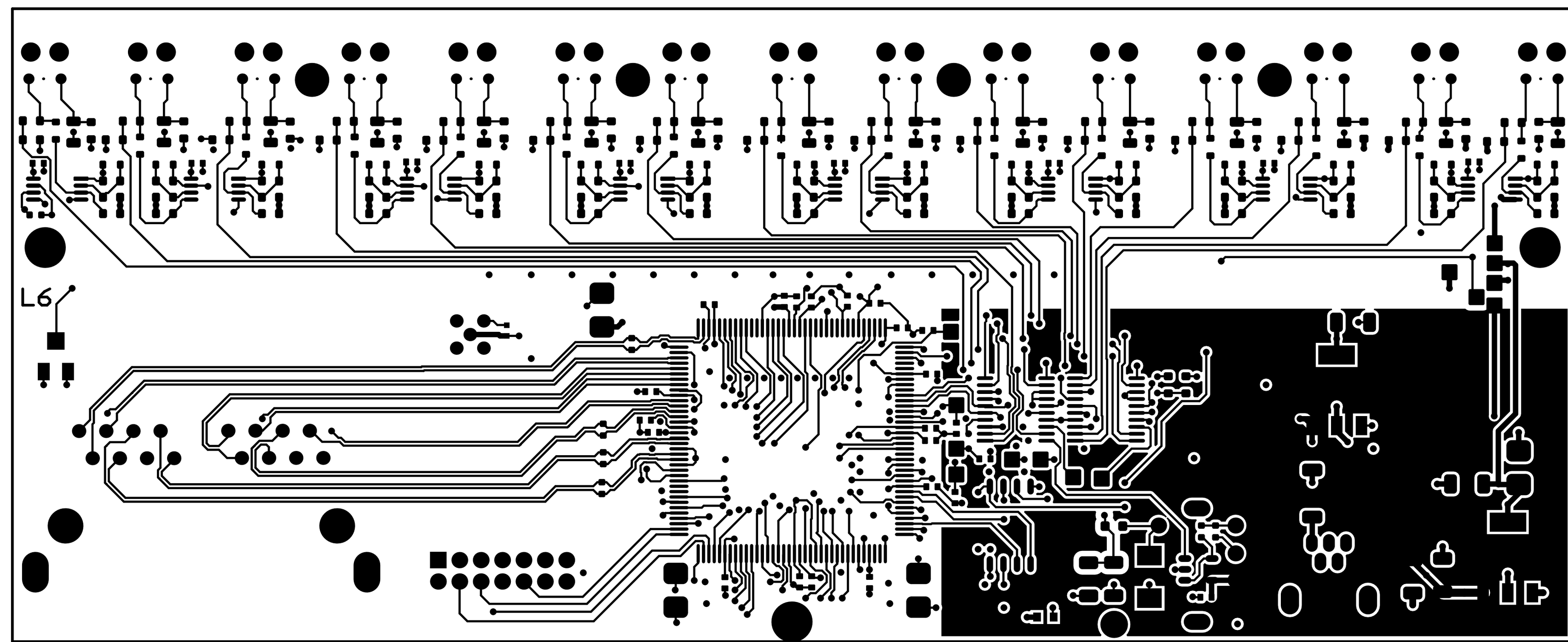
Approved By: Gary S. Varner	Print Date: 4/17/2018	Signature:	Size: A3 H	
Title: GND Plane Layer 5 GD2				**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**



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Approved By: Gary S. Varner	Print Date: 4/17/2018	Signature:	Size: A3 H	

Title:

Bottom Layer 6 GBL

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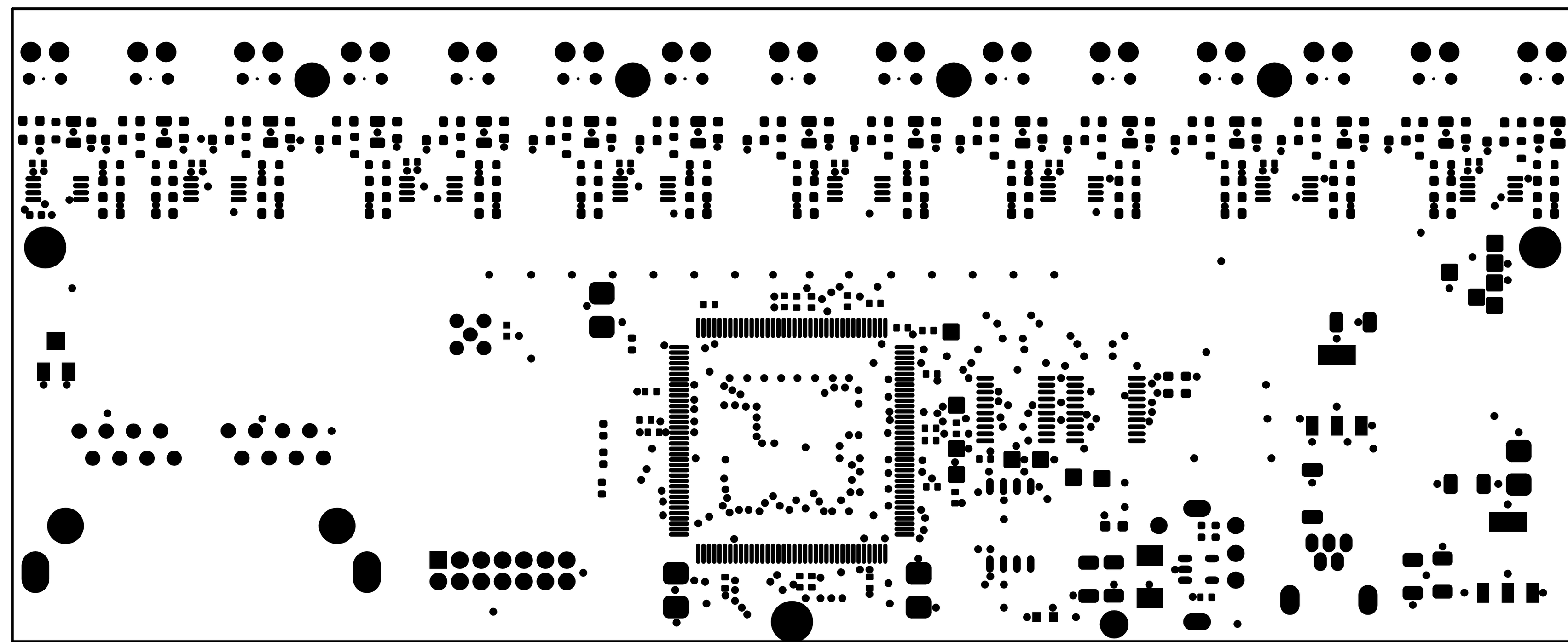

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Approved By: Gary S. Varner	Print Date: 4/17/2018	Signature:	Size: A3 H	
Title: Bottom Solder Mask GBS				**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**