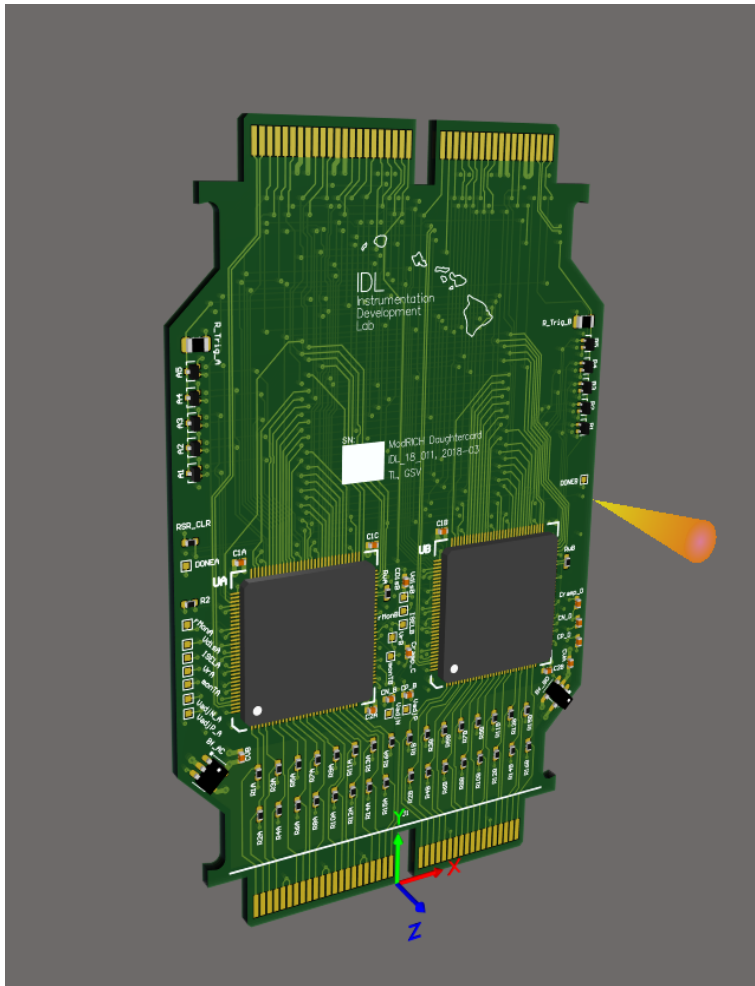




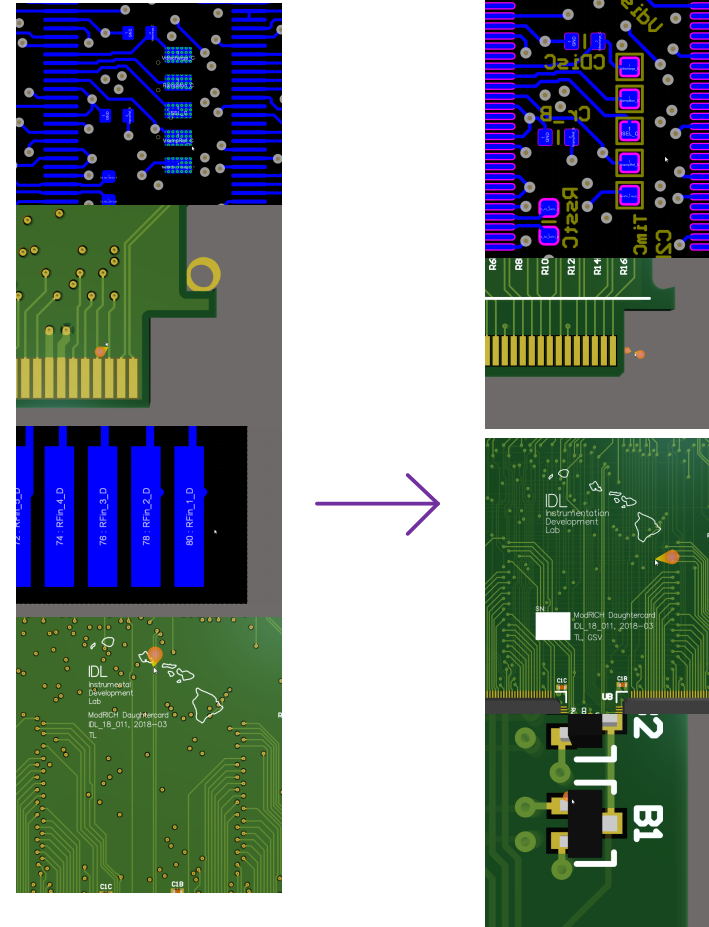
Instrumentation Development Lab IDL_18_011 - mRich Daughter Card V2

Designer : Tommy Lum,
Gary Varner
Adviser : Gary Varner

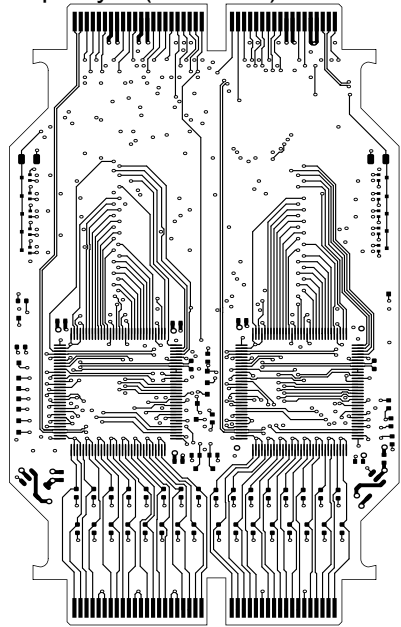
Change Log

5/10/2018 - Change Done by : JDC, CK

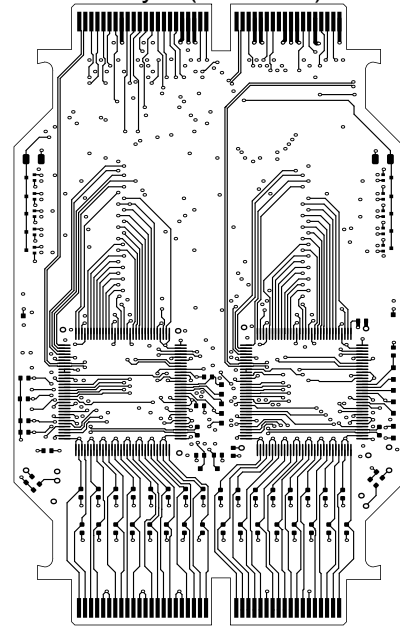
1. Added additional note/gerber specifying the chamfer location.
2. Removed the pastmask layer from the connectors and the test points.
3. Corrected the Boarder outline to the match the datasheet of the 3M connector.
4. Corrected some trace width to match the other size.
5. Corrected the SOT23 package footprint.
6. Corrected the output pdf and gerber file.
7. Changed the size of the test pads to a smaller footprint. (30mil - > 20mil)
8. Clean traced entry to pads
9. Added a Serial Number slikscreen to the top of the boards.
10. Changed the Ref Designators locations to be better seen.
11. Added additional note to the gerber drill drawing (#19, 20, & Figure 1)



Top Layer (Scale 1:1)



Bottom Layer (Scale 1:1)



Drill Table

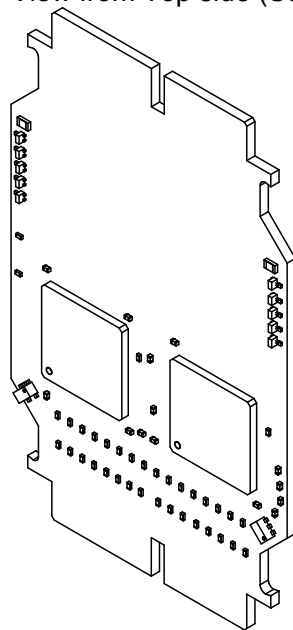
Symbol	Count	Hole Size	Plated	Hole Tolerance
□	525	0.20mm	Plated	None
○	15	0.41mm	Plated	None
540 Total				

Layer Stack Legend

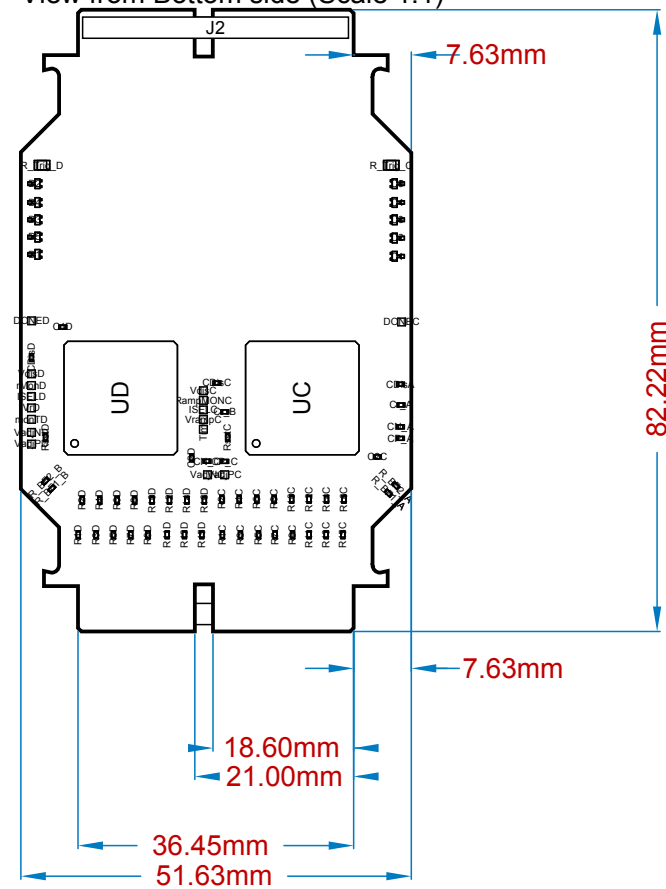
	Material	Layer	Thickness	Dielectric Material	Type	Gerber
		Top Paste			Paste Mask	GTP
		Top Overlay			Legend	GTO
	Surface Material	Top Solder	0.01mm	Solder Resist	Solder Mask	GTS
	Copper	Top Layer	0.04mm		Signal	GTL
			0.15mm	FR-4	Dielectric	
	Copper	GND	0.04mm		Internal Plane	GP1
			0.30mm	FR-4	Dielectric	
	Copper	AUX Route Vert	0.04mm		Signal	G1
			0.41mm	FR-4	Dielectric	
	Copper	AUX Route Horz	0.04mm		Signal	G2
			0.30mm	FR-4	Dielectric	
	Copper	2.5V	0.04mm		Internal Plane	GP2
			0.15mm	FR-4	Dielectric	
	Copper	Bottom Layer	0.04mm		Signal	GBL
	Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask	GBS
		Bottom Overlay			Legend	GBO
		Bottom Paste			Paste Mask	GBP

Total thickness: 1.55mm

View from Top side (Scale 1:1)

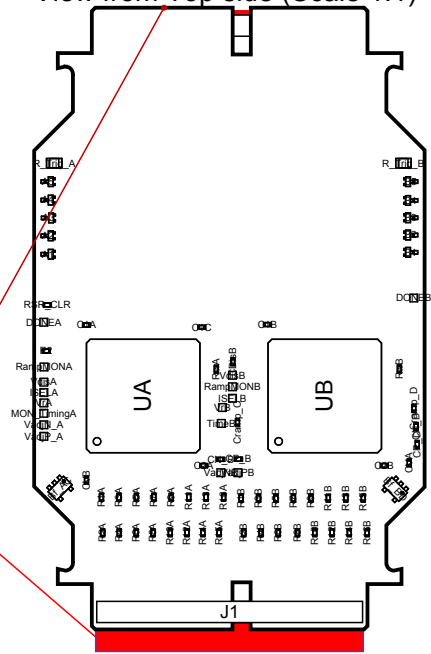


View from Bottom side (Scale 1:1)

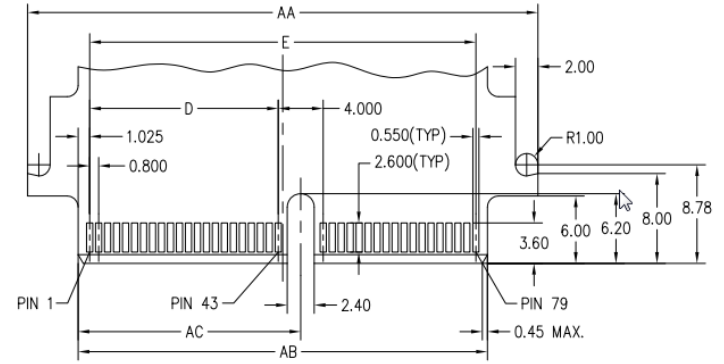
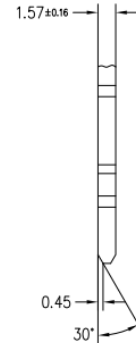


Chamfer This edge

View from Top side (Scale 1:1)



View from Left side (Scale 1:1)



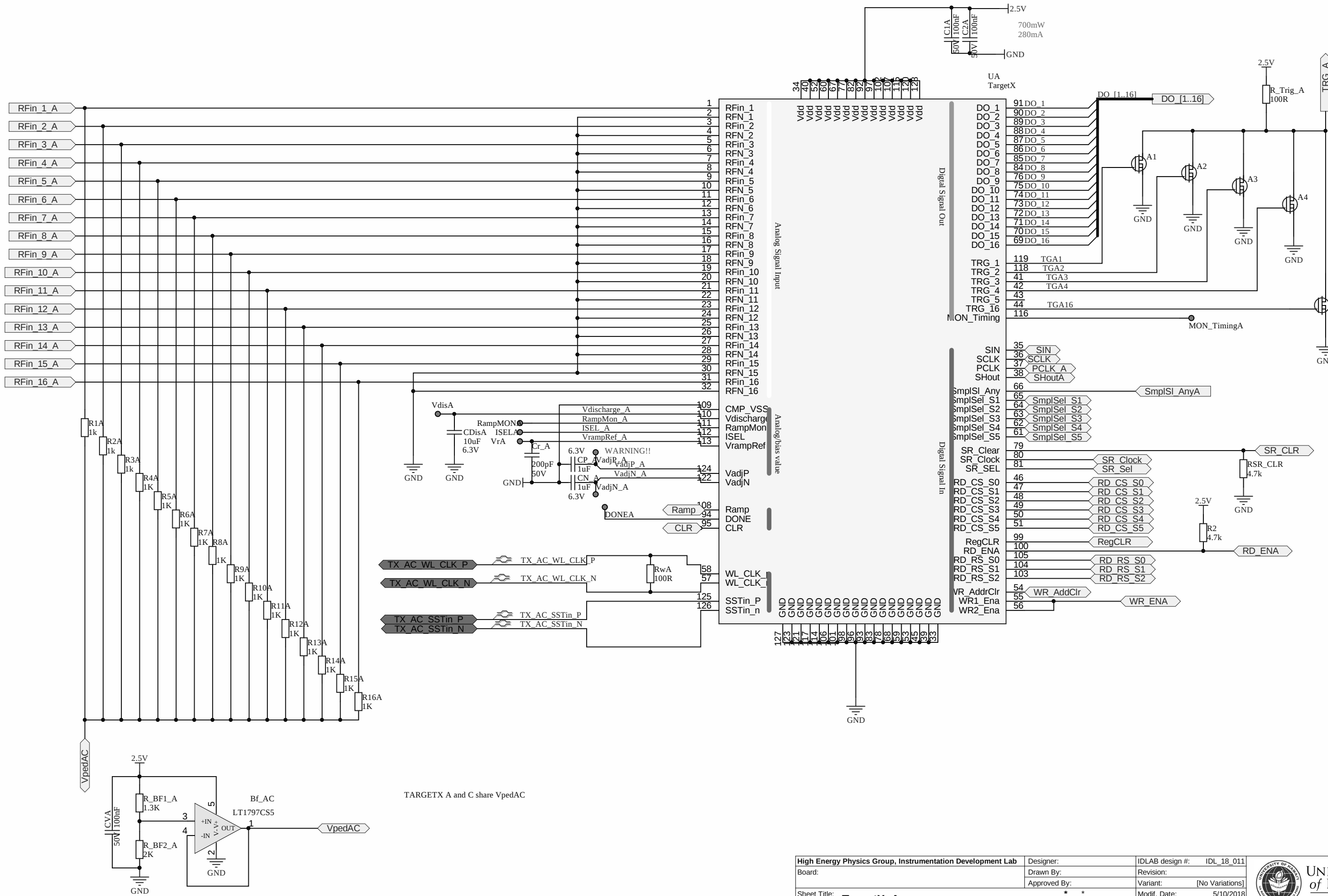
RECOMMENDED MATING CARD LAYOUT

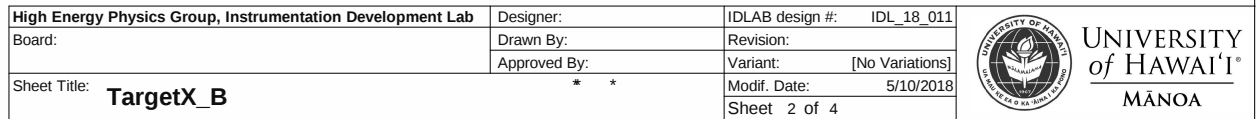
POSITIONS	DIMENSIONS							
	A	B	C	D	E	F	G	AA
80	51.05	36.60	19.90	16.800	34.400	37.40	42.10	45.45

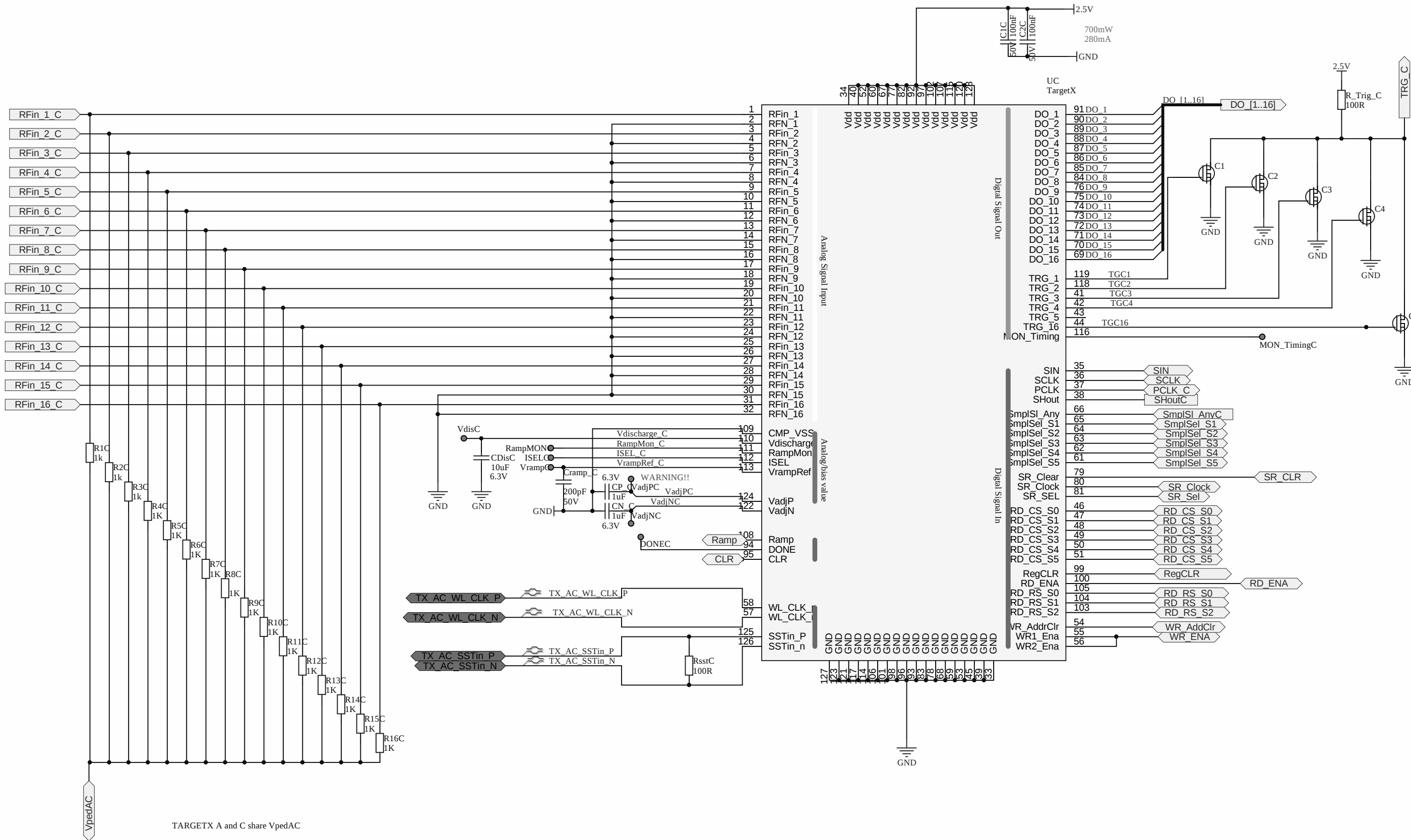
DESIGN REFERENCE	NEXT ASSEMBLY	REV	ECO	ISSUE DATE AND DESCRIPTION	DRGT	CHKD
1000	1000	1	1	05/21/11	1000	1000
DO NOT SCALE DRAWING	SCALE 2:1	TOLERANCES UNLESS NOTED	INCHES	3M	THIS DOCUMENT IS THE PROPRIETARY PROPERTY OF 3M COMPANY AND MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN PERMISSION OF 3M COMPANY.	
THIRD ANGLE PROJECTION	ISO 1	UNIT: MILLIMETERS	ANGLES: DEGREES	SPD08 HIGH SPEED CARD EDGE CONNECTOR, 0.8MM PITCH SMT		
MAX SURFACE ROUGHNESS	0.40	0.80	1.60	DATE: 05/21/11	DRAWN BY: 1000	REV: 1
ALL SURFACES CHAMFERED ONLY	0.40	0.80	1.60	DATE: 05/21/11	DRAWN BY: 1000	REV: 1

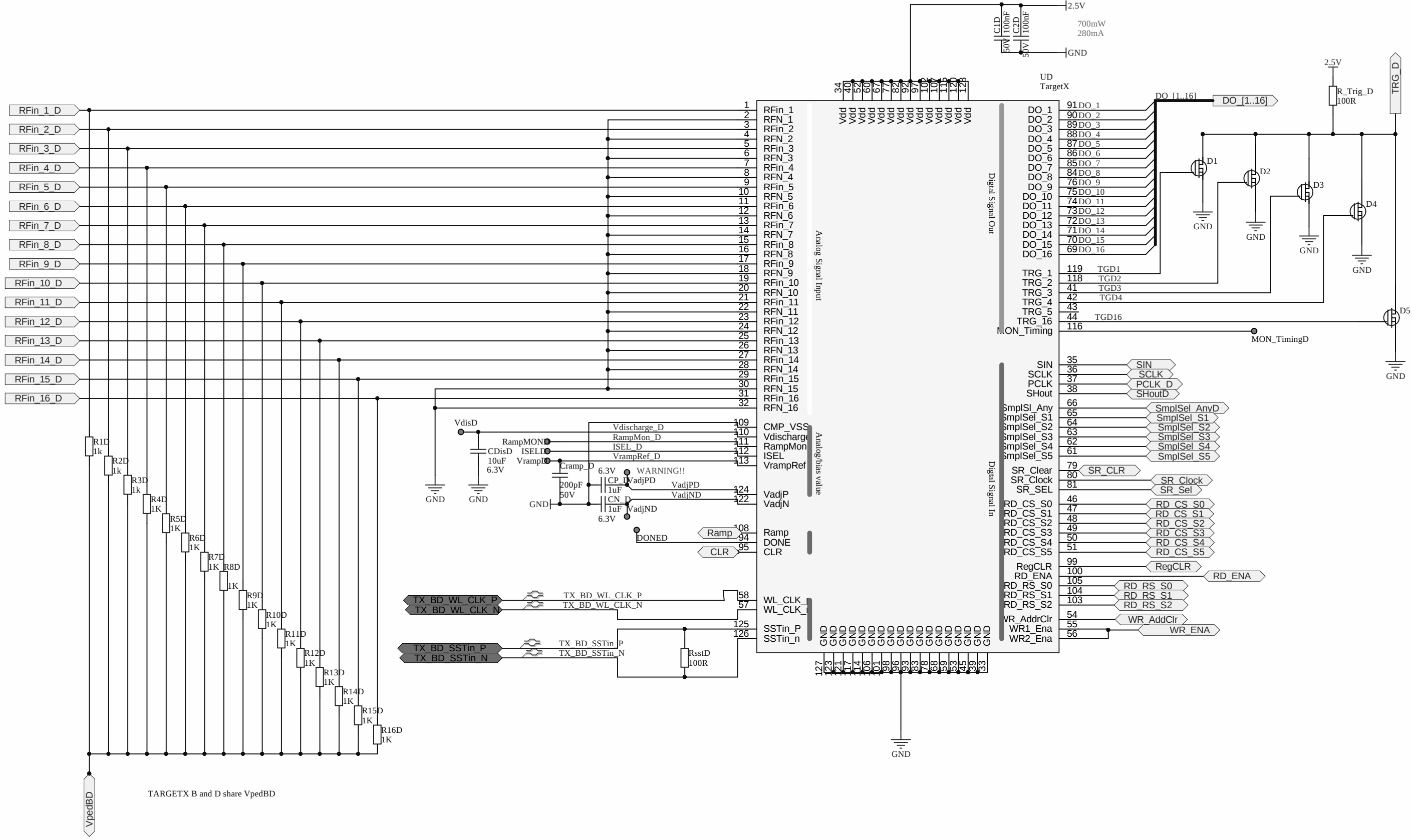
Bill Of Materials

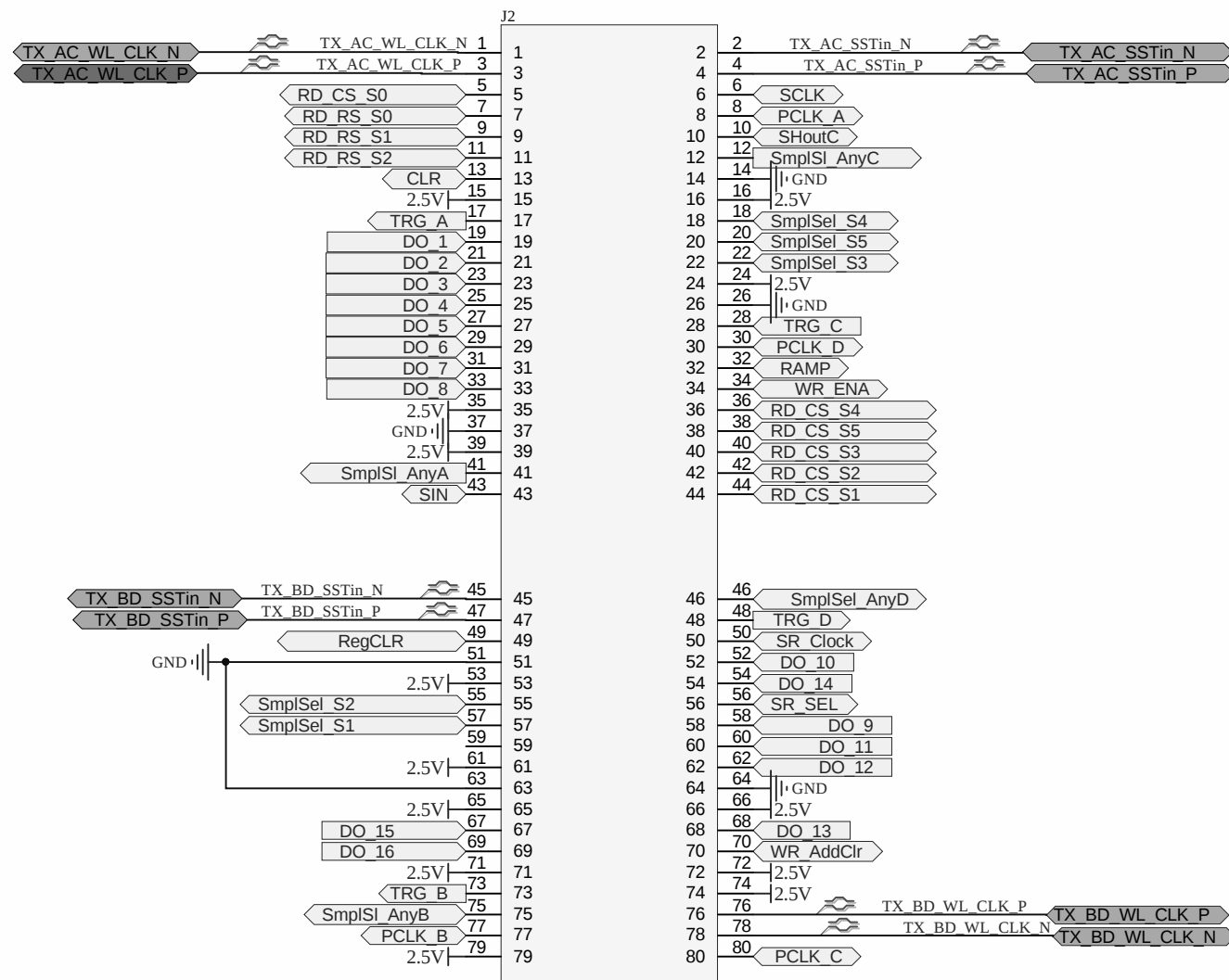
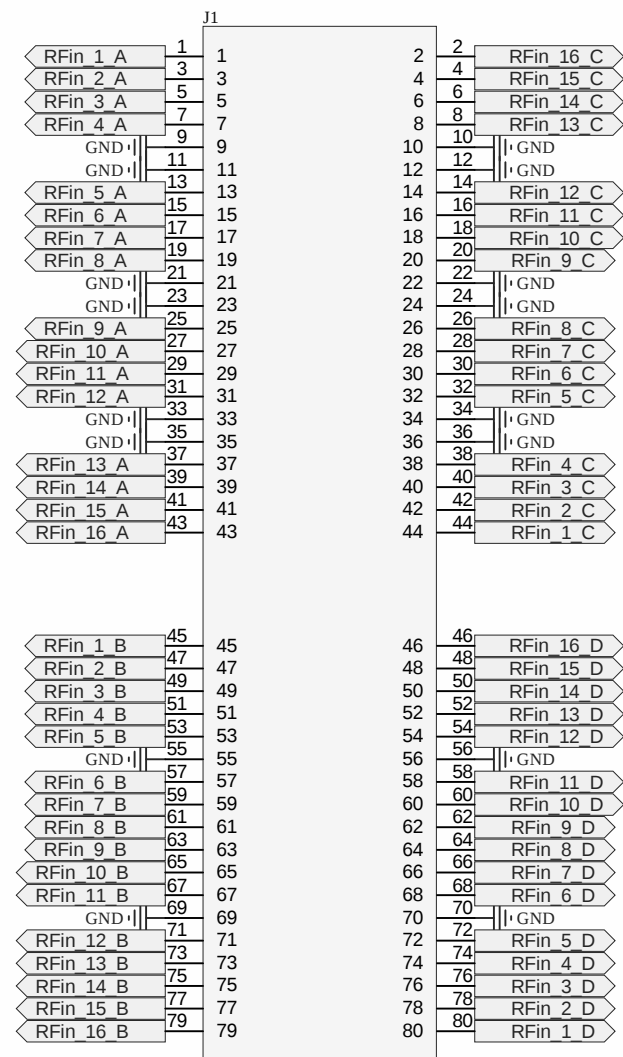
Line #	Designator	Comment	Quantity
1	A1, A2, A3, A4, A5, B1, B2, B3, B4, B5, C1, C2, C3, C4, C5, D1, D2, D3, D4, D5	MOSFET	20
2	Bf_AC, Bf_BD	LT1797CS5	2
3	C1A, C1B, C1C, C1D, C2A, C2B, C2C, C2D, CVA, CVB	100nF	10
4	CDisA, CDisB, CDisC, CDisD	10uF	4
5	CN_A, CN_B, CN_C, CN_D, CP_A, CP_B, CP_C, CP_D	1uF	8
6	Cr_A, Cr_B, Cramp_C, Cramp_D	200pF	4
7	J1, J2	SPD08 Card Edge Connector Mating Card Layout	2
8	R_BF1_A, R_BF1_B	1.3K	2
9	R_BF2_A, R_BF2_B	2K	2
10	R_Trig_A, R_Trig_B, R_Trig_C, R_Trig_D	100R	4
11	R1A, R1B, R1C, R1D, R2A, R2B, R2C, R2D, R3A, R3B, R3C, R3D	1k	12
12	R2, RSR_CLR	4.7k	2
13	R4A, R4B, R4C, R4D, R5A, R5B, R5C, R5D, R6A, R6B, R6C, R6D, R7A, R7B, R7C, R7D, R8A, R8B, R8C, R8D, R9A, R9B, R9C, R9D, R10A, R10B, R10C, R10D, R11A, R11B, R11C, R11D, R12A, R12B, R12C, R12D, R13A, R13B, R13C, R13D, R14A, R14B, R14C, R14D, R15A, R15B, R15C, R15D, R16A, R16B, R16C, R16D	1K	52
14	RsstC, RsstD, Rwa, Rwb	100R	4
15	UA, UB, UC, UD	TargetX	4

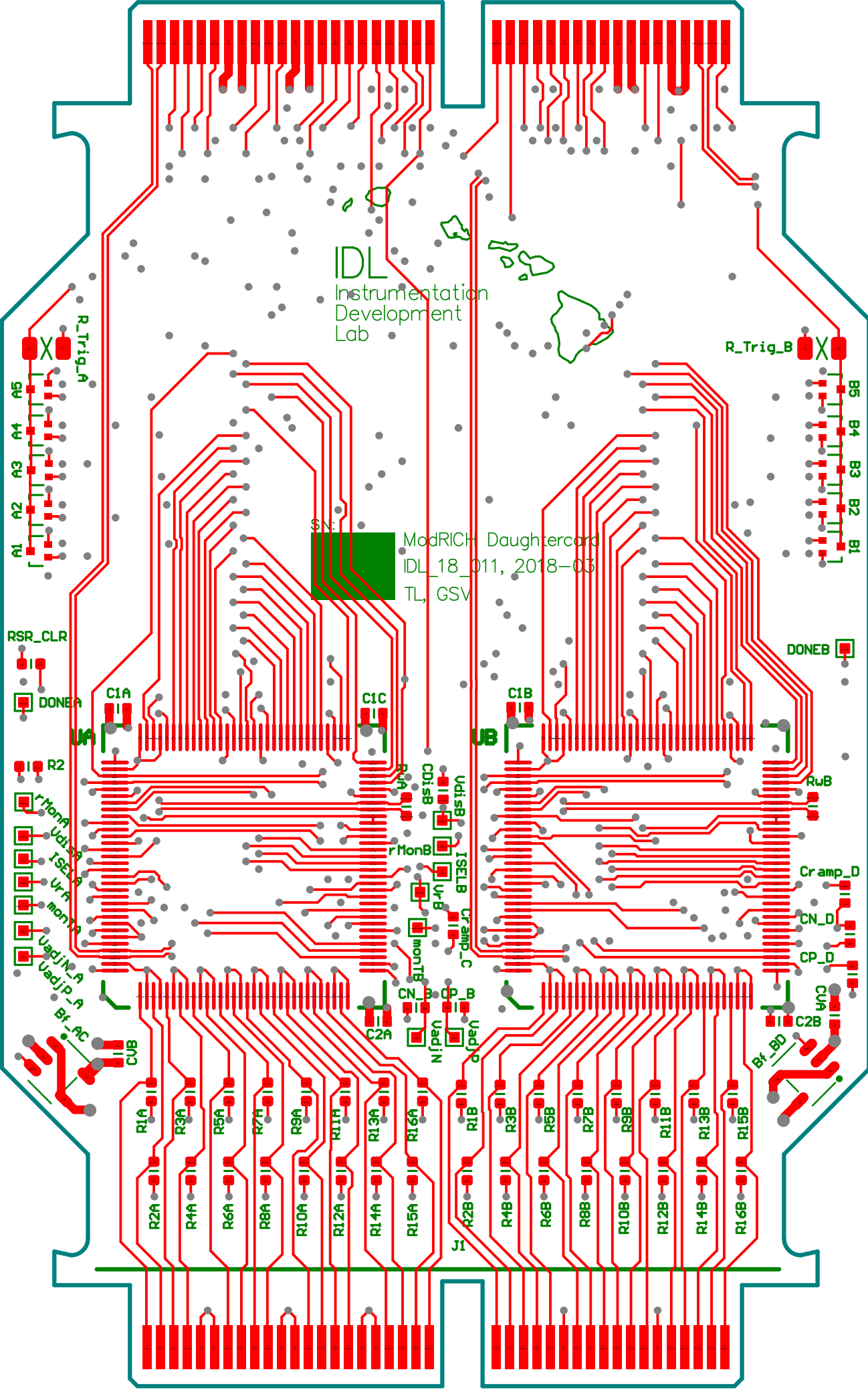


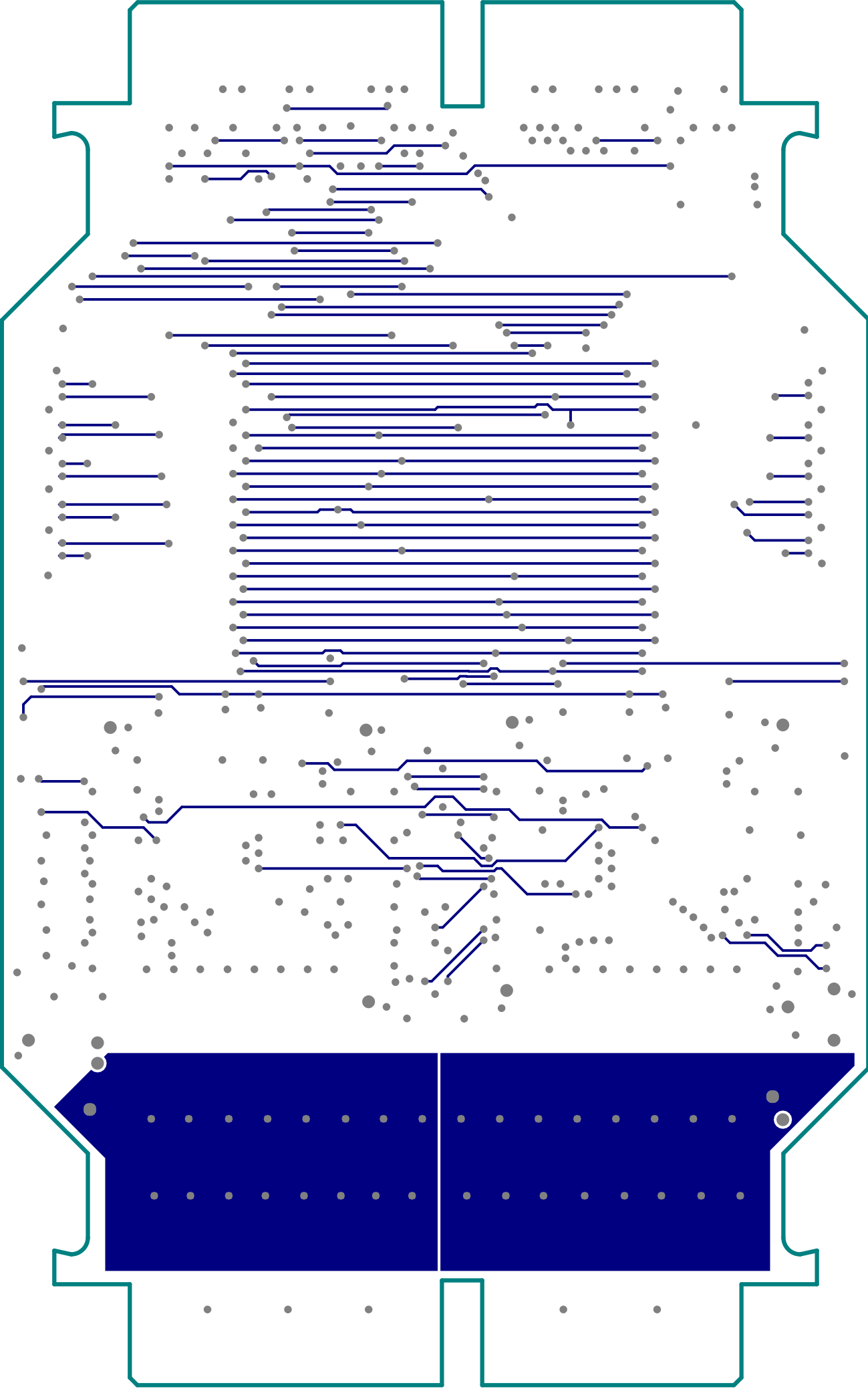


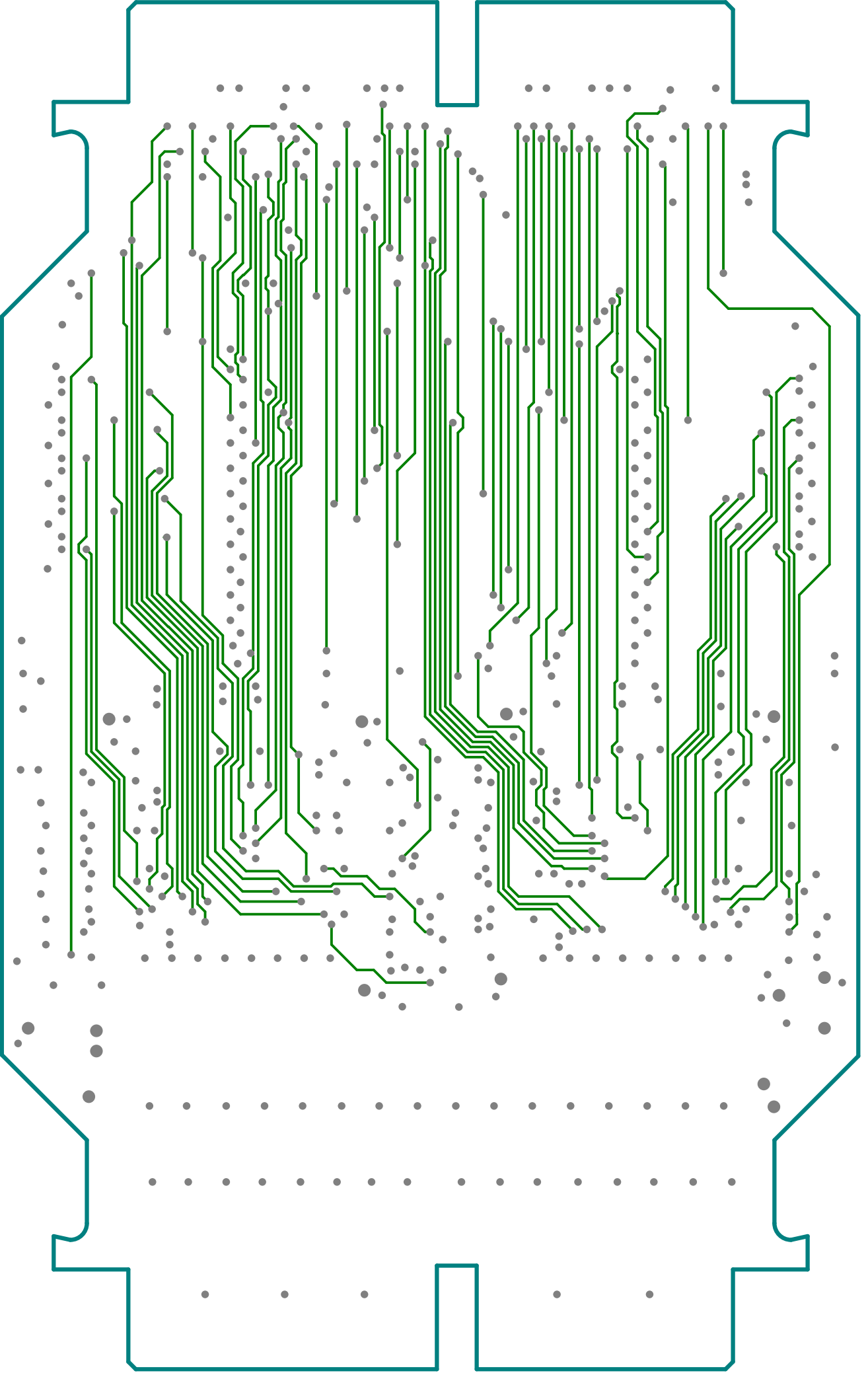


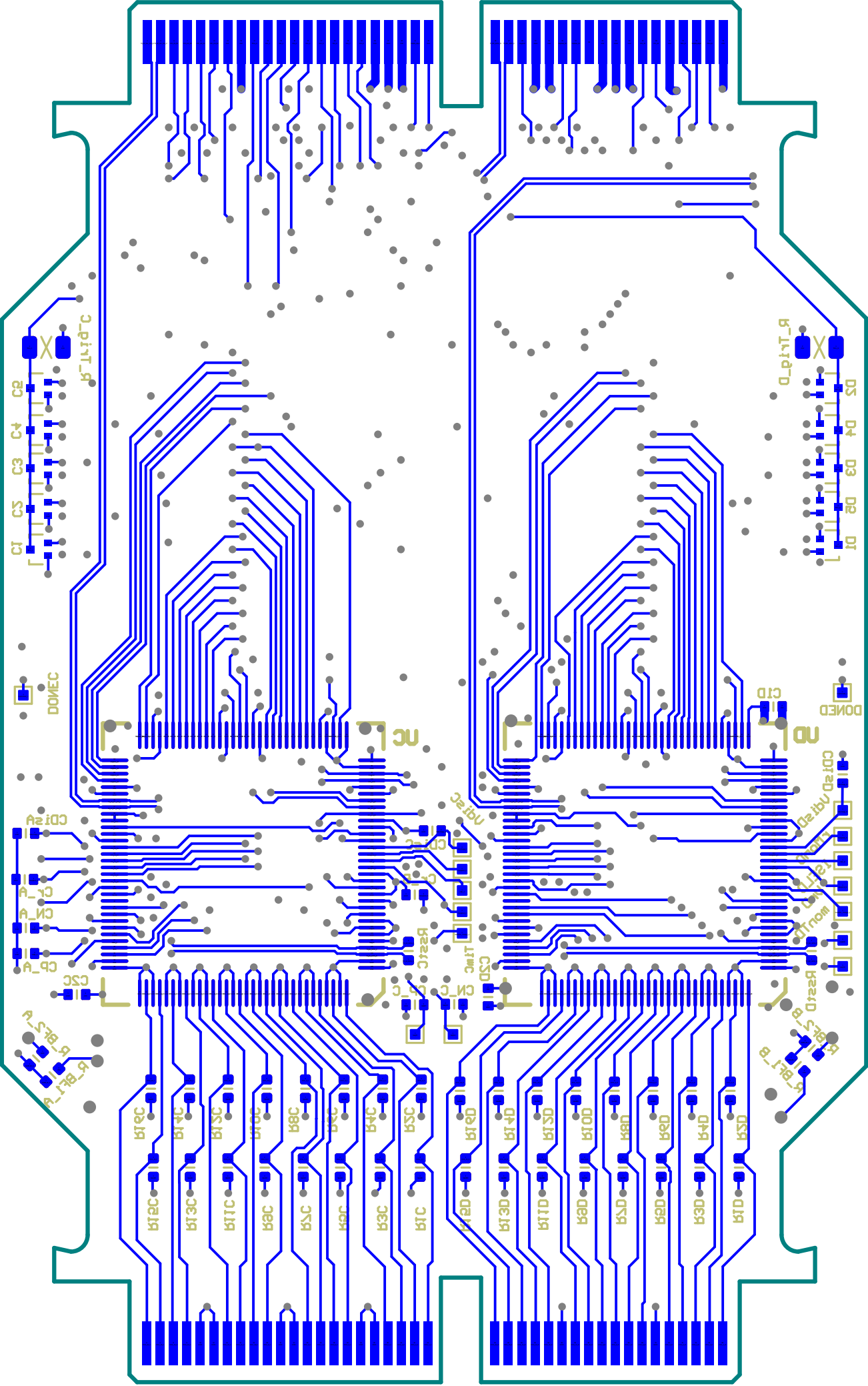


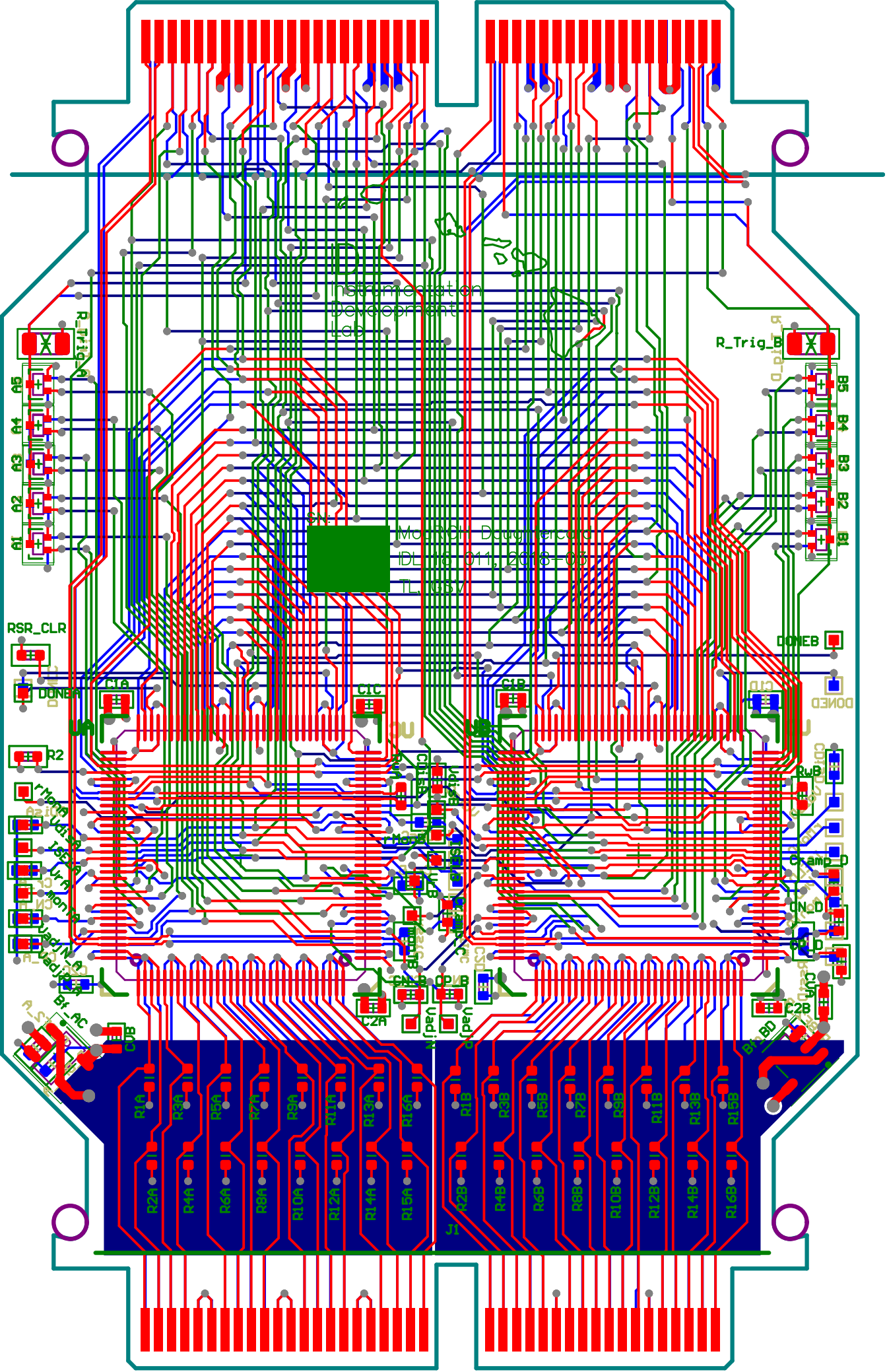












IDL
Instrumentation
Development
Lab

SN:



ModRICH Daughtercard
IDL_18_011, 2018-03
TL, GSV

