

E

D

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6

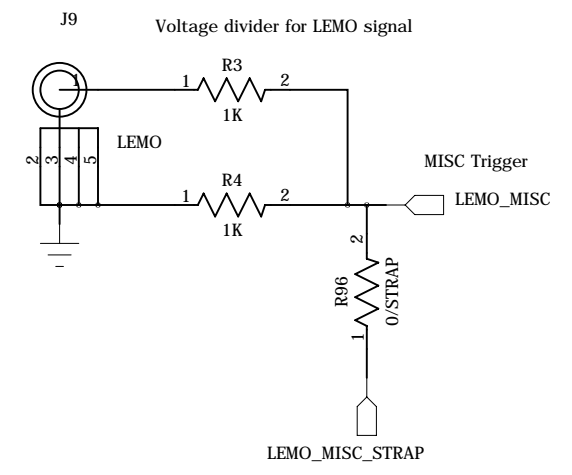
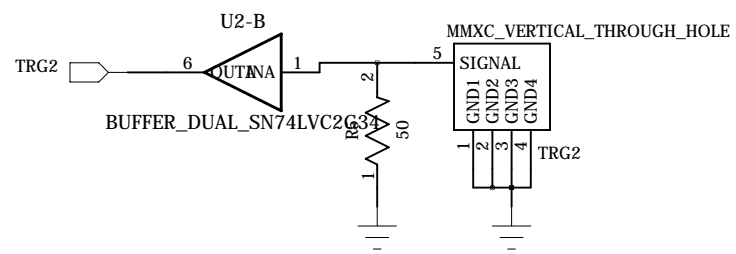
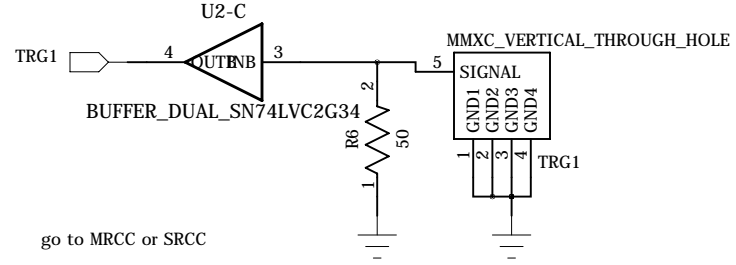
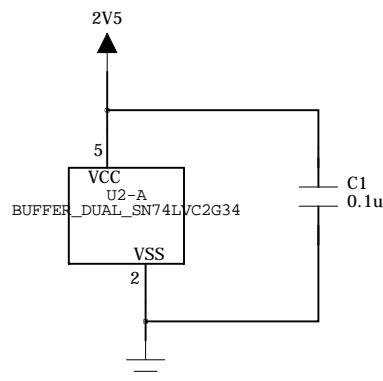
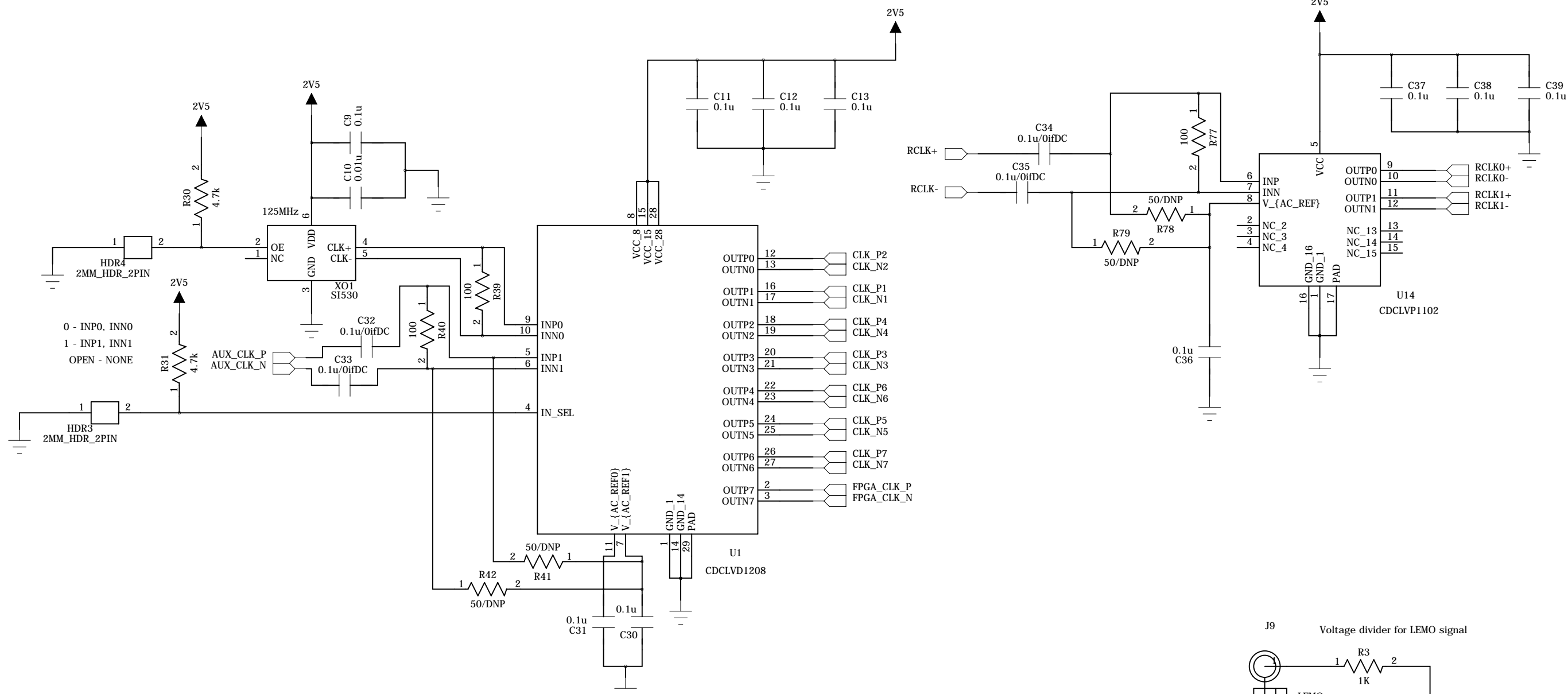
5

4

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1



institution: University of Hawaii at Manoa
 High Energy Physics Lab
 Instrumentation Development Lab

title: HMB_BMH
 revision: A
 IDLAB design #: IDL_17_010
 circuit design: JLB
 PCB design: JLB

sheet #: 1 of 10
 sheet description: Clocking
 date last modified: June 2, 2017

6

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4

3

2

1

E

E

D

D

C

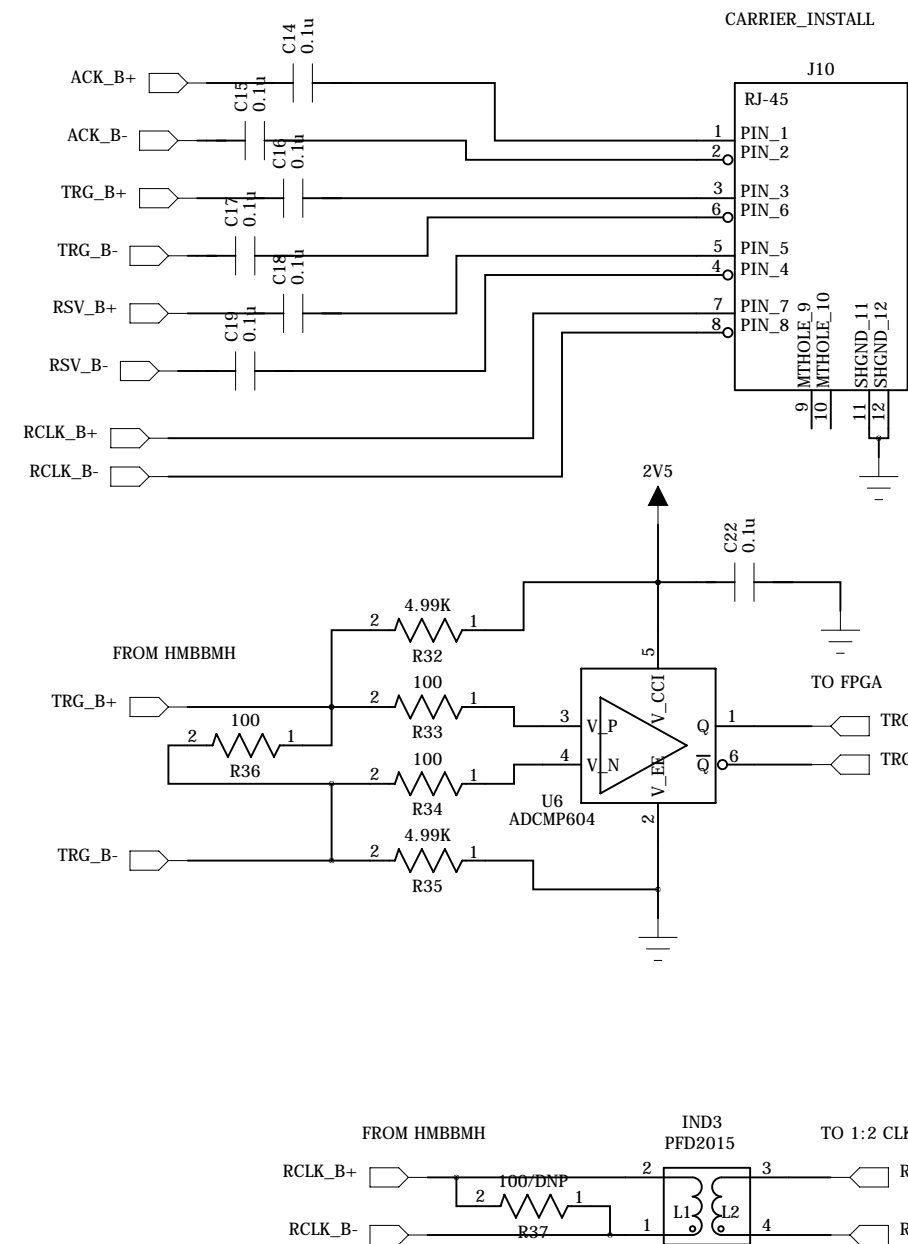
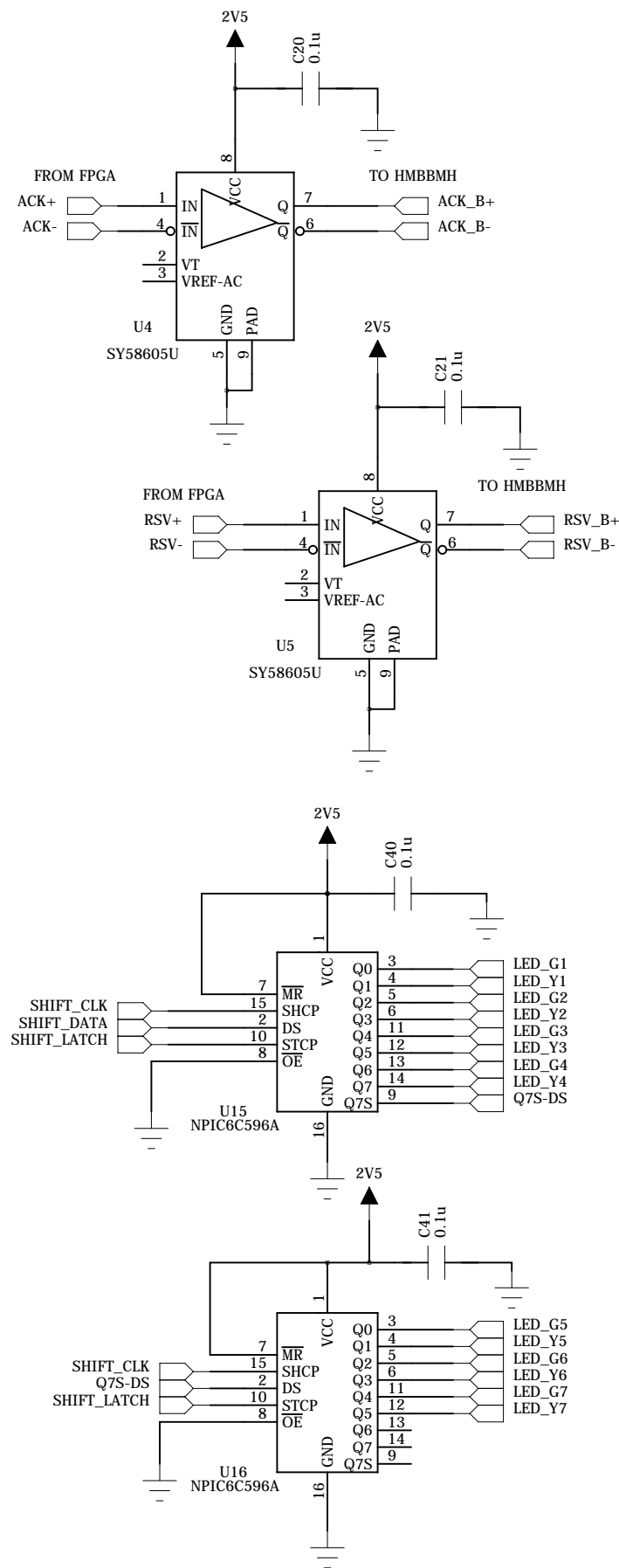
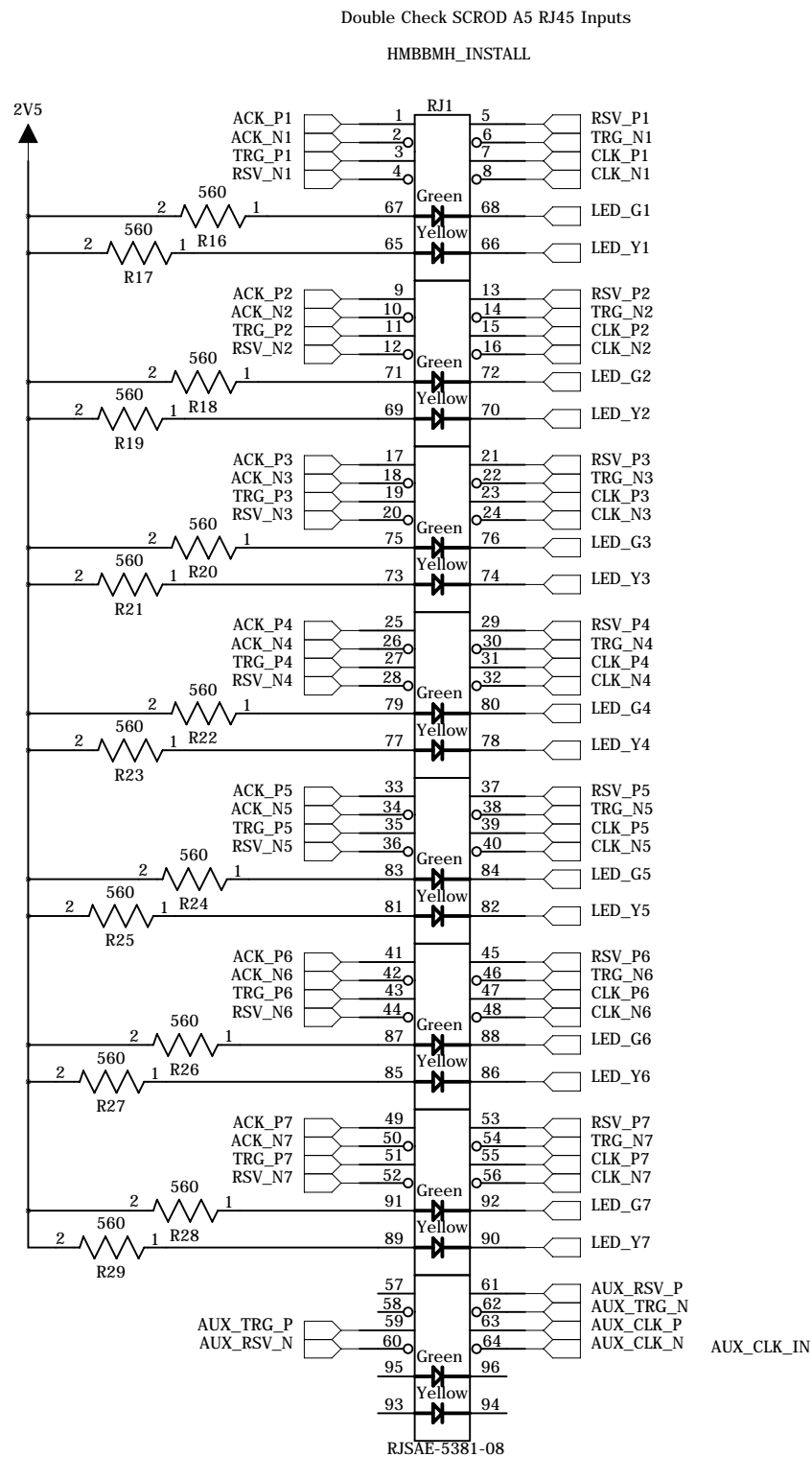
C

B

B

A

A



institution: University of Hawaii at Manoa
High Energy Physics Lab
Instrumentation Development Lab

title: HMB_BMH
revision: A
IDLAB design #: IDL_17_010
circuit design: JLB
PCB design: JLB

sheet #: 2 of 10
sheet description: RJ45
date last modified: June 2, 2017

6

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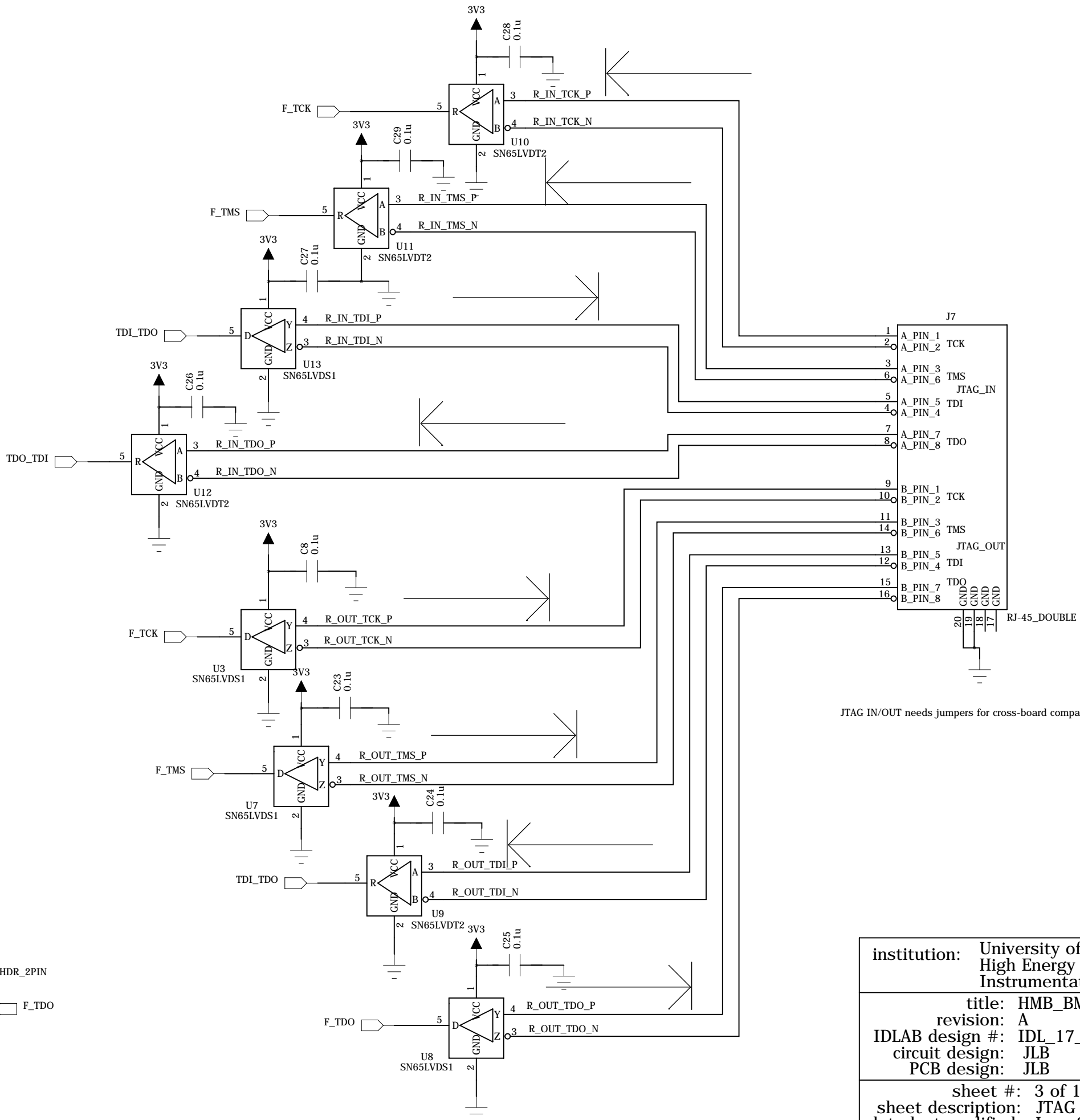
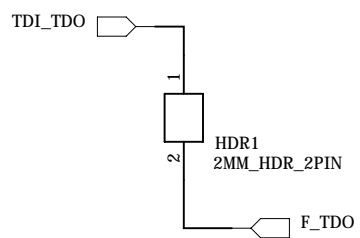
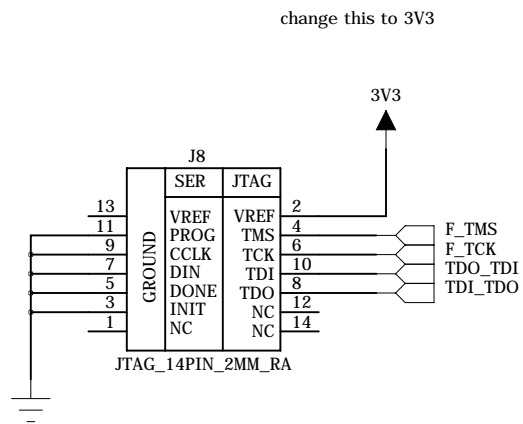
C

B

B

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A



JTAG IN/OUT needs jumpers for cross-board compatibility

institution:	University of Hawaii at Manoa High Energy Physics Lab Instrumentation Development Lab
title:	HMB_BMH
revision:	A
IDLAB design #:	IDL_17_010
circuit design:	JLB
PCB design:	JLB
sheet #:	3 of 10
sheet description:	JTAG
date last modified:	June 2, 2017

6

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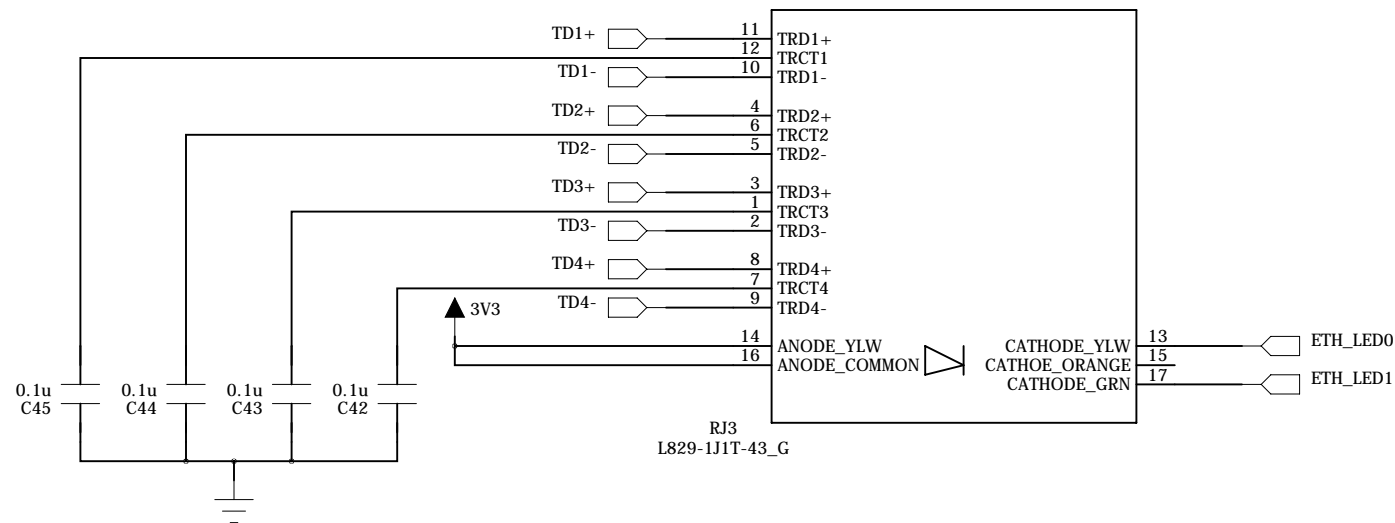
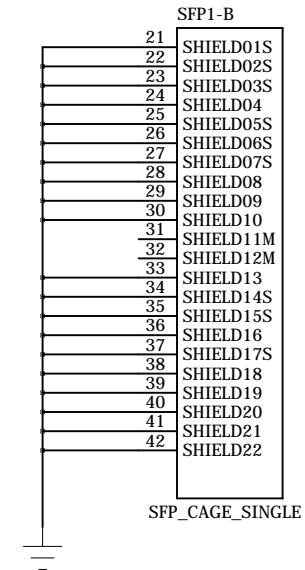
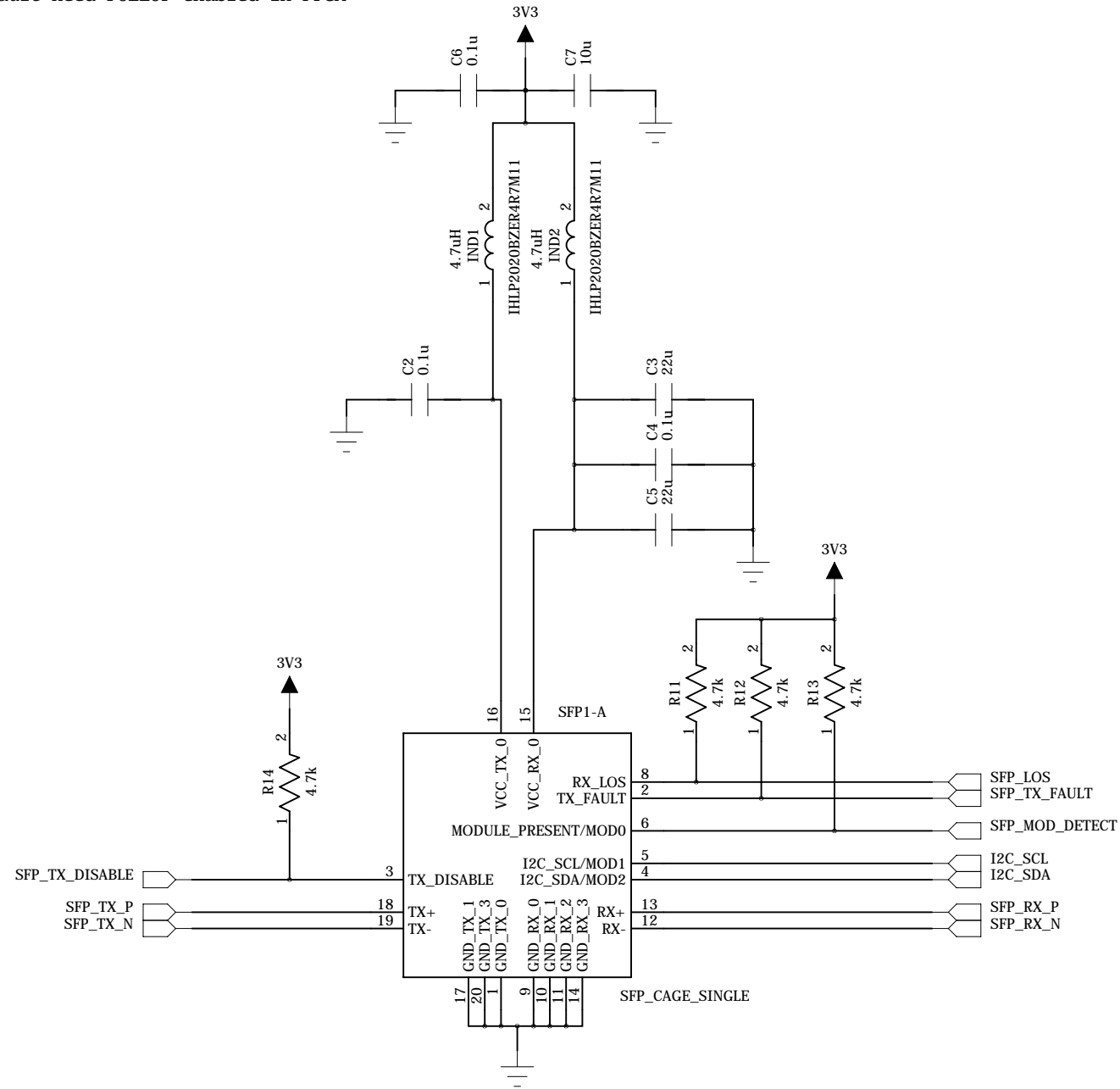
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each AFBR-57D7APZ uses 235mA
 trig_present and data_present need PULLUP enabled in FPGA
 data_tx_fault and trig_tx_fault need PULLUP enabled in FPGA



institution:	University of Hawaii at Manoa High Energy Physics Lab Instrumentation Development Lab
title:	HMB_BMH
revision:	A
IDLAB design #:	IDL_17_010
circuit design:	JLB
PCB design:	JLB
sheet #:	4 of 10
sheet description:	Fiber Optics
date last modified:	June 2, 2017

6

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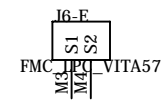
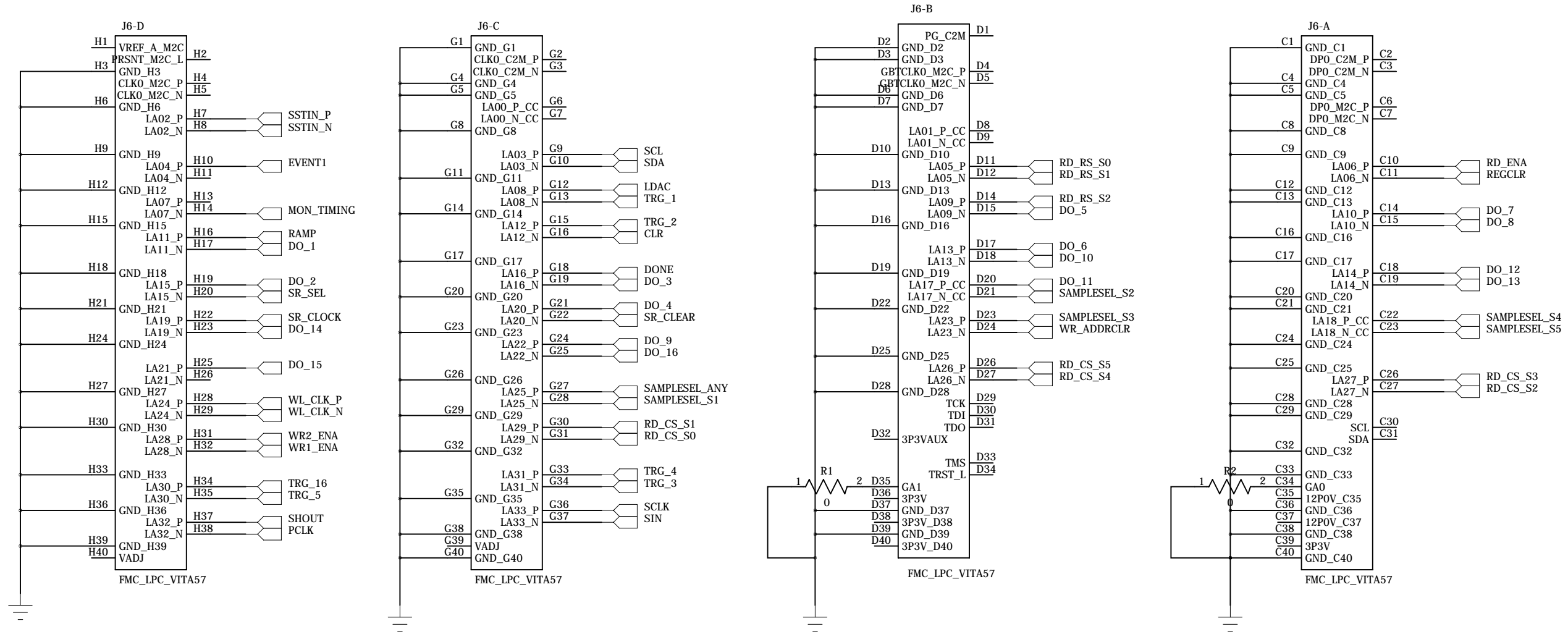
C

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A

A



institution:	University of Hawaii at Manoa High Energy Physics Lab Instrumentation Development Lab
title:	HMB_BMH
revision:	A
IDLAB design #:	IDL_17_010
circuit design:	JLB
PCB design:	JLB
sheet #:	5 of 10
sheet description:	FMC Carrier Connector
date last modified:	June 2, 2017

6

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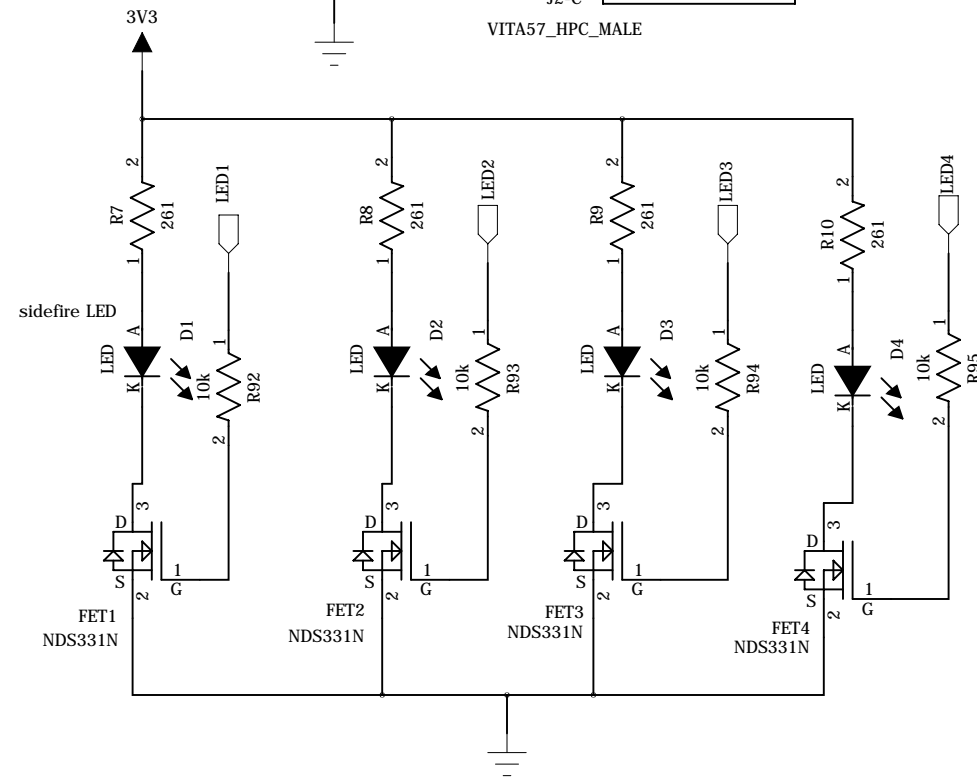
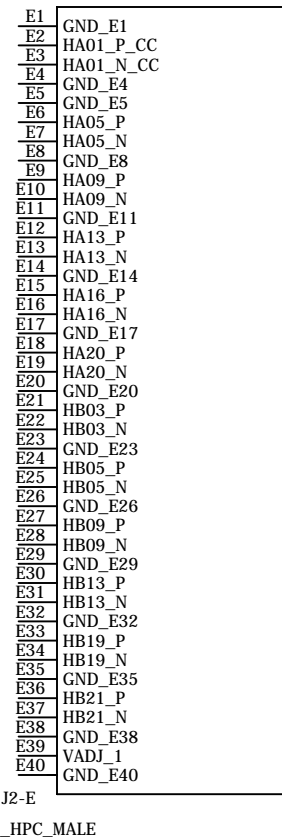
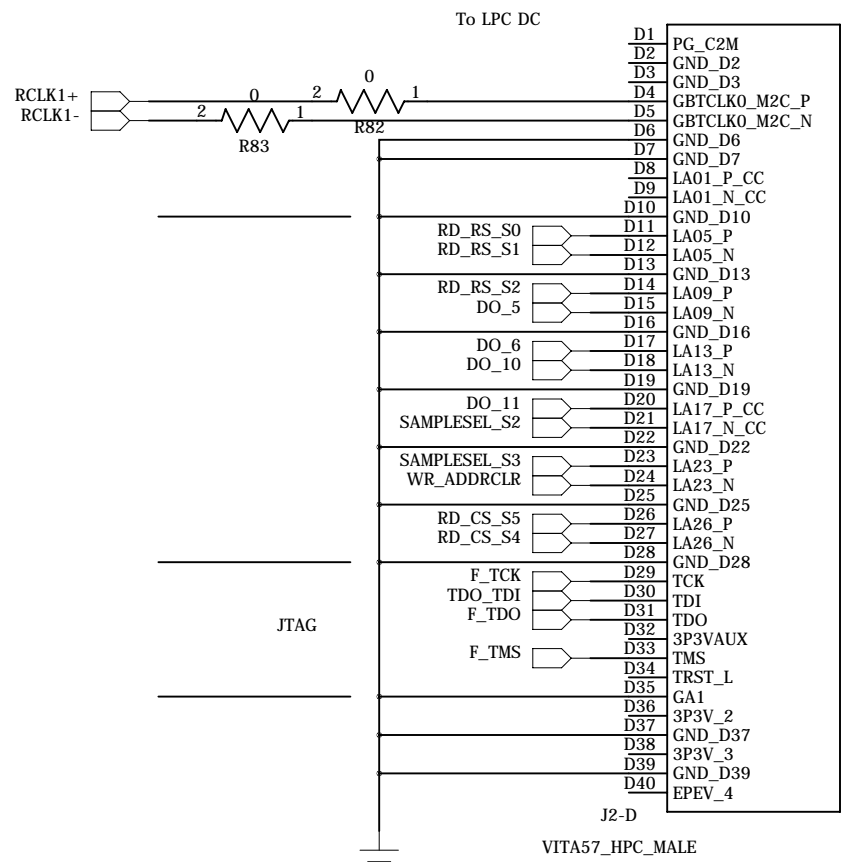
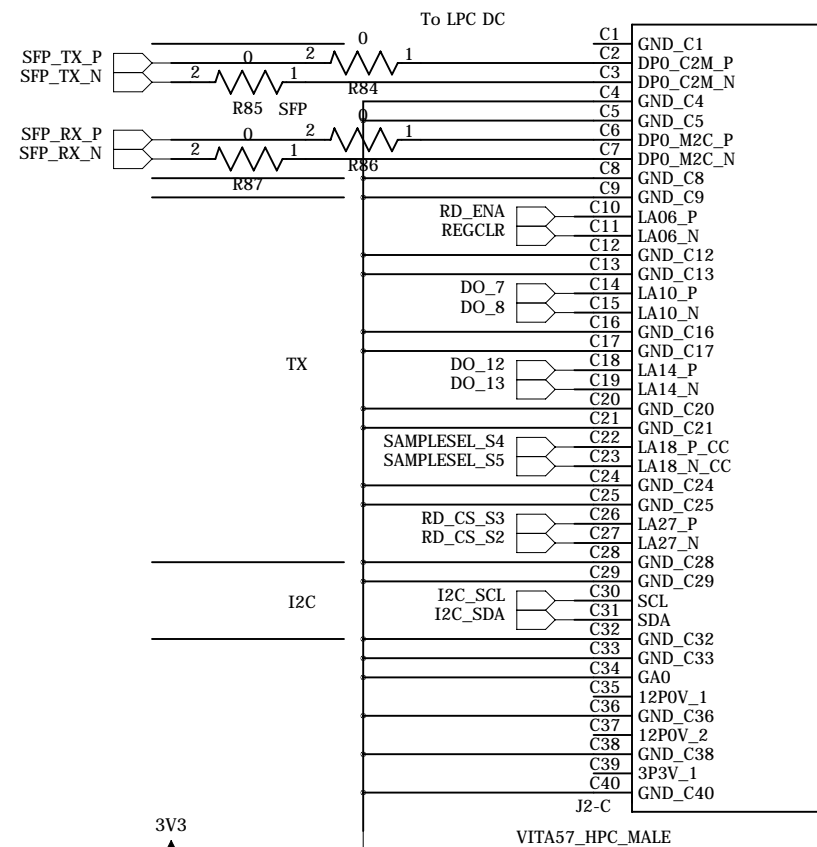
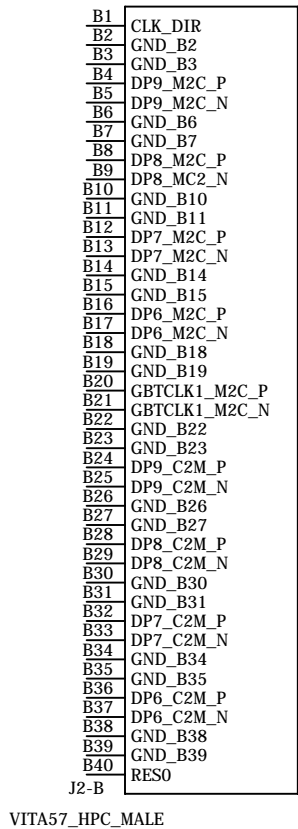
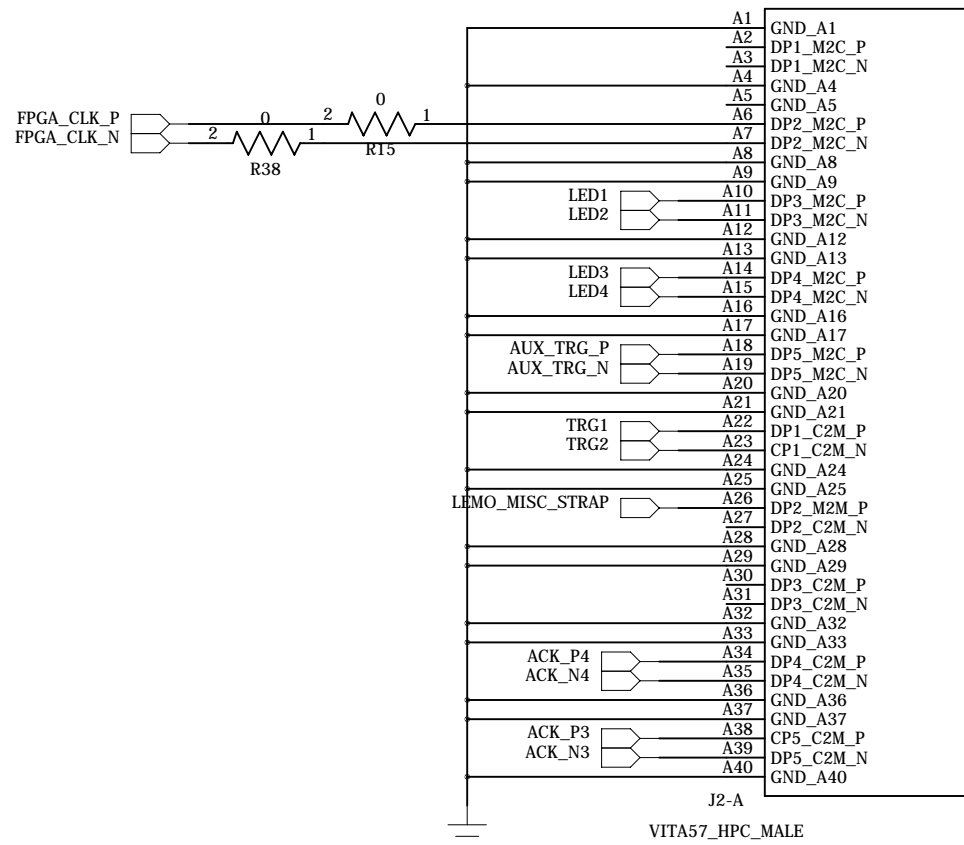
C

B

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A

A



institution: University of Hawaii at Manoa
High Energy Physics Lab
Instrumentation Development Lab

title: HMB_BMH
revision: A
IDLAB design #: IDL_17_010
circuit design: JLB
PCB design: JLB

sheet #: 6 of 10
sheet description: HPC Male A
date last modified: June 2, 2017

E

D

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A

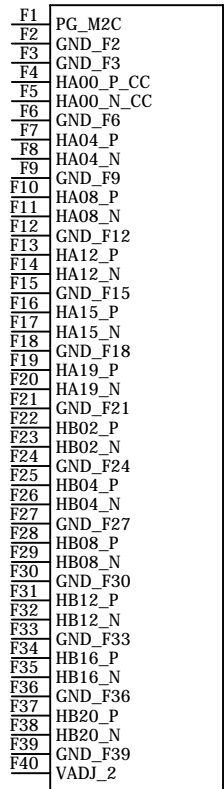
E

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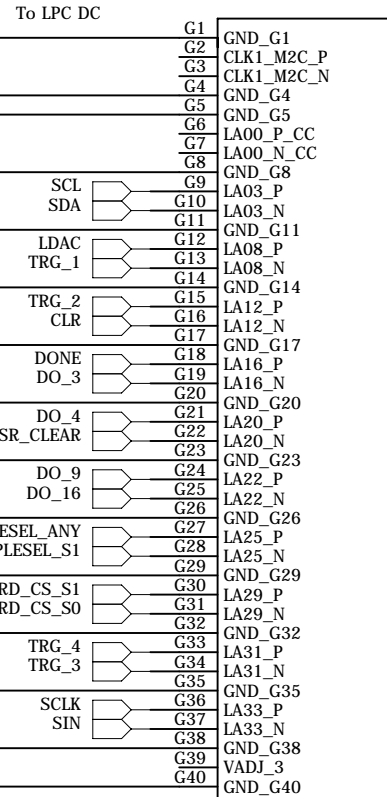
A



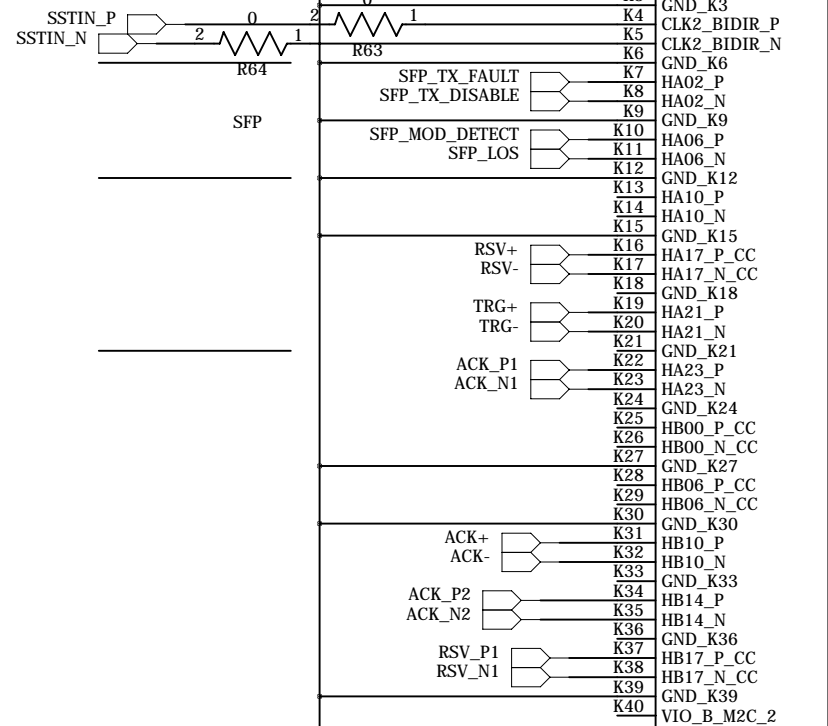
J2-F
VITA57_HPC_MALE

TX_I2C_PERIPHERALS

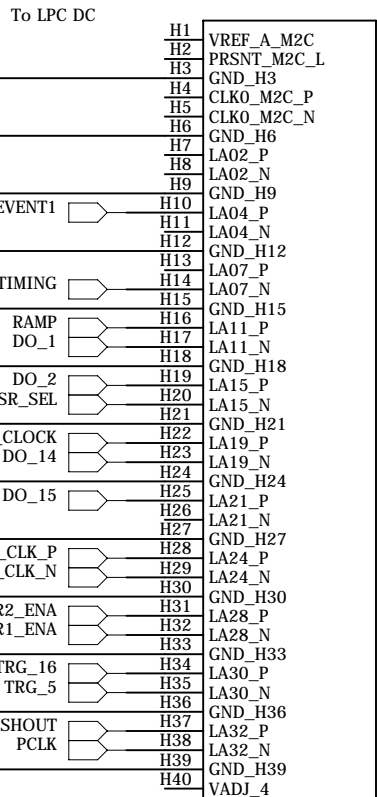
TX



J2-G
VITA57_HPC_MALE

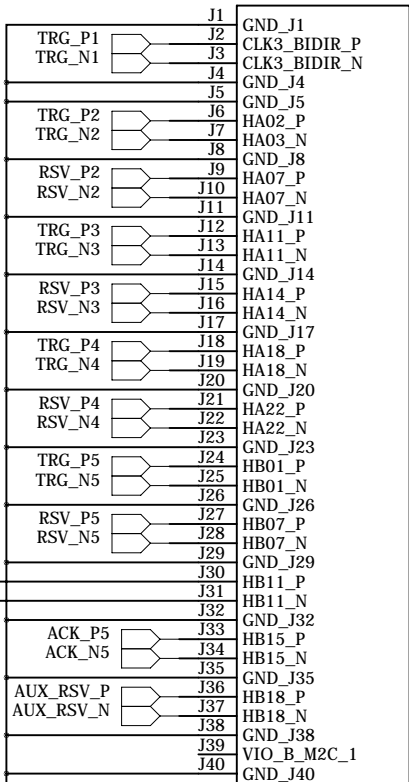
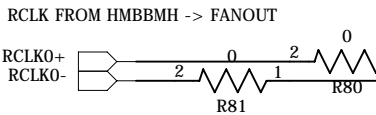


J2-K
VITA57_HPC_MALE

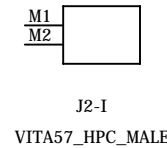


J2-H
VITA57_HPC_MALE

TX



J2-J
VITA57_HPC_MALE



institution: University of Hawaii at Manoa
High Energy Physics Lab
Instrumentation Development Lab

title: HMB_BMH

revision: A

IDLAB design #: IDL_17_010

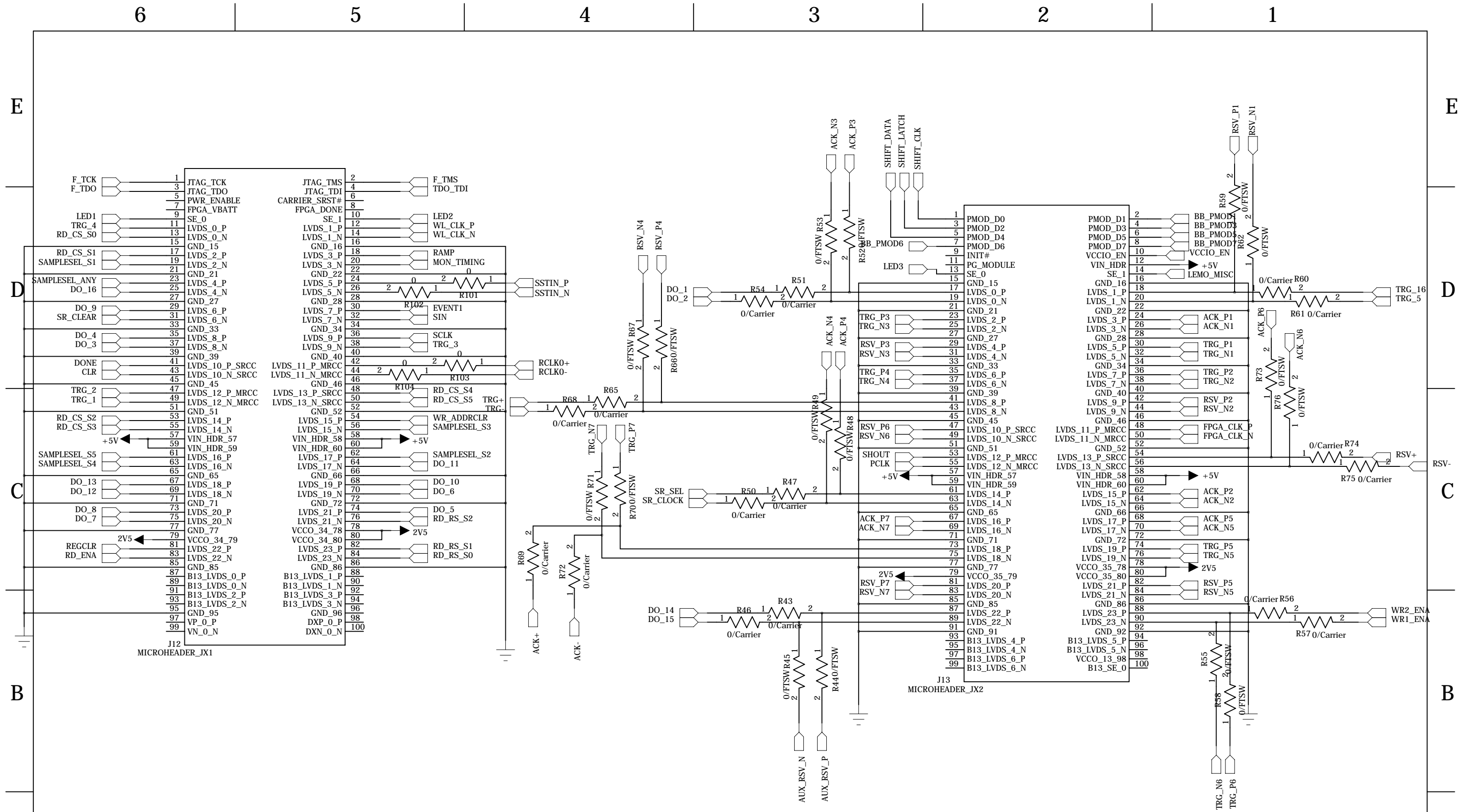
circuit design: JLB

PCB design: JLB

sheet #: 7 of 10

sheet description: HPC Male B

date last modified: June 2, 2017



institution:	University of Hawaii at Manoa High Energy Physics Lab Instrumentation Development Lab
title:	HMB_BMH
revision:	A
IDLAB design #:	IDL_17_010
circuit design:	JLB
PCB design:	JLB
sheet #:	8 of 10
sheet description:	CONN Microzed
date last modified:	June 2, 2017

6

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E

E

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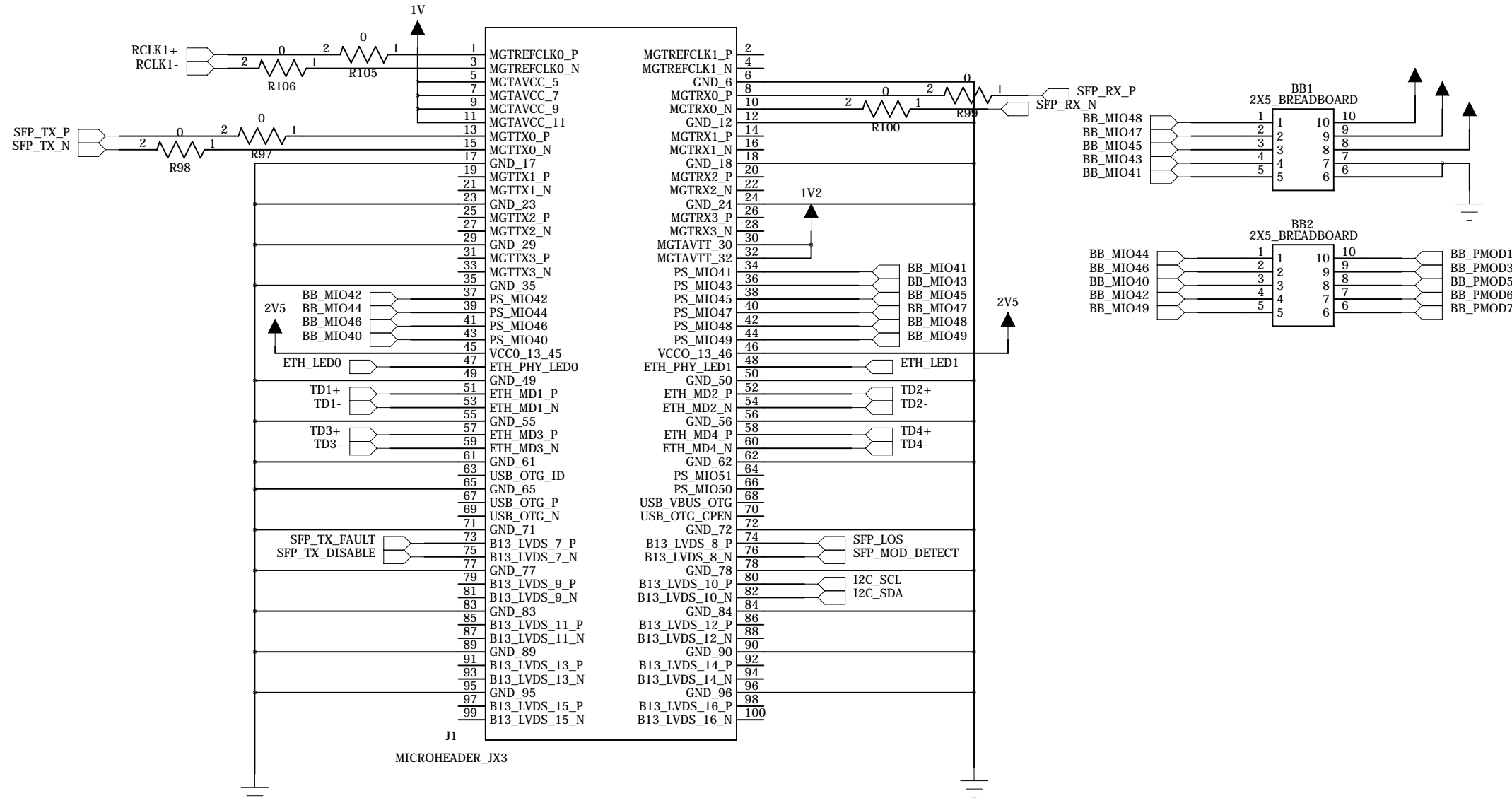
C

B

B

A

A



institution:	University of Hawaii at Manoa High Energy Physics Lab Instrumentation Development Lab
title:	HMB_BMH
revision:	A
IDLAB design #:	IDL_17_010
circuit design:	JLB
PCB design:	JLB
sheet #:	9 of 10
sheet description:	CONN Picozed
date last modified:	June 2, 2017

E

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C

B

A

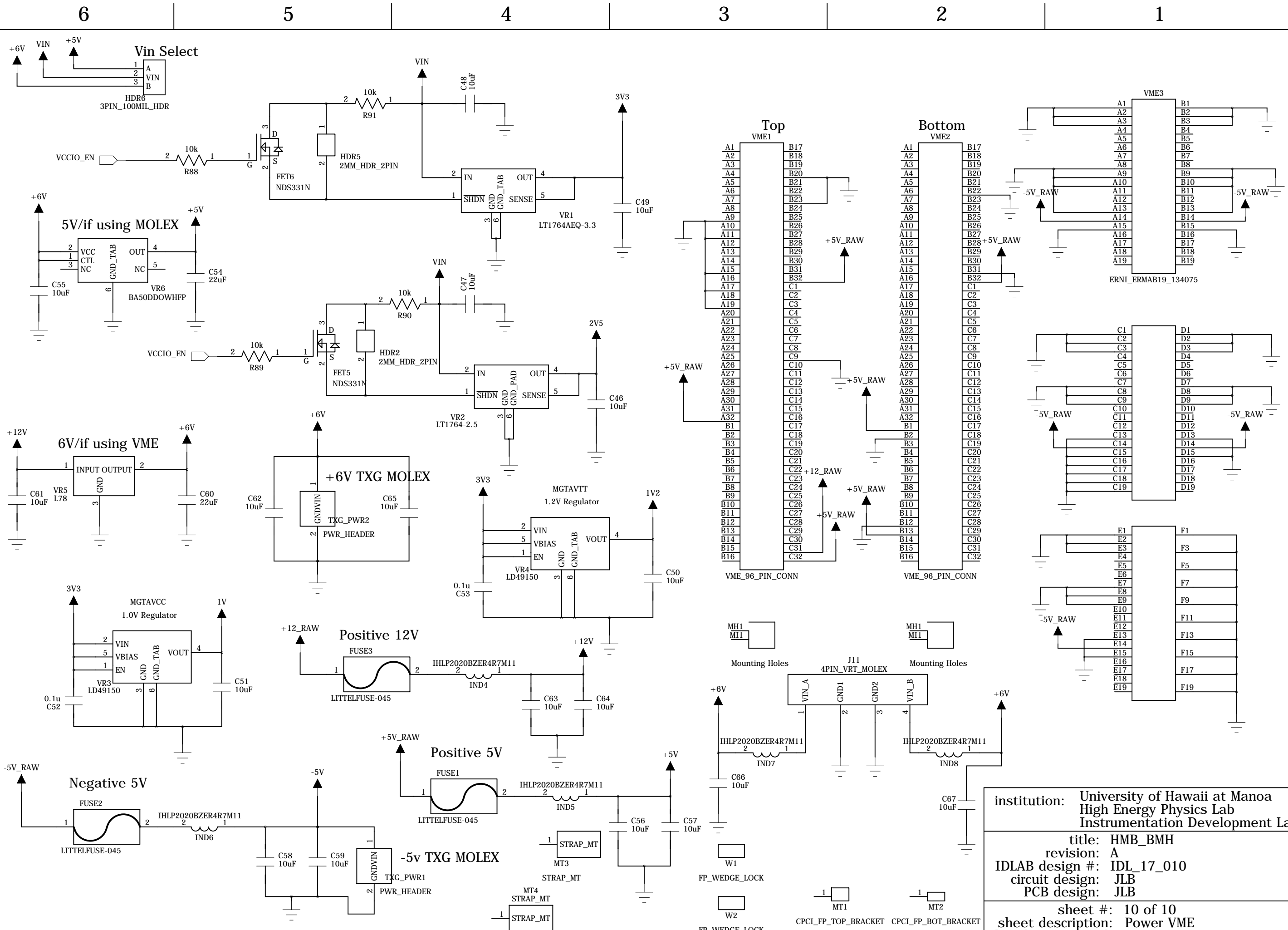
E

D

C

B

A



institution: University of Hawaii at Manoa
 High Energy Physics Lab
 Instrumentation Development Lab

title: HMB_BMH
 revision: A
 IDLAB design #: IDL_17_010
 circuit design: JLB
 PCB design: JLB

sheet #: 10 of 10
 sheet description: Power VME
 date last modified: June 2, 2017