

6

5

provides power to 4

3

2

1

E

E

D

D

C

C

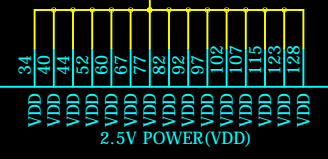
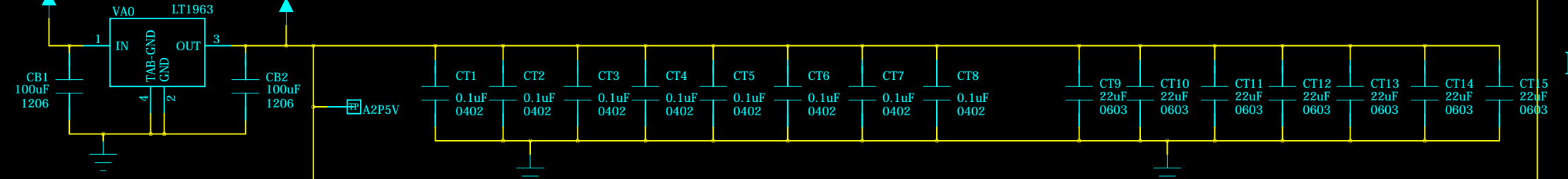
B

B

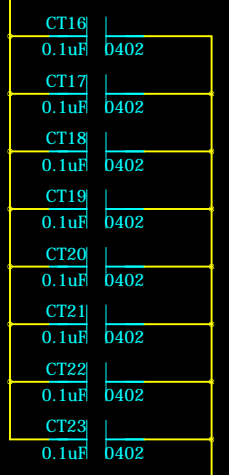
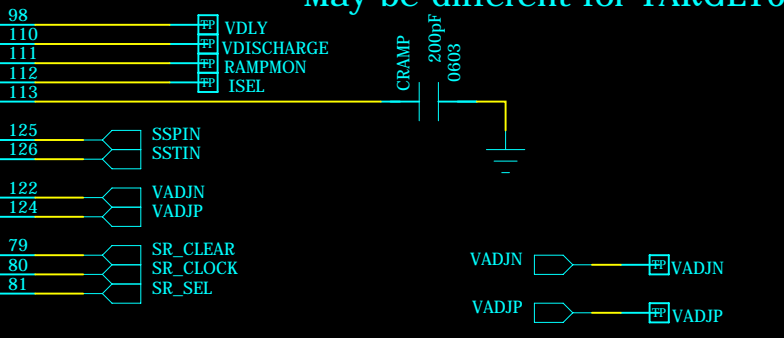
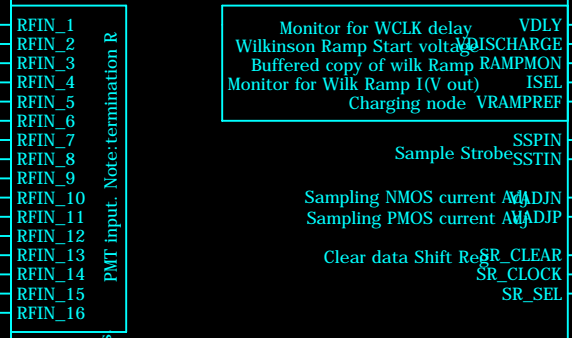
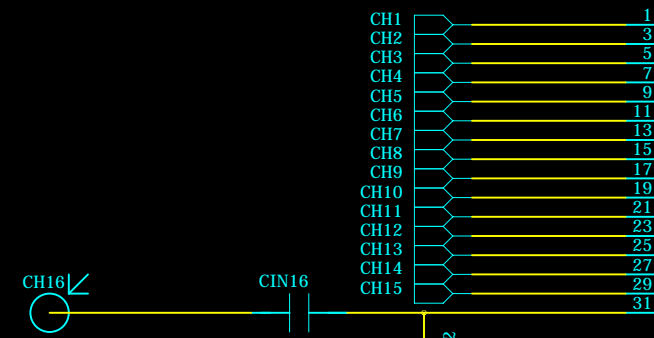
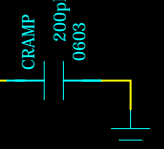
A

A

320mV max dropout
A2.5V

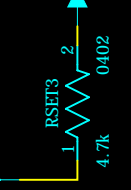


200pF for TARGET4
May be different for TARGET6



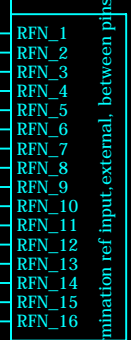
A2.5V

REGCLR

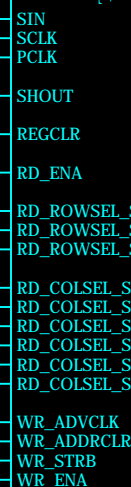


the pullup is so all the registers are cleared (even when FPGA not present)

Termination ref input, external, between pins



PMT input. Note: termination R



Start Wilkinson Conversion
Clear Wilkinson Counters



institution:	University of Hawaii at Manoa High Energy Physics Lab Instrumentation Development Lab
title:	T6 KLM Readout Daughtercard
revision:	B
IDLAB design #:	IDL_13_032
circuit design:	XS
PCB design:	XS
sheet #:	1 of 5
sheet description:	
date last modified:	6-28-2013

6

5

4

3

2

1

E

E

D

D

C

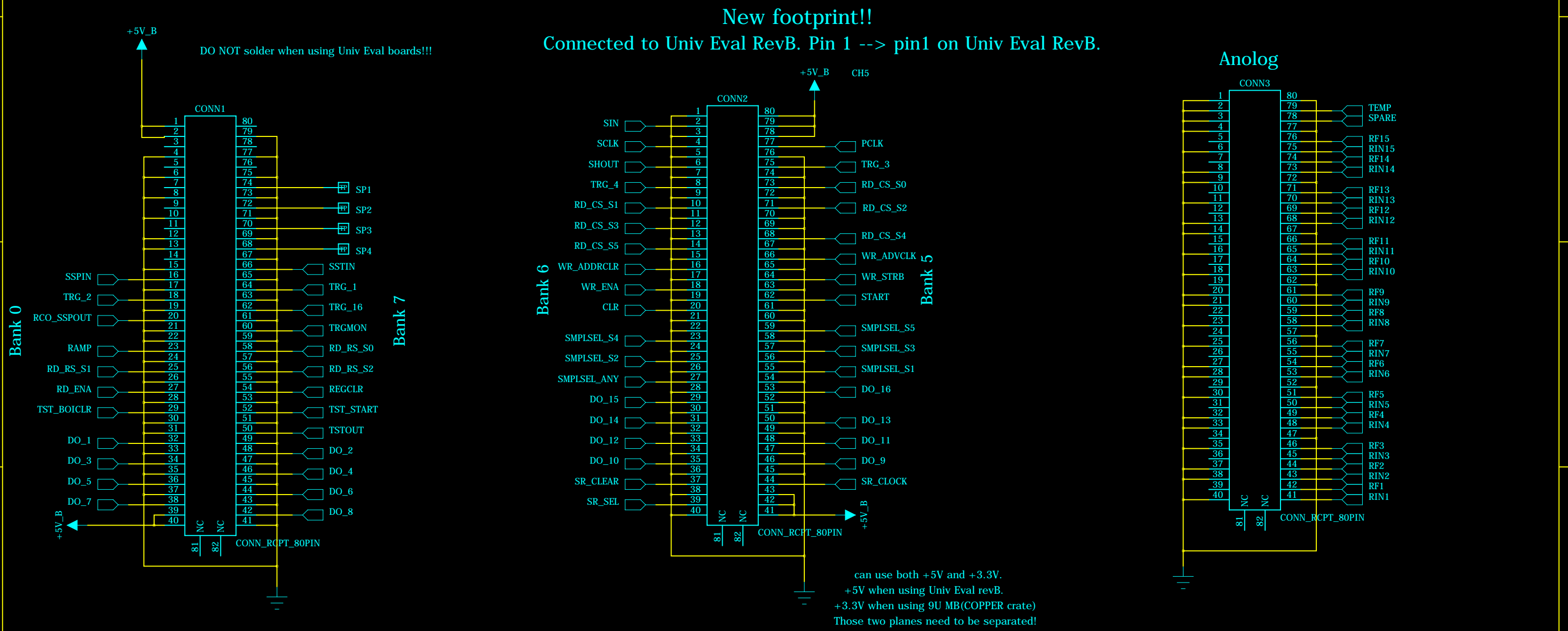
C

B

B

A

A



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IDLAB design #:	IDL_13_032
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5

4

3

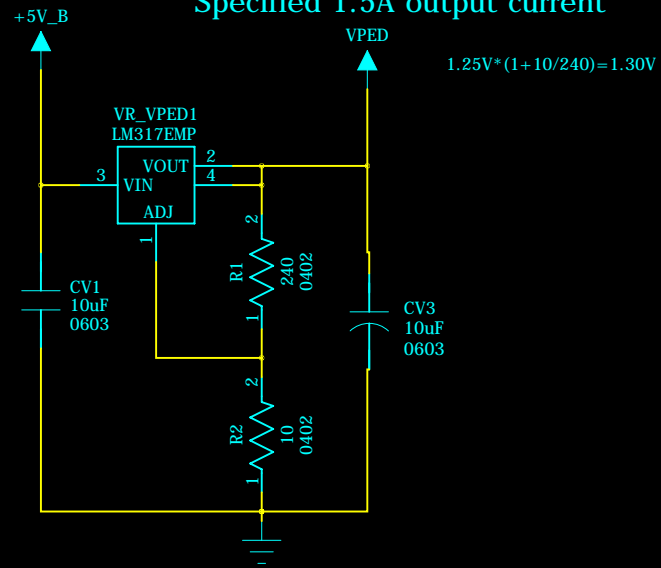
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1

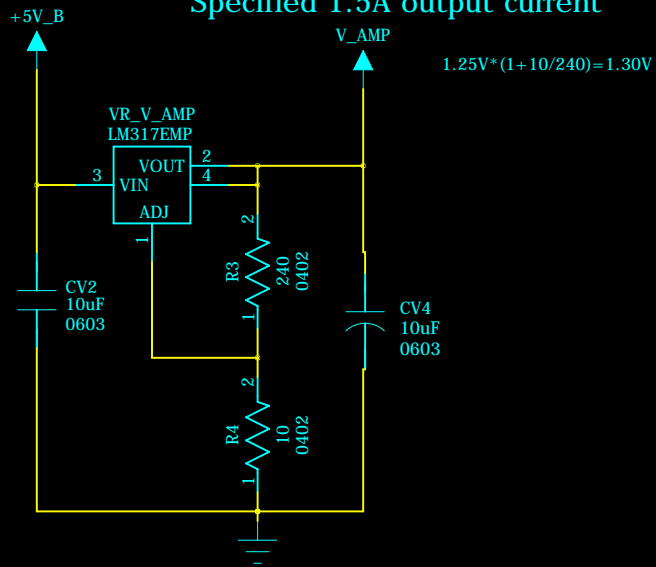
E

E

LM317 input voltage: 4.2V~37V
provides pedestal voltage for ASIC
Specified 1.5A output current



LM317 input voltage: 4.2V~37V
provides ~1.3V for preamps
Specified 1.5A output current



D

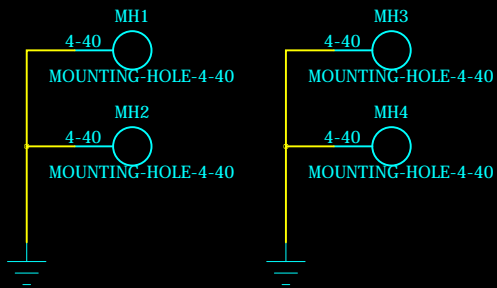
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C

C

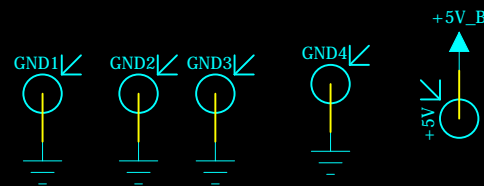
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B



A

A



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5

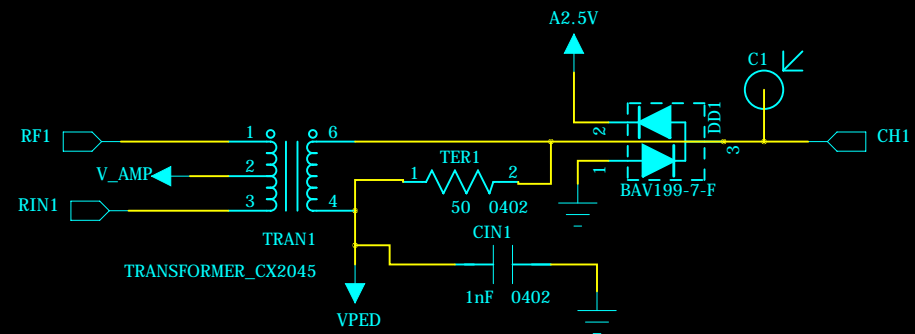
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3

2

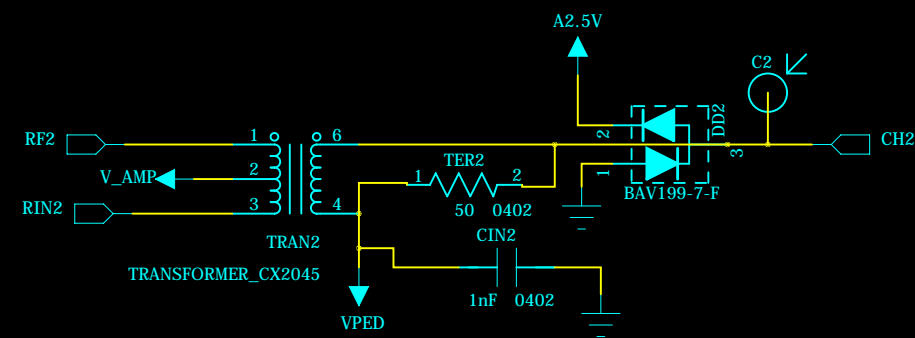
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E



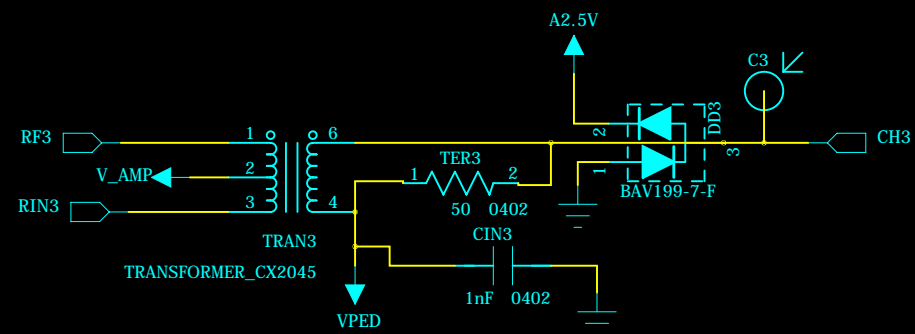
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D



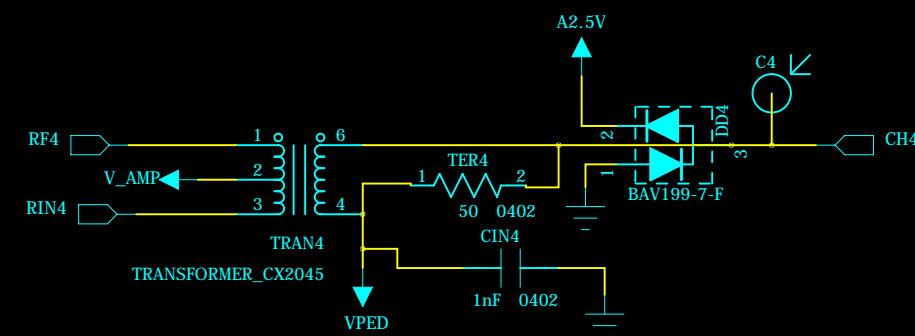
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C



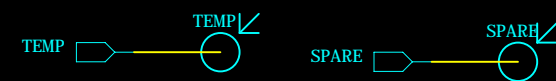
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B

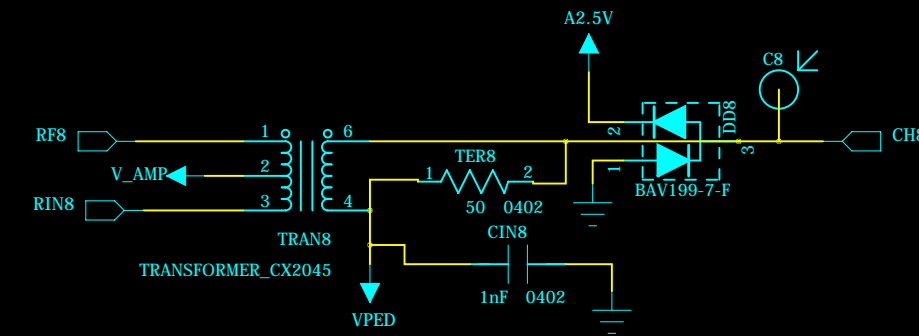
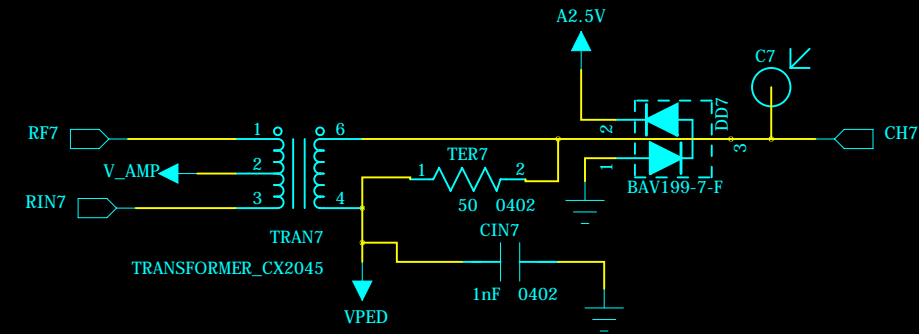
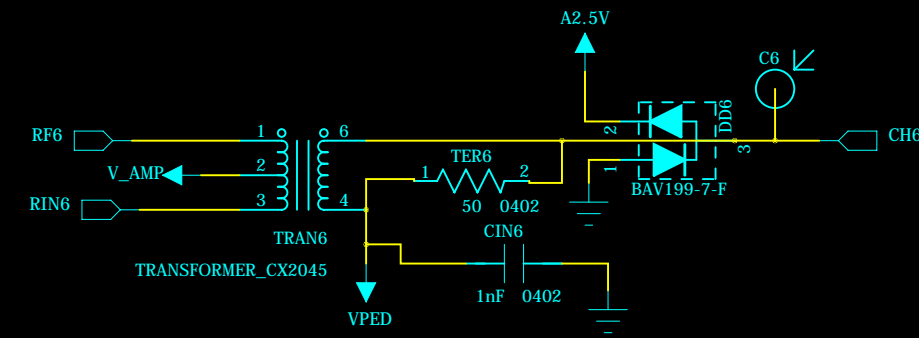
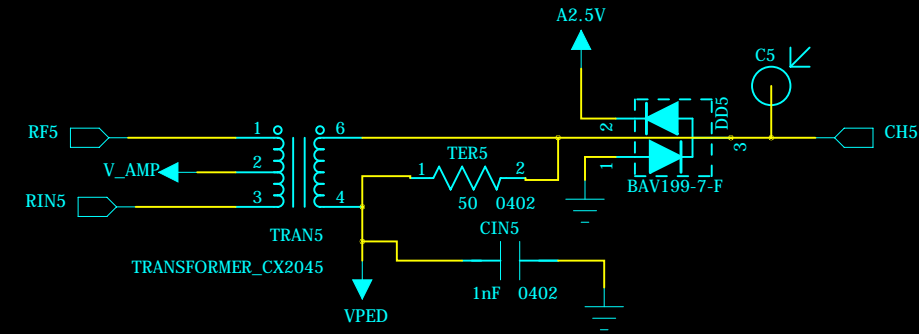


B

A



A



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High Energy Physics Lab
Instrumentation Development Lab

title: T6 KLM Readout Daughtercard
revision: B
IDLAB design #: IDL_13_032
circuit design: XS
PCB design: XS

sheet #: 4 of 5
sheet description:
date last modified: 6-28-2013

6

5

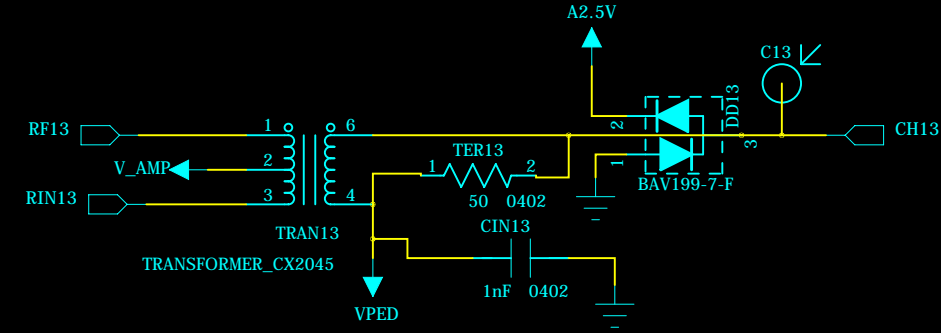
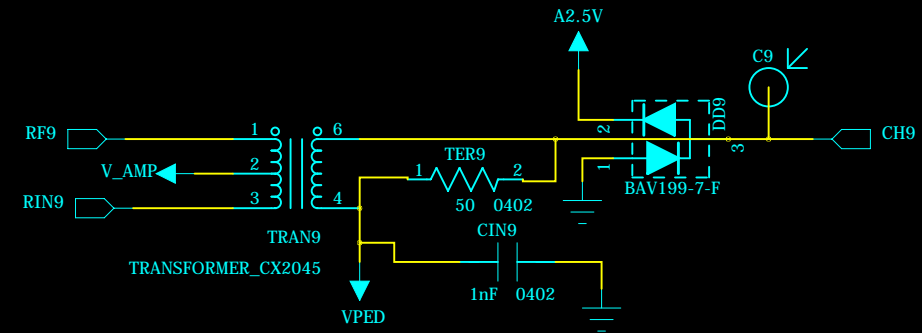
4

3

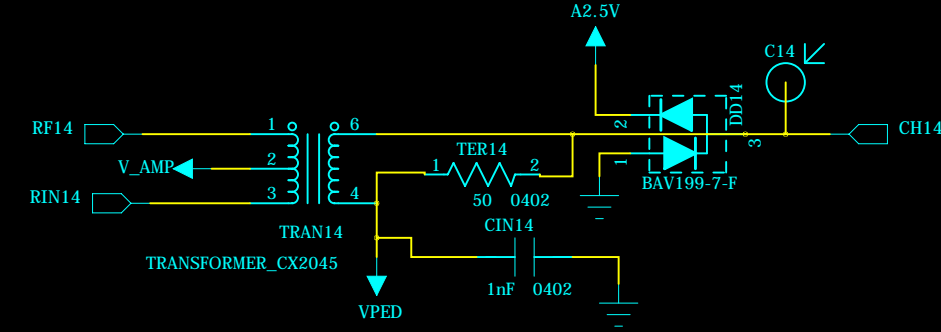
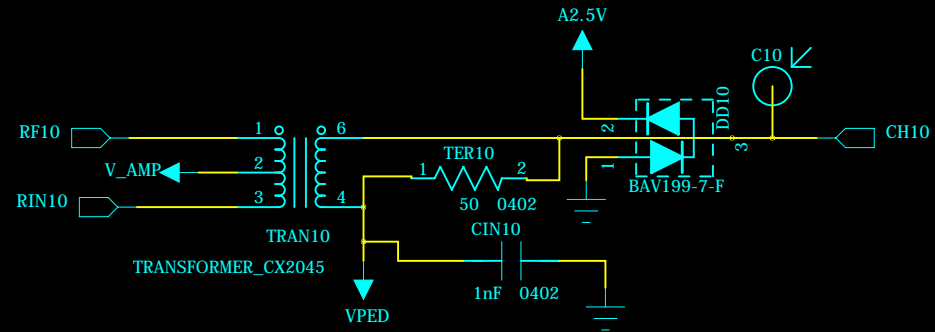
2

1

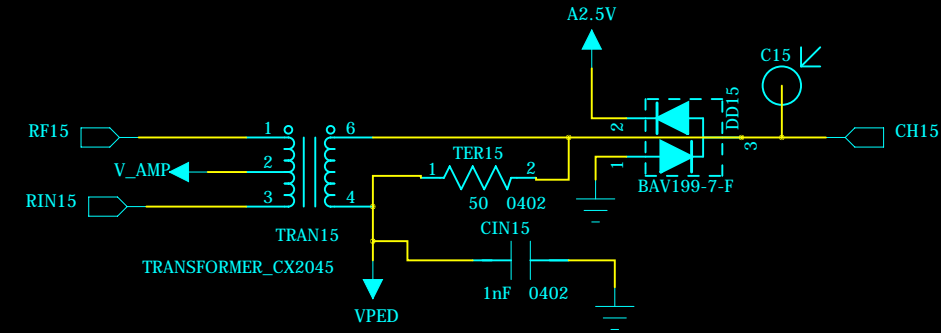
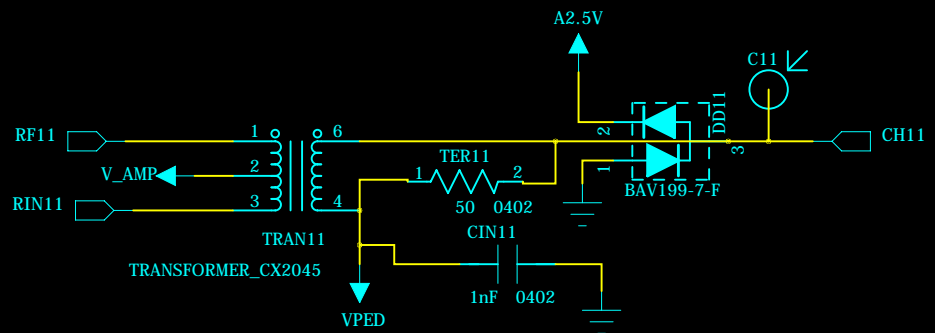
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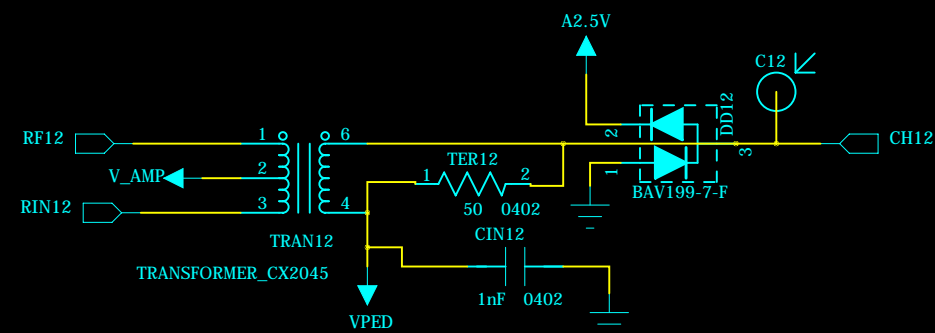
D



C



B



A

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IDLAB design #: IDL_13_032
circuit design: XS
PCB design: XS

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E

D

C

B

A