

6

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4 provides power to ASIC

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C

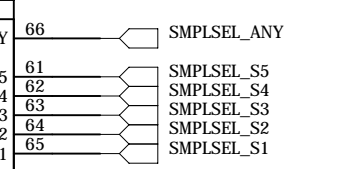
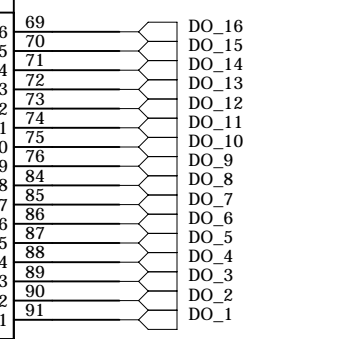
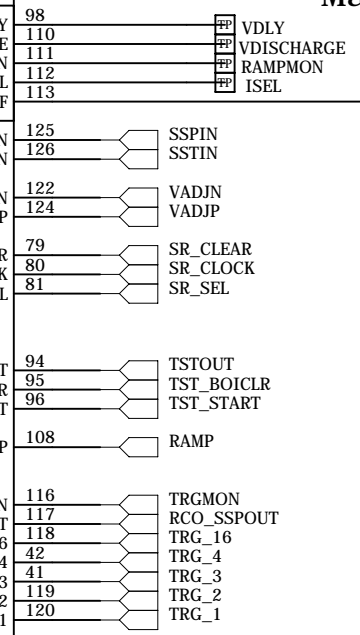
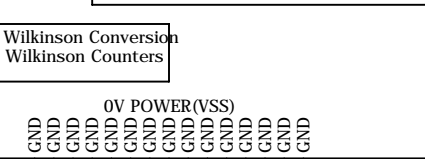
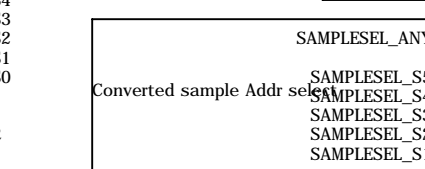
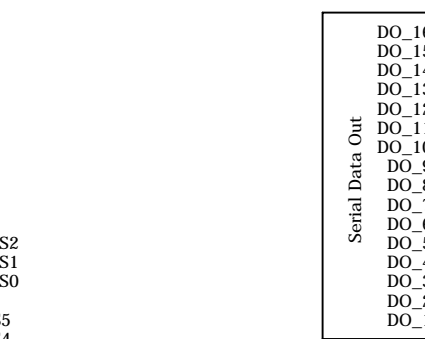
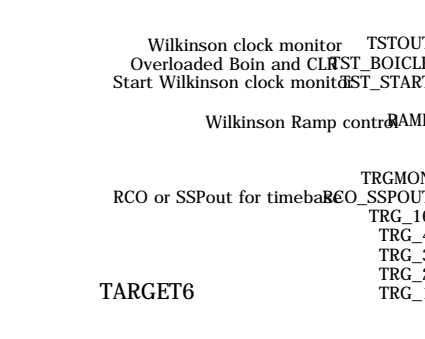
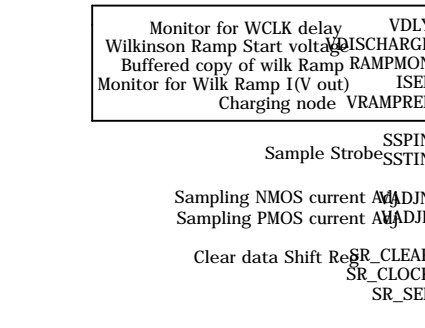
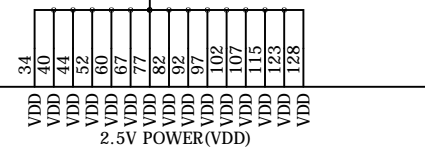
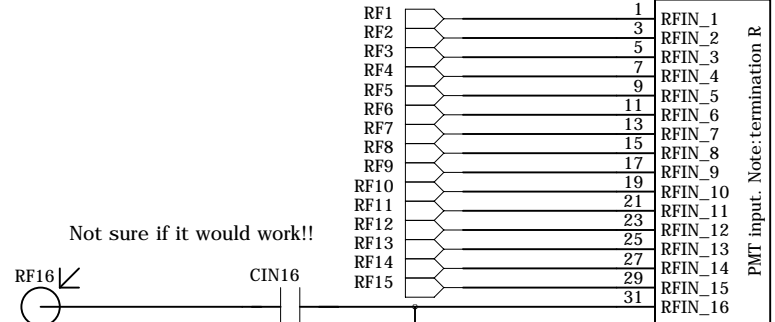
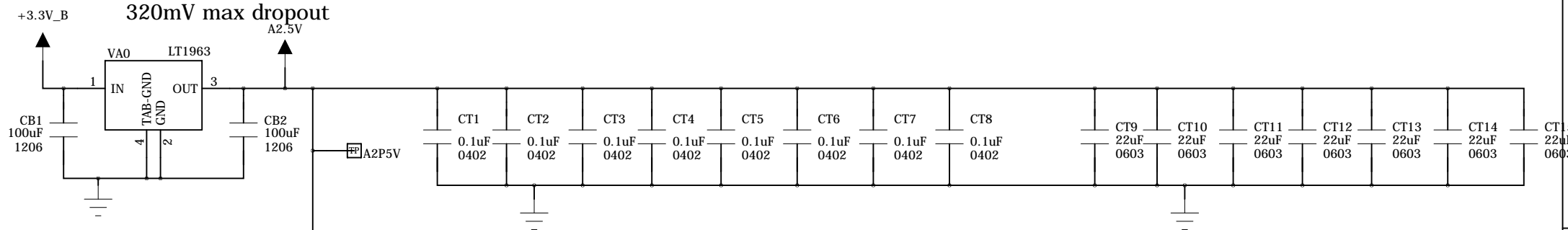
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B

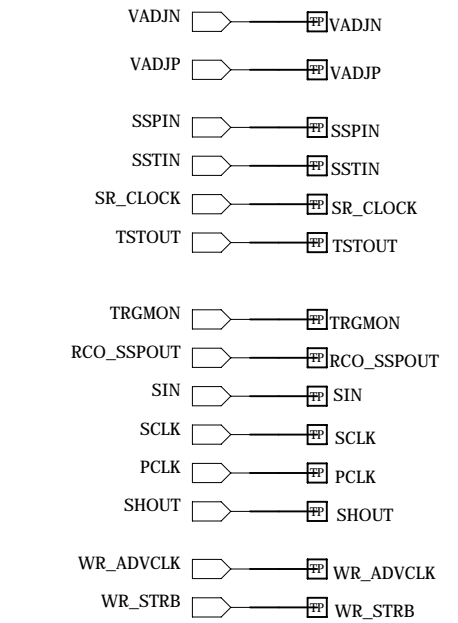
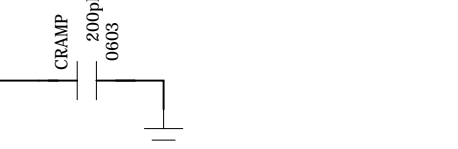
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A

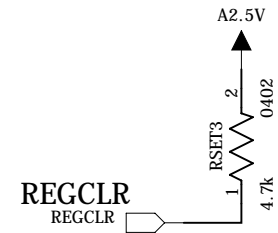
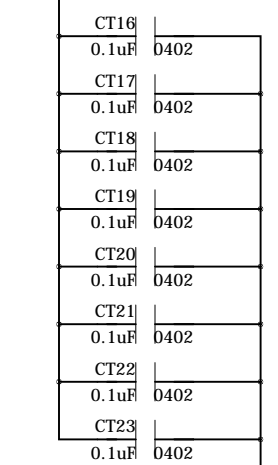
A



200pF for TARGET4  
May be different for TARGET6



VPED



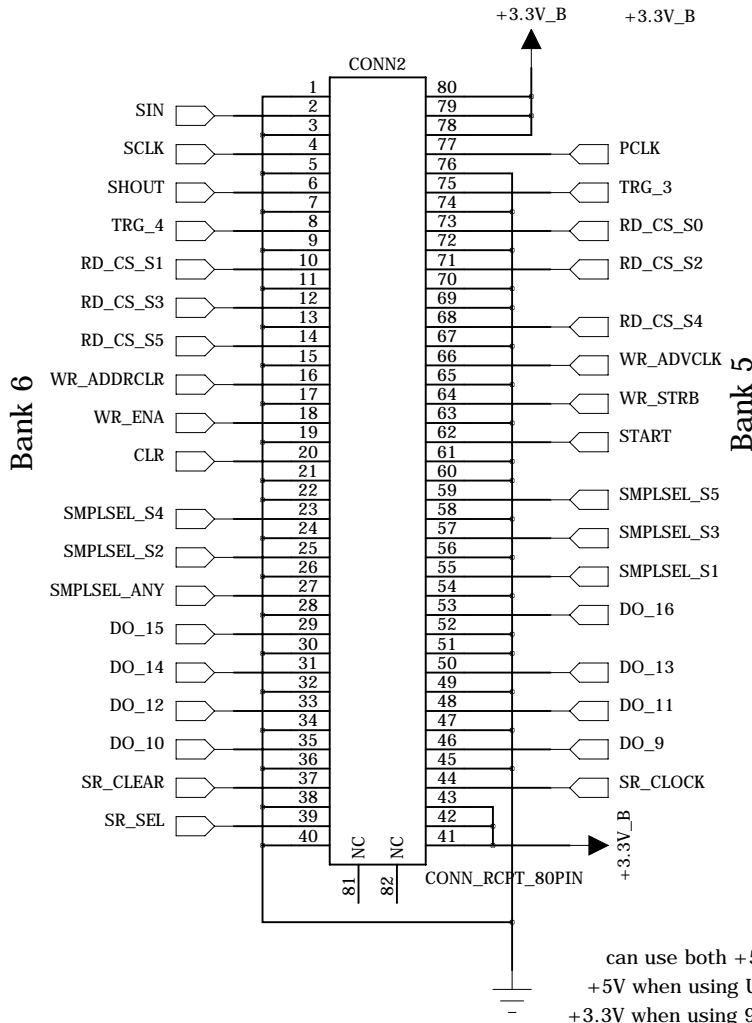
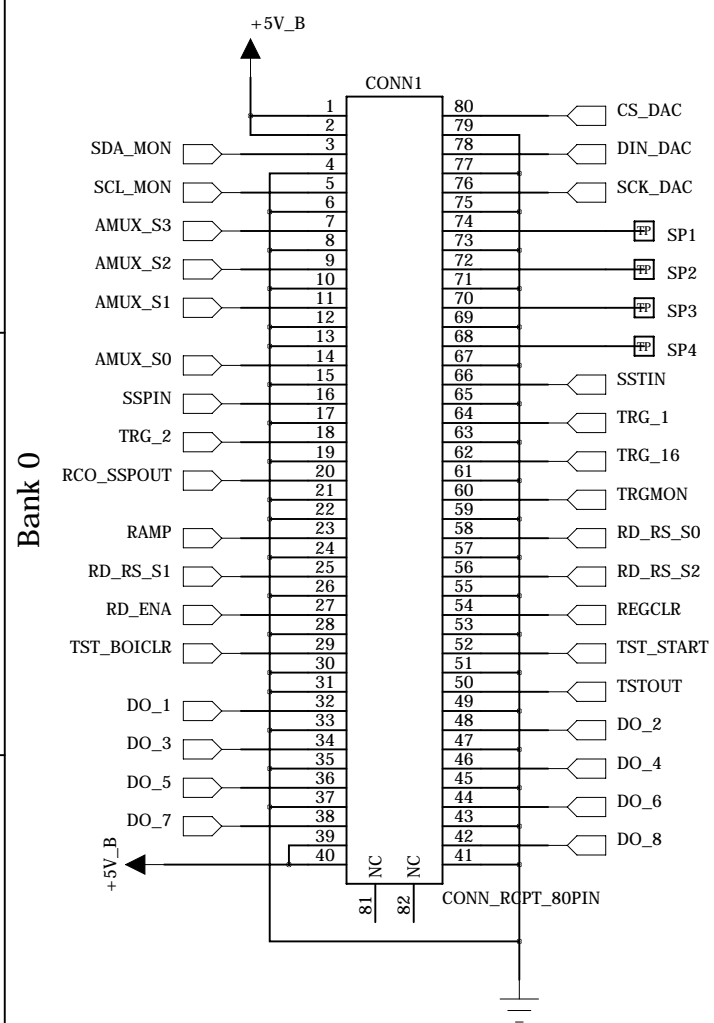
the pullup is so all the registers are cleared (even when FPGA not present)

institution:	University of Hawaii at Manoa High Energy Physics Lab Instrumentation Development Lab
title:	T6 KLM Readout Daughtercard
revision:	A
IDLAB design #:	IDL_13_019
circuit design:	XS
PCB design:	XS
sheet #:	1 of 6
sheet description:	
date last modified:	4-30-2013

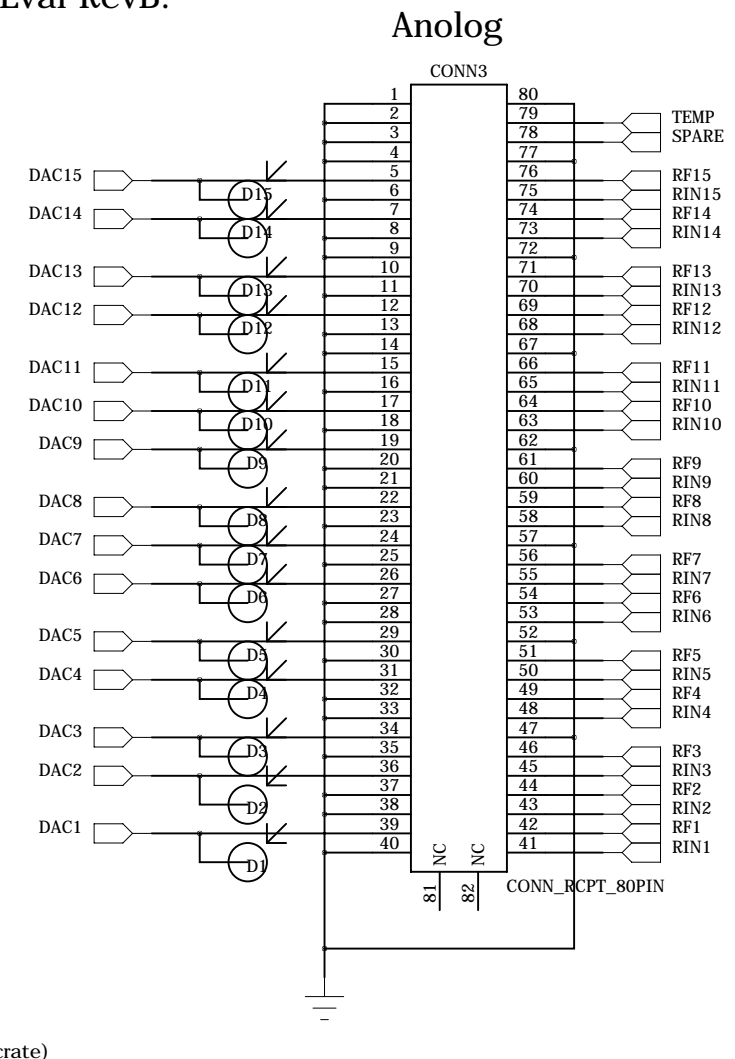
### New footprint!!

Connected to Univ Eval RevB. Pin 1 --> pin1 on Univ Eval RevB.

DO NOT solder when using Univ Eval boards!!!



can use both +5V and +3.3V.  
 +5V when using Univ Eval revB.  
 +3.3V when using 9U MB(COPPER crate)  
 Those two planes need to be separated!



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sheet #:	2 of 6
sheet description:	
date last modified:	4-30-2013

E

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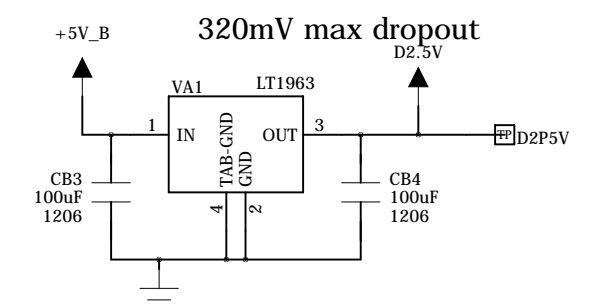
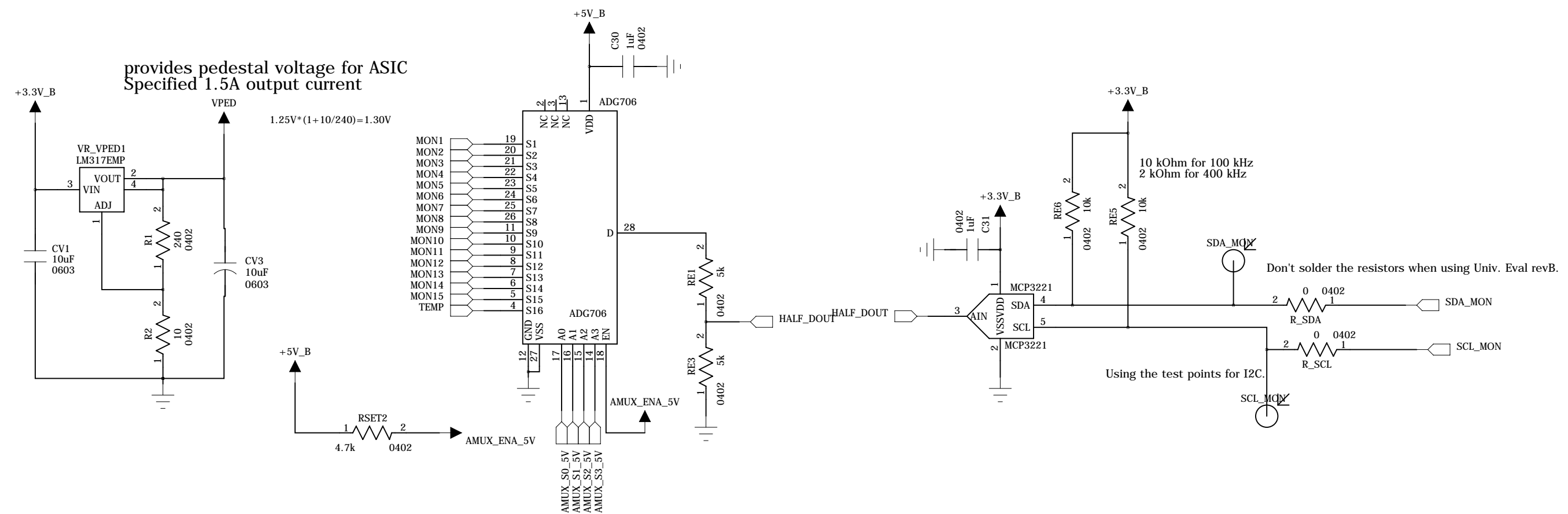
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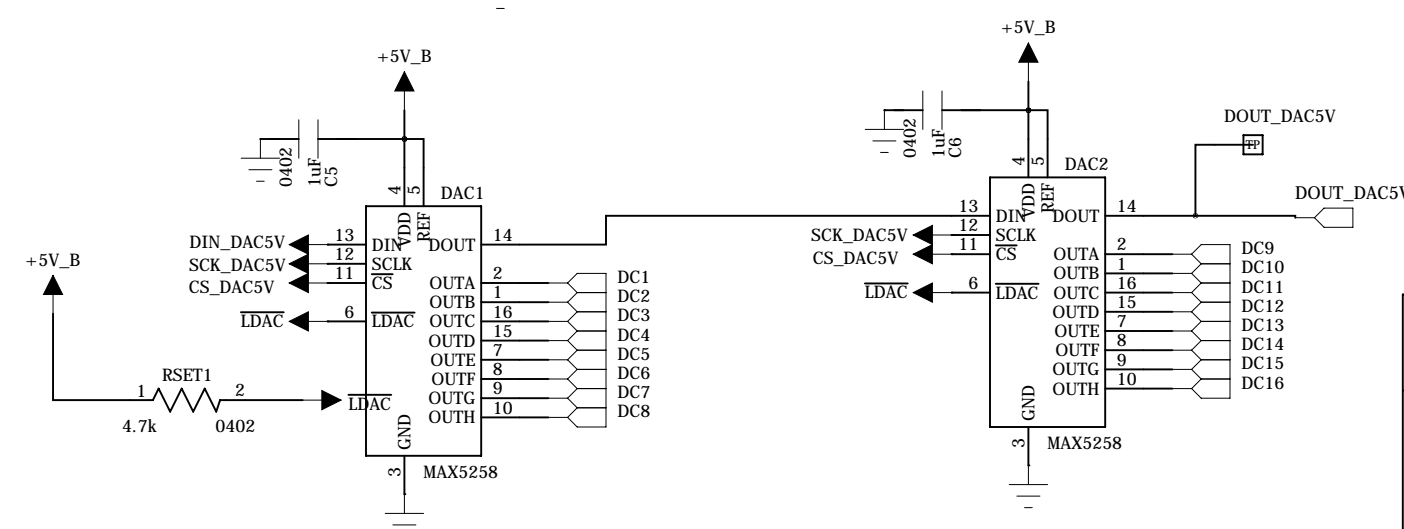
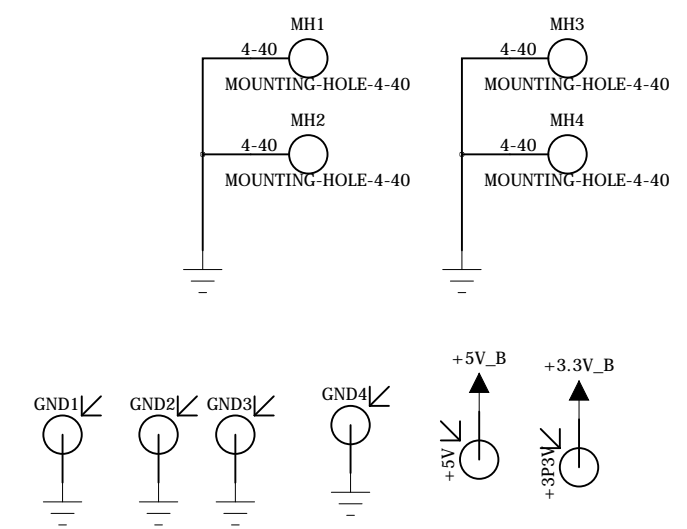
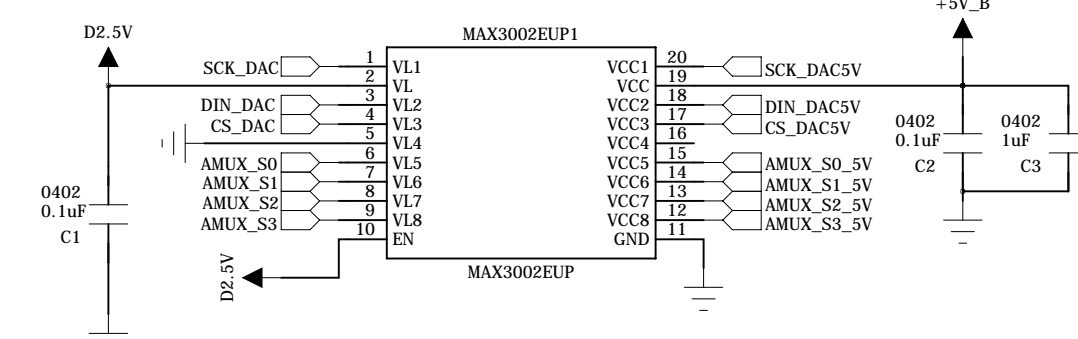
B

A

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To reduce ripple and the chance of transmitting incorrect data, bypass VL and VCC to ground with a 0.1µF



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sheet description:	
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6

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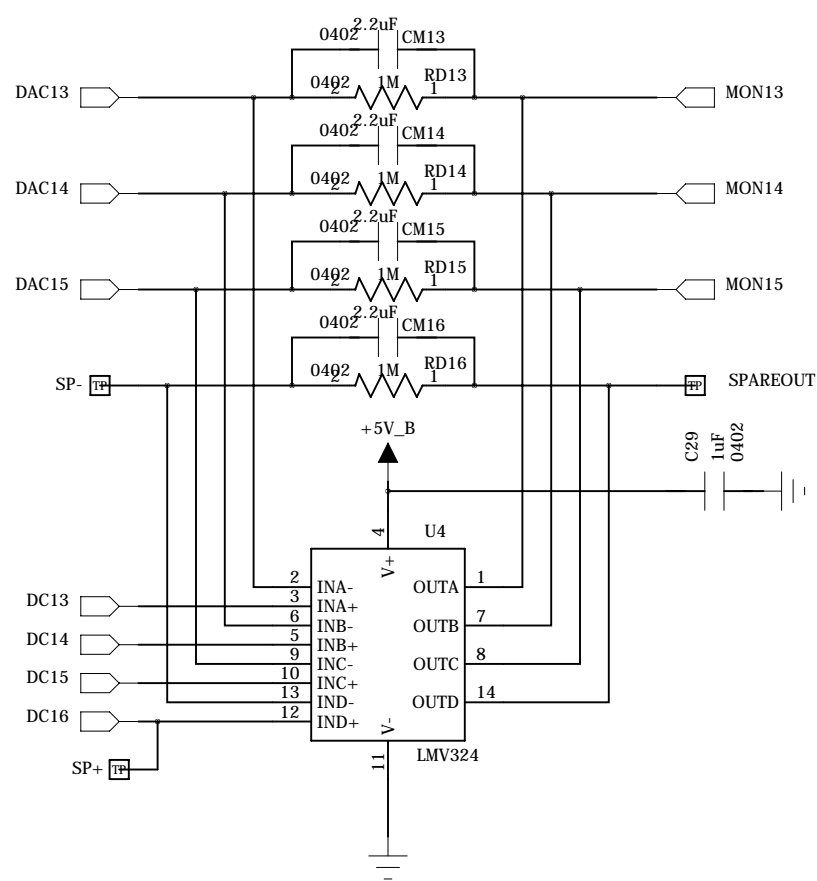
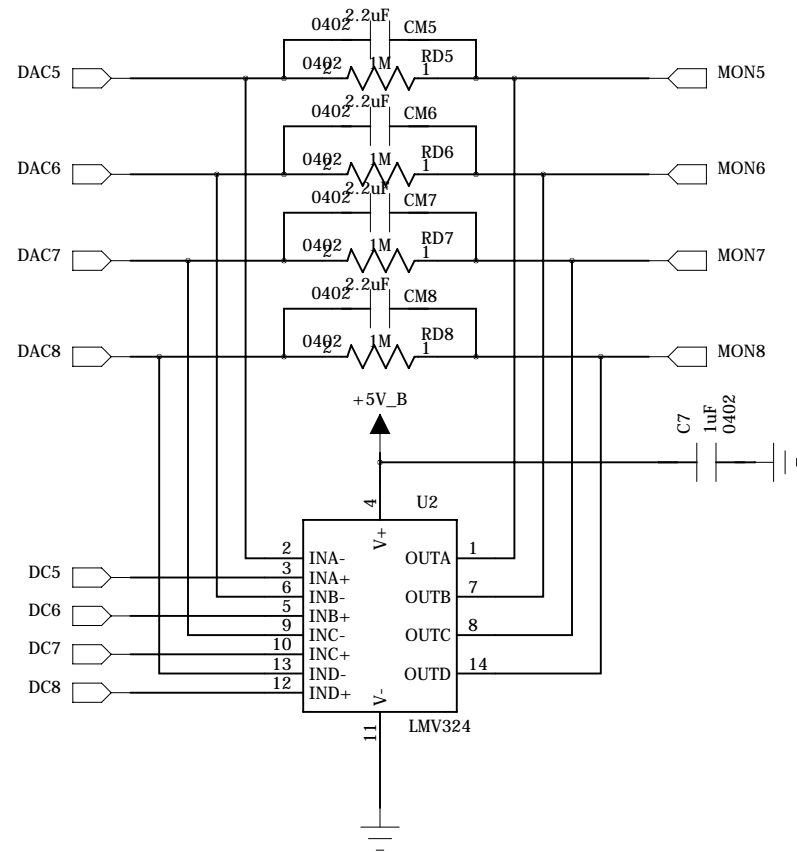
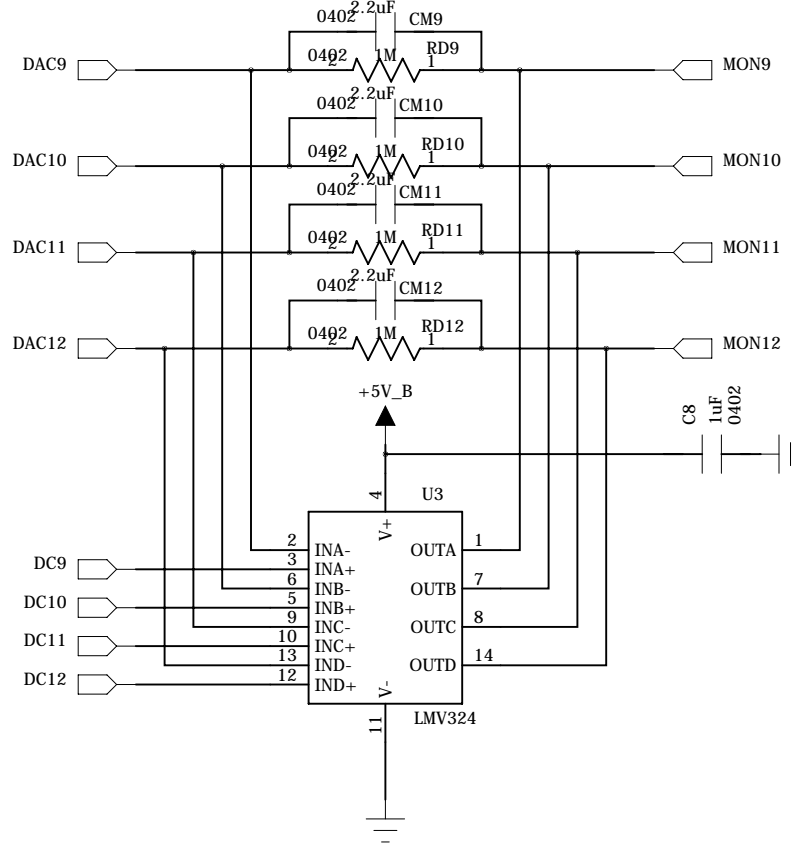
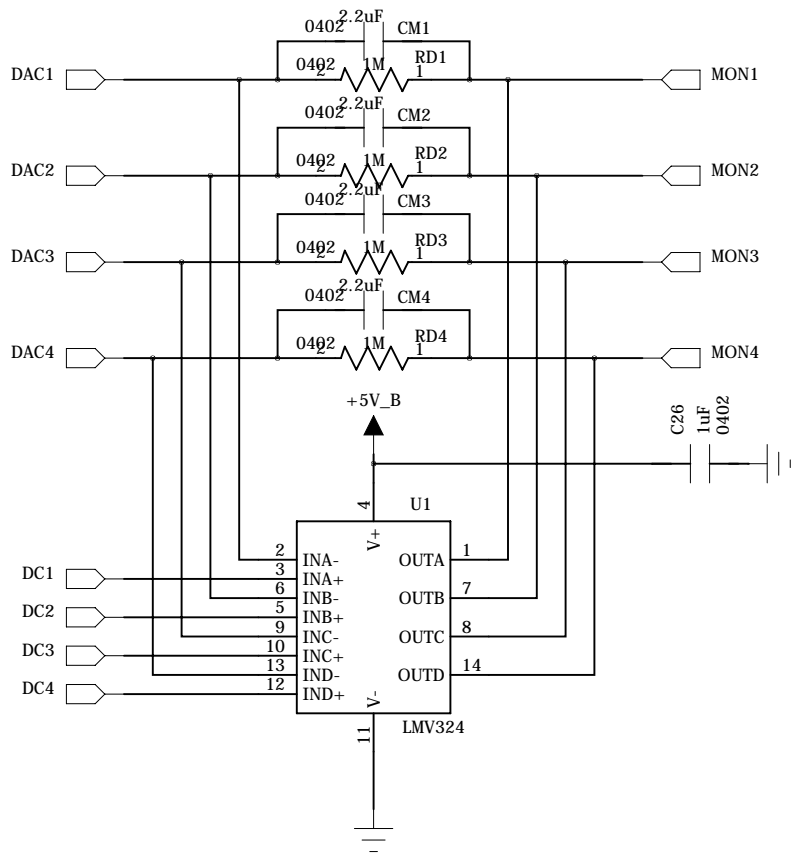
C

B

B

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A



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sheet #:	4 of 6
sheet description:	
date last modified:	4-30-2013

6

5

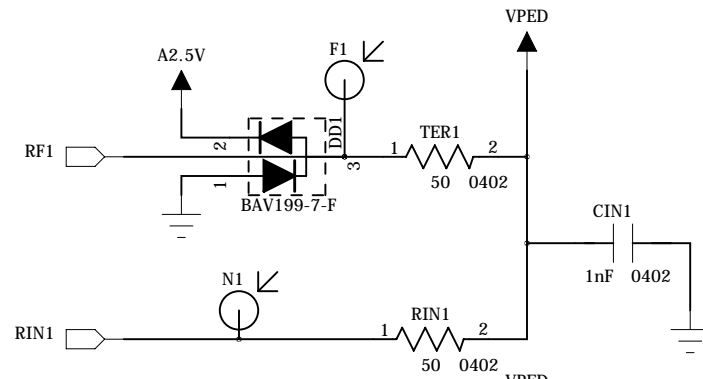
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3

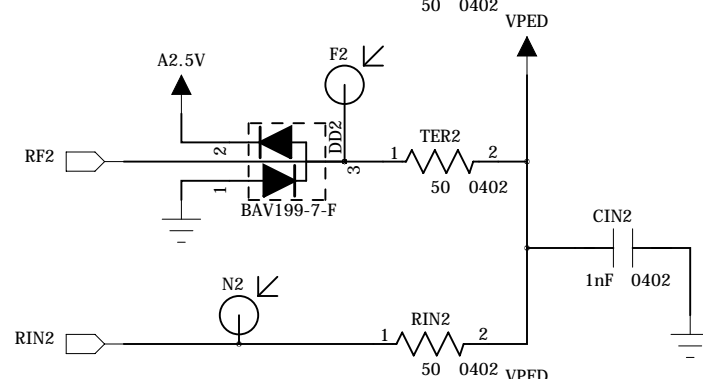
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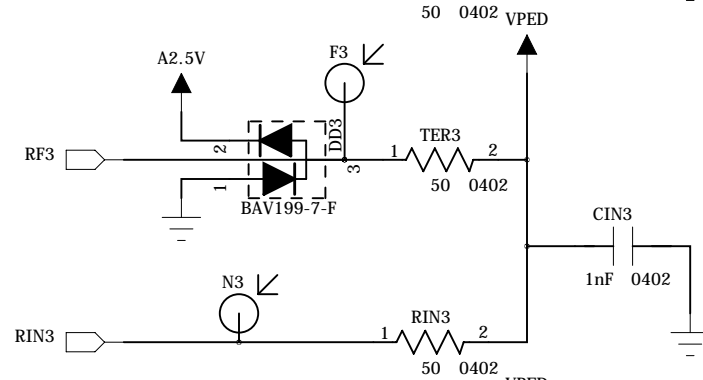
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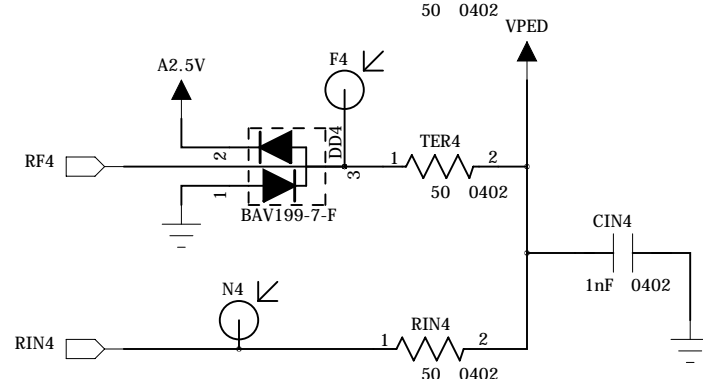
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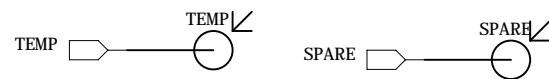
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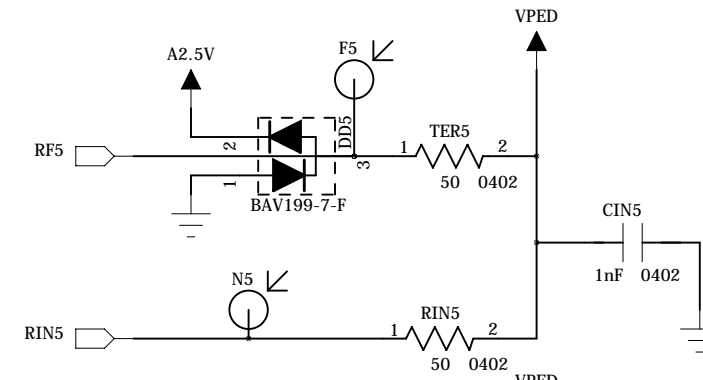
B



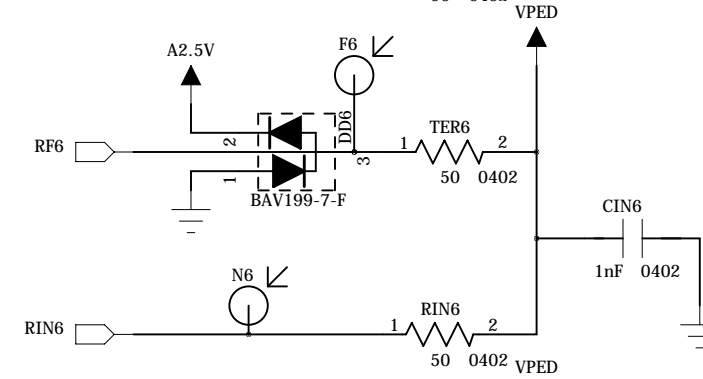
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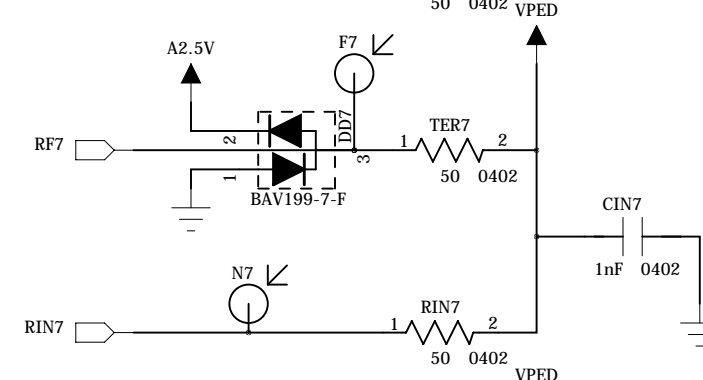
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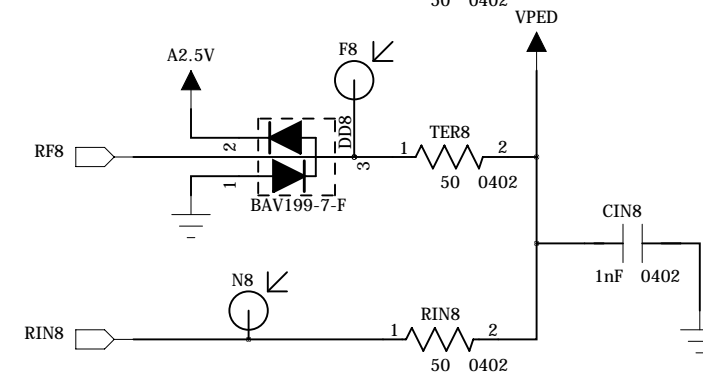
D



C



B



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IDLAB design #: IDL\_13\_019  
circuit design: XS  
PCB design: XS

sheet #: 5 of 6  
sheet description:  
date last modified: 4-30-2013

A

6

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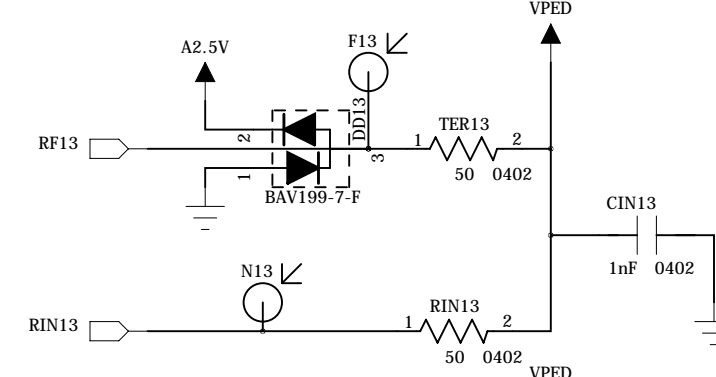
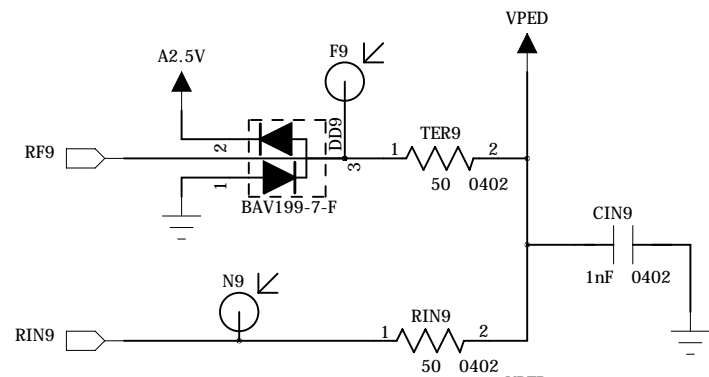
3

2

1

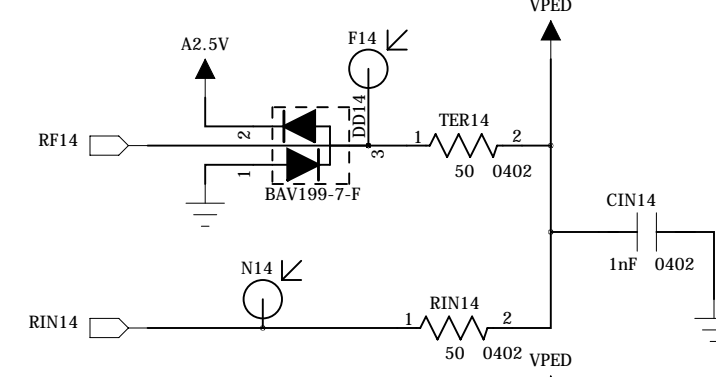
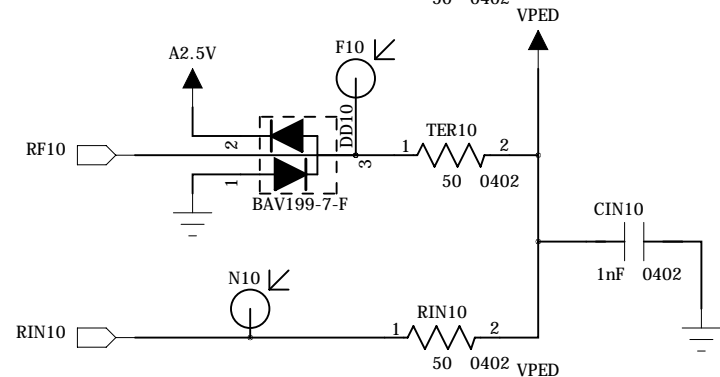
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E



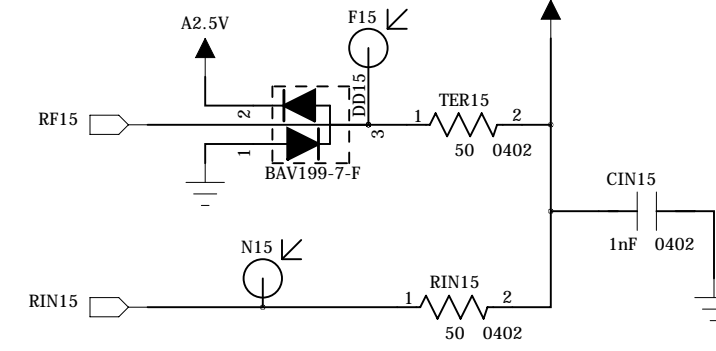
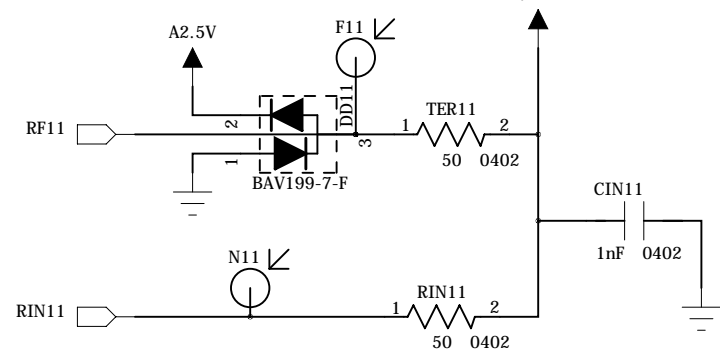
D

D



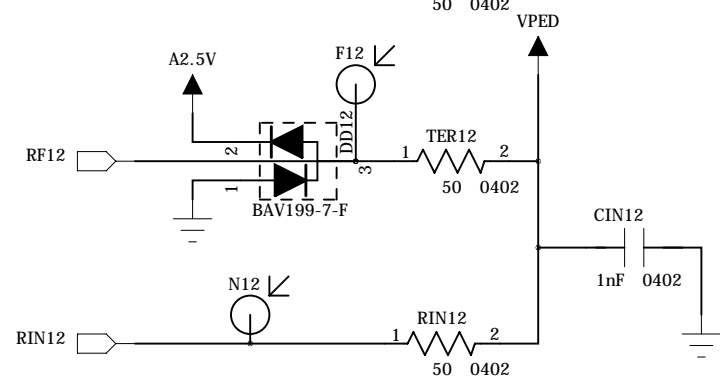
C

C



B

B



A

A

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