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High Energy Physics Group
Instrumentation Development Laboratory
2505 Correa Road, Honolulu, HI 96822

Production Documentation for:

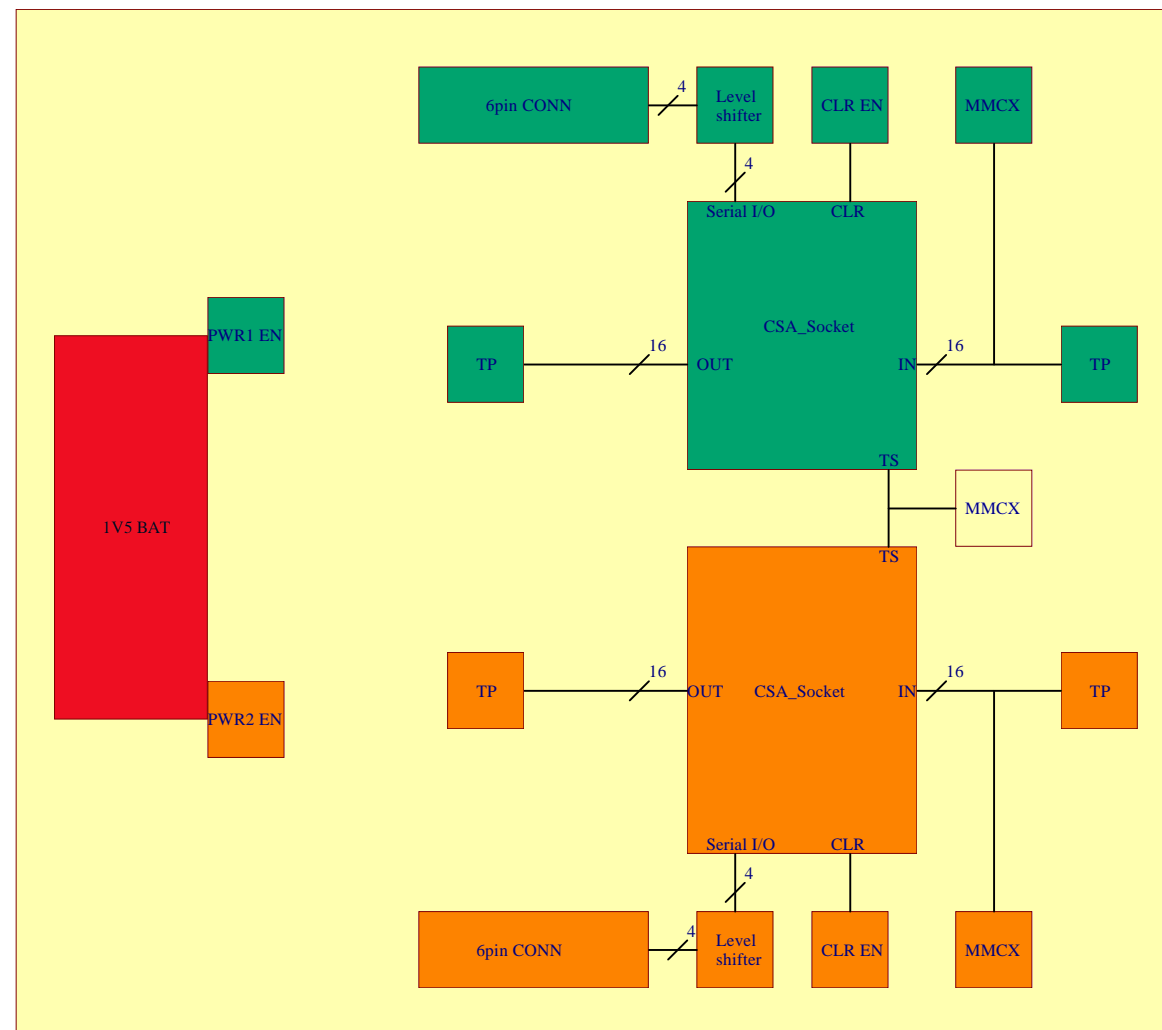
Project Name: CSA_V3
Board Name: CSA_V3_Radiation_Board
IDL num: IDL_16_016
Revision: A
Variant: [No Variations]

Designer: AS/KPL
Drawn by: KPL
Approved by: Gary S. Varner

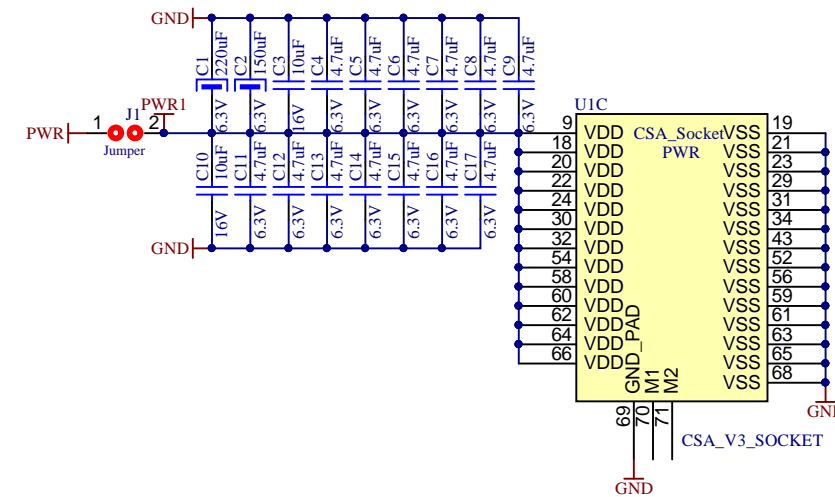
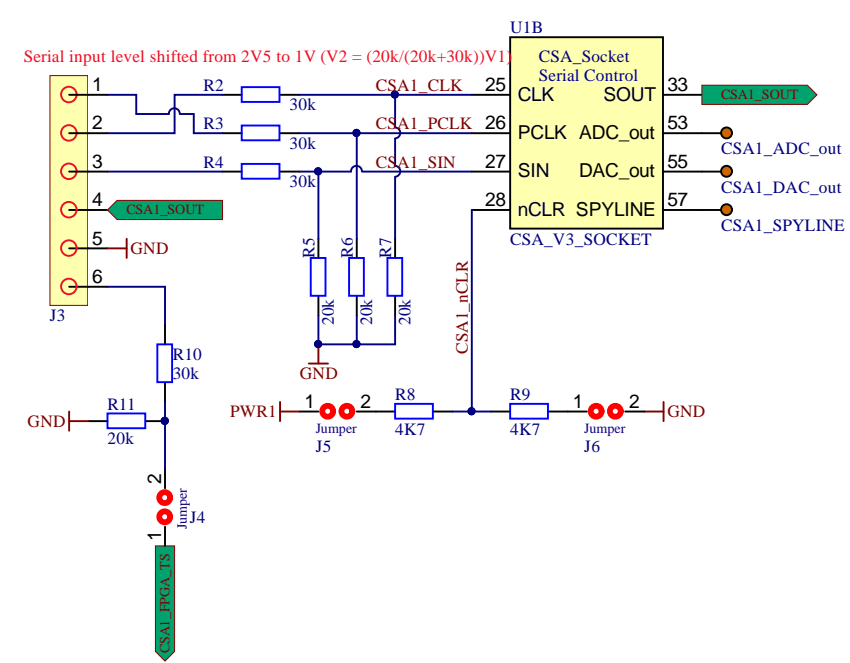
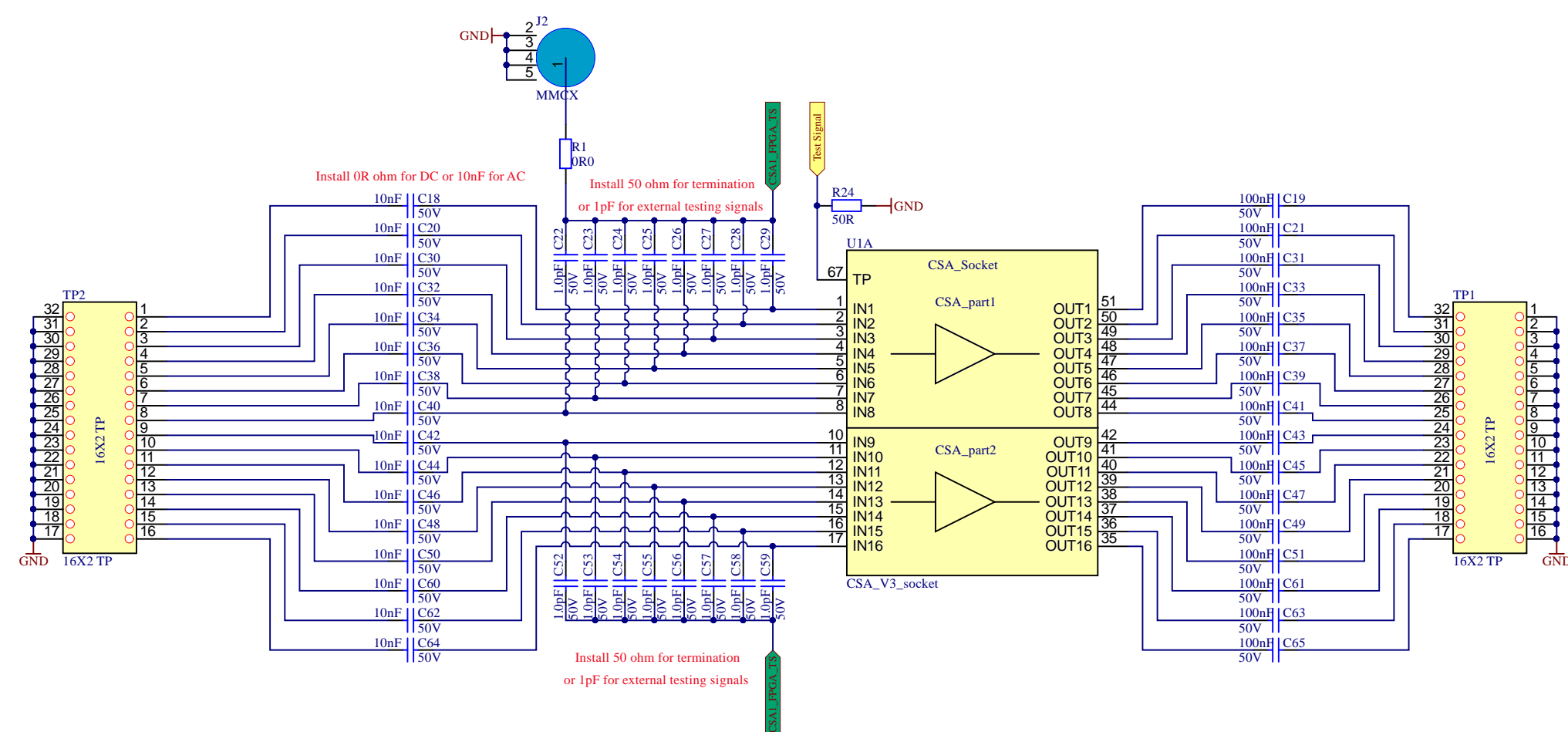
High Energy Physics Group, Instrumentation Development Lab		Designer: AS/KPL	IDLAB design #: IDL_16_016
Project name: CSA_V3		Drawn By: KPL	Revision: A
		Approved By: Gary S. Varner	Variant: [No Variations]
Board name: CSA_V3_Radiation_Board		Modif. Date: 10/24/2016	
		Sheet 1 of 4	



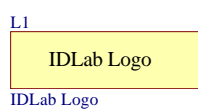
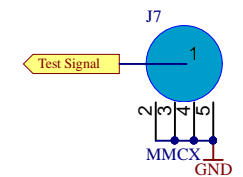
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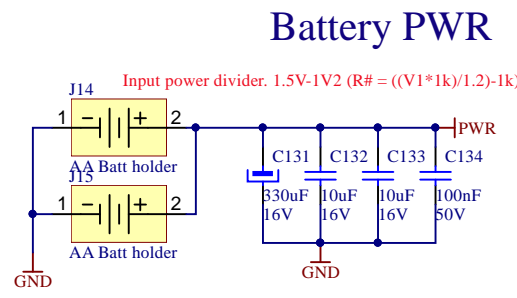
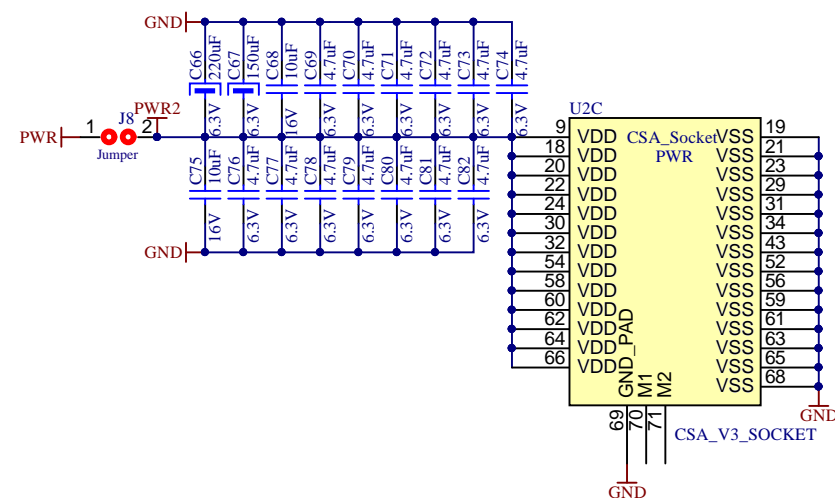
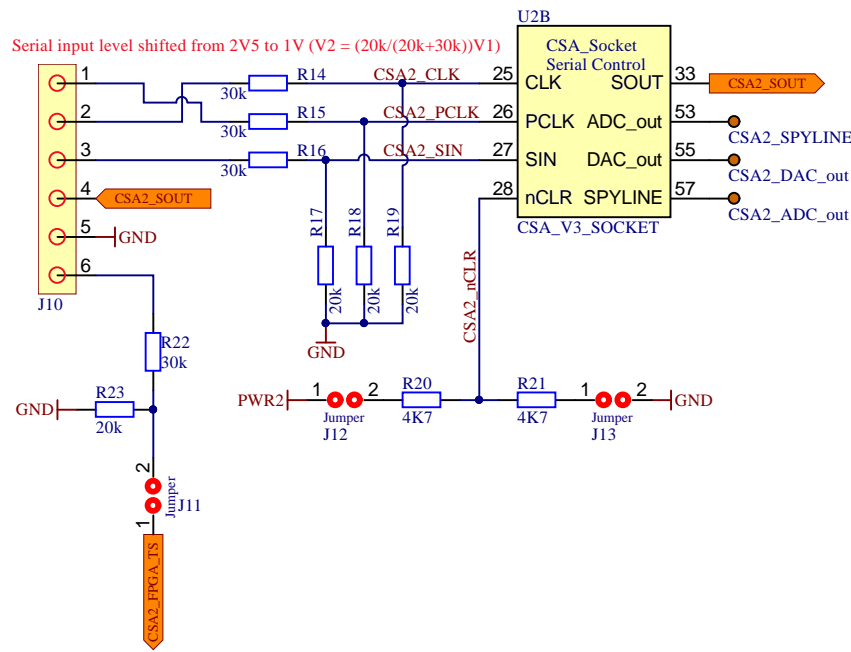
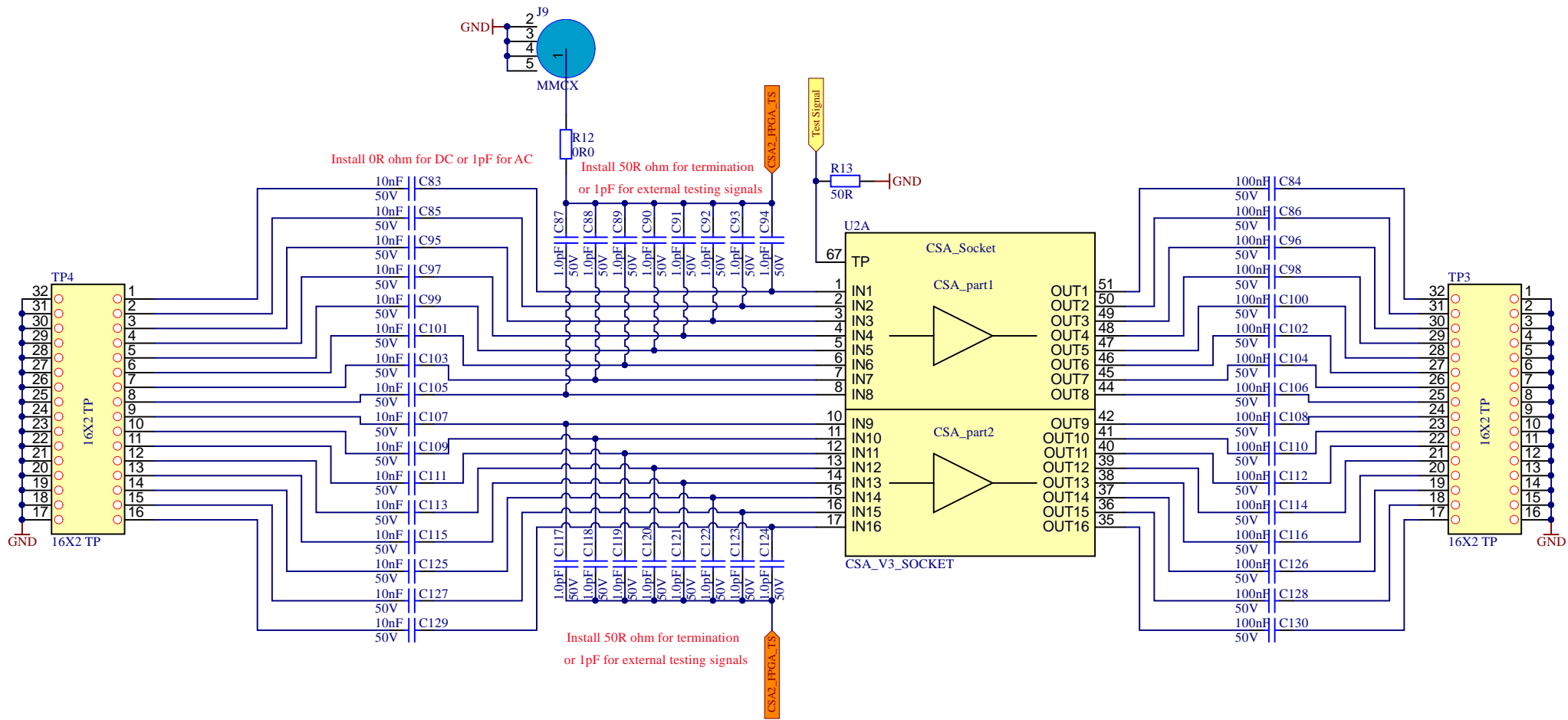
CSAv3 Socket1

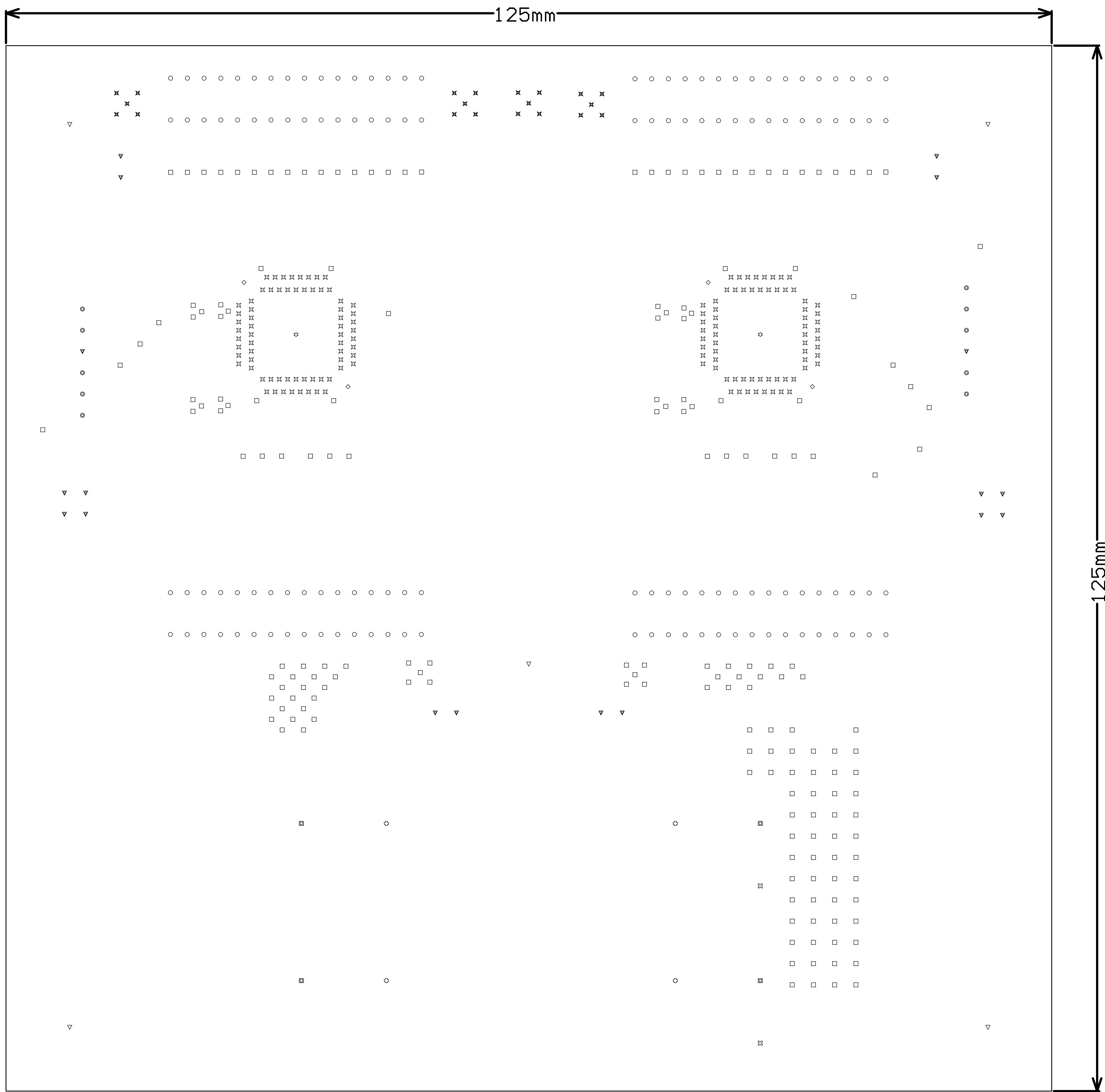


Test Signal Input



CSAv3 Socket2





Notes:

- Board shall be fabricated - performace class II as per IPC-6011 and IPC6012
- Silkscreen printed on both sides
- Material: high temperature FR4 class epoxy glass rated UL94V-0. UL symbol and rating shall be marked farside
35um copper for external layers and 18um for all internal layers
Must be RoHS compliant and survive a lead-free assembly max reflow of 260 deg C (5 passes)
Td rating: >340 deg C
Tg = 150 deg C (min)
- Solder mask: SMOBC per IPC-SM-840C, class T must be Rohs compliant, 0.001" max measured over bare copper plating, must clear all lands as indicated on gerber solder mask layers, color= GREEN
- Finish: electro-less nickel immersion gold (ENIG), 0.05-0.125um Au over 3-6um Ni - over bare copper only
- Solderability test: Category 2 of J-STD-003
- Finished boards shall not have nicks, scratches, voids, exposed copper, poor plating or misdrilled holes
- All holes sizes are after plating
- PCB manufacturer may add copper thieving as needed to improve manufacturability, thieving to be 0.030" round pads at 0.050" spacing.
Thieving will have a minimum of 0.100" clearance from existing copper and should not be placed under surface mounted devices
- PCB manufacturer may use tear drops to improve annular rings as long as DRC rules are followed
- All via connections to power and ground planes are solid
- All unconnected pads on inner signal layers are removed
- All finished boards are to be 100% electrically tested
- Unless otherwise indicated, all linear toleracnes shall be XX.X +/-0.2mm and XX.XX +/- 0.1mm
- Gerber file GM1 shows board outline (milling line)
- Table 1 shows Layer stack details

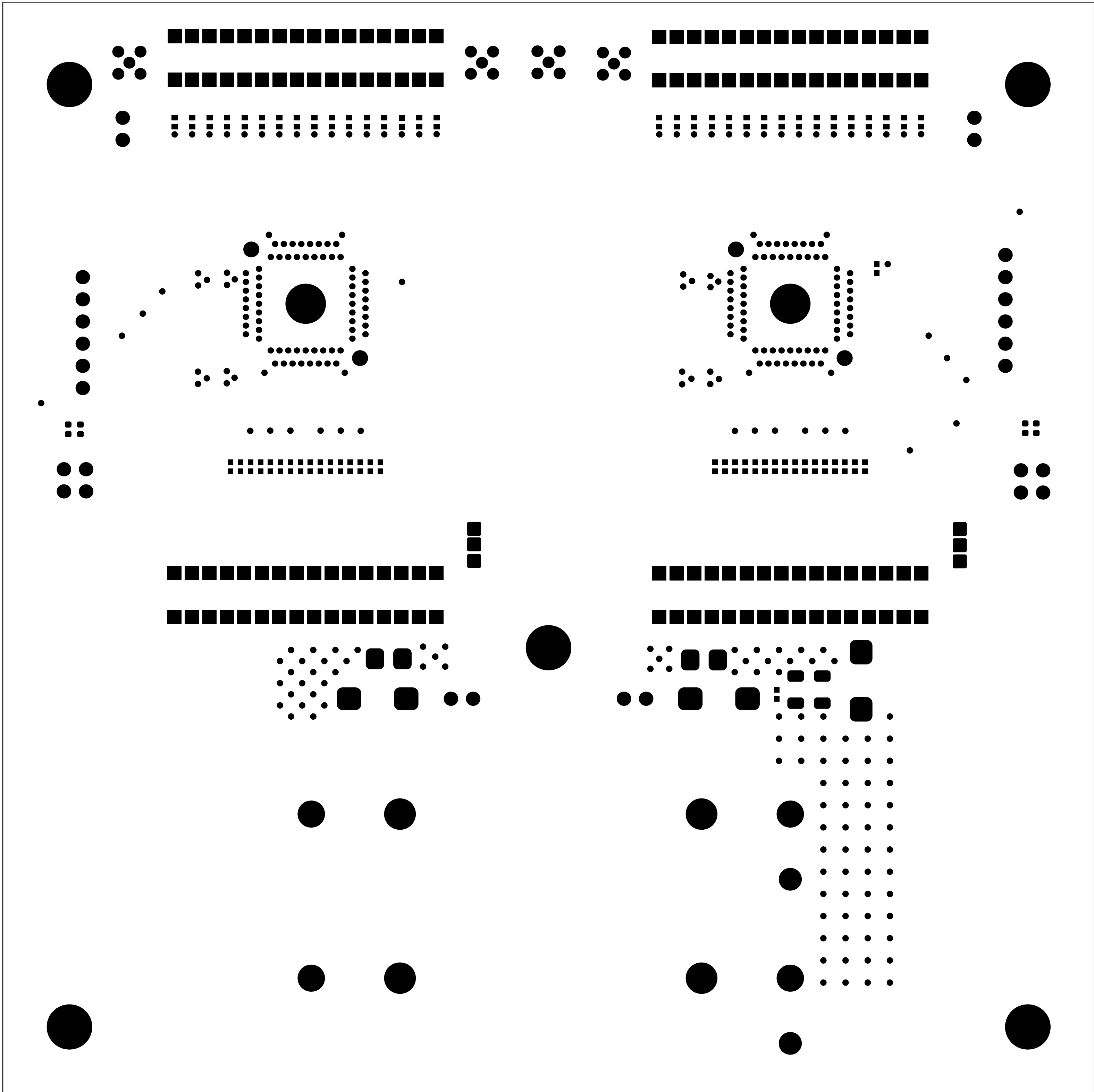
Table 1a: Layer Stack Details for IDL_16_016 (Imperial Units)

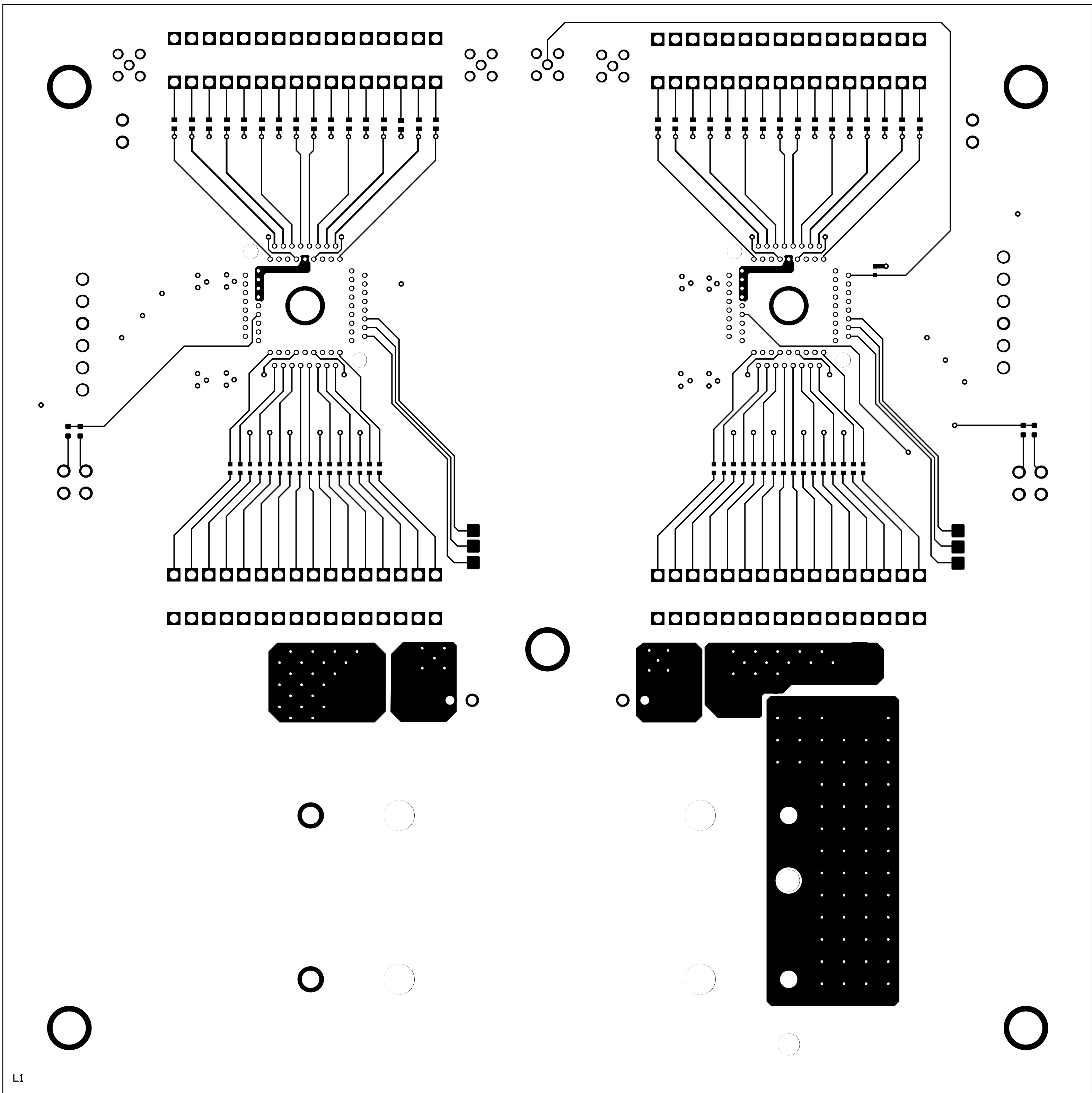
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer - SIG1	Copper	1.38mil		
4	Dielectric 1	FR-4	8.00mil	4.65	
5	MID1_GND	Copper	0.71mil		
6	Dielectric 2	FR-4	40.00mil	4.65	
7	MID2_PWR	Copper	0.71mil		
8	Dielectric 4	FR-4	8.00mil	4.2	
9	Bottom Layer - SIG2	Copper	1.38mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

Table 2: NC Drill Details for IDL_16_016

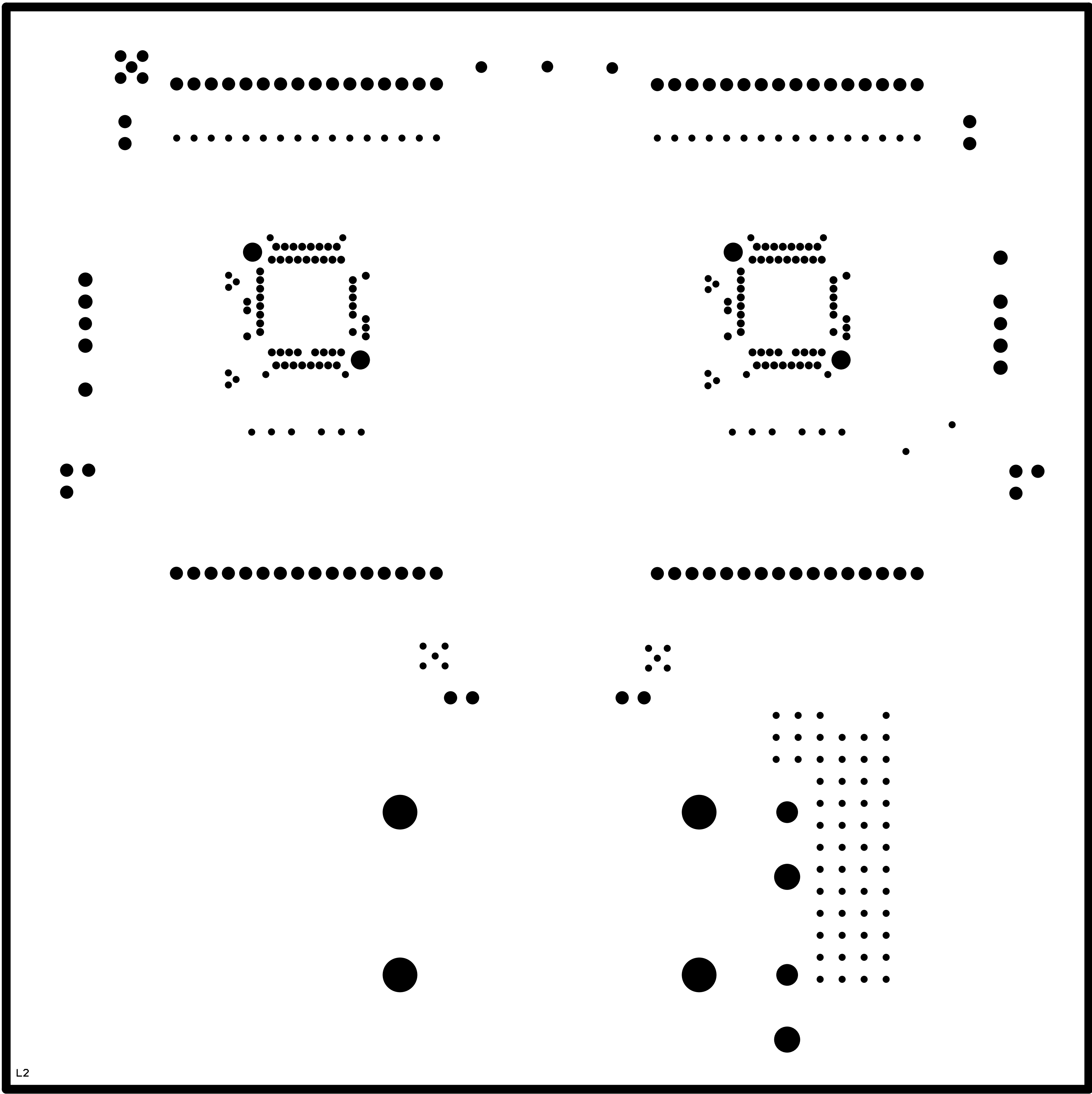
Symbol	Count	Hole Size	Plated	Hole Type
□	188	12.00mil <0.305mm	PTH	Round
⌘	136	15.75mil <0.400mm	PTH	Round
⌘	20	33.07mil <0.840mm	PTH	Round
○	128	39.37mil <1.000mm	PTH	Round
▼	18	40.00mil <1.016mm	PTH	Round
⊙	10	45.00mil <1.143mm	PTH	Round
◇	4	66.93mil <1.700mm	NPTH	Round
▣	4	78.74mil <2.000mm	PTH	Round
⌘	2	98.43mil <2.500mm	NPTH	Round
⊕	4	137.80mil <3.500mm	NPTH	Round
☆	2	137.80mil <3.500mm	PTH	Round
▽	5	150.00mil <3.810mm	PTH	Round
	521 Total			

Designer: AS/KPL	Revision: .Version	File: IDL_16_016.PcbDoc	Sheet 1 of 1	Code: IDL_16_016
Drawn By: KPL	Modif. Date: Date	Variant: [No Variations]	PCB	
Approved By: Gary S. Varner	Print Date: 1/9/2017	Signature:	Size: A3 H	ID: CSA_V3_Radiation_Boa
Title: Drill Drawing and Dimensions GD1				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory

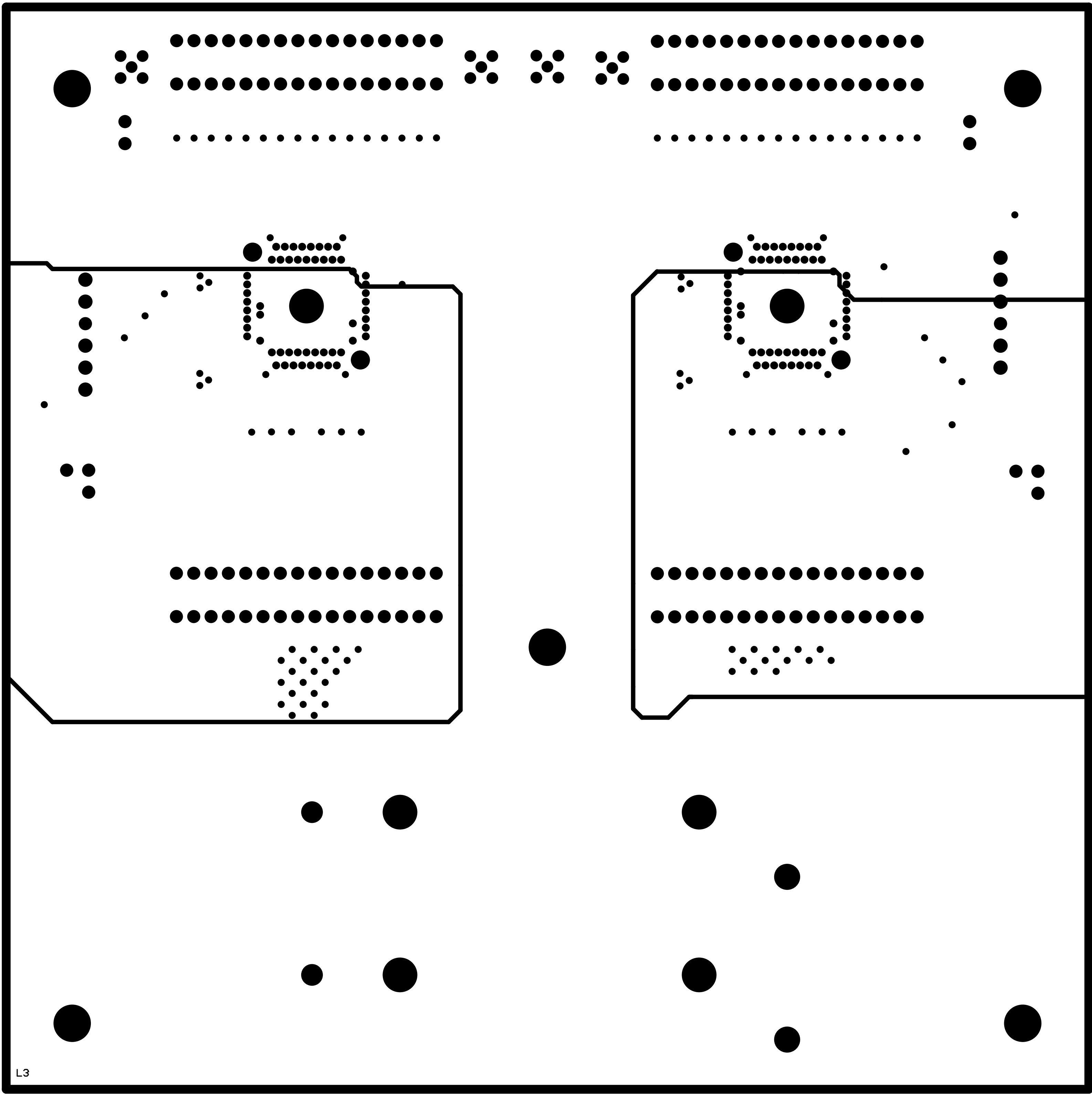




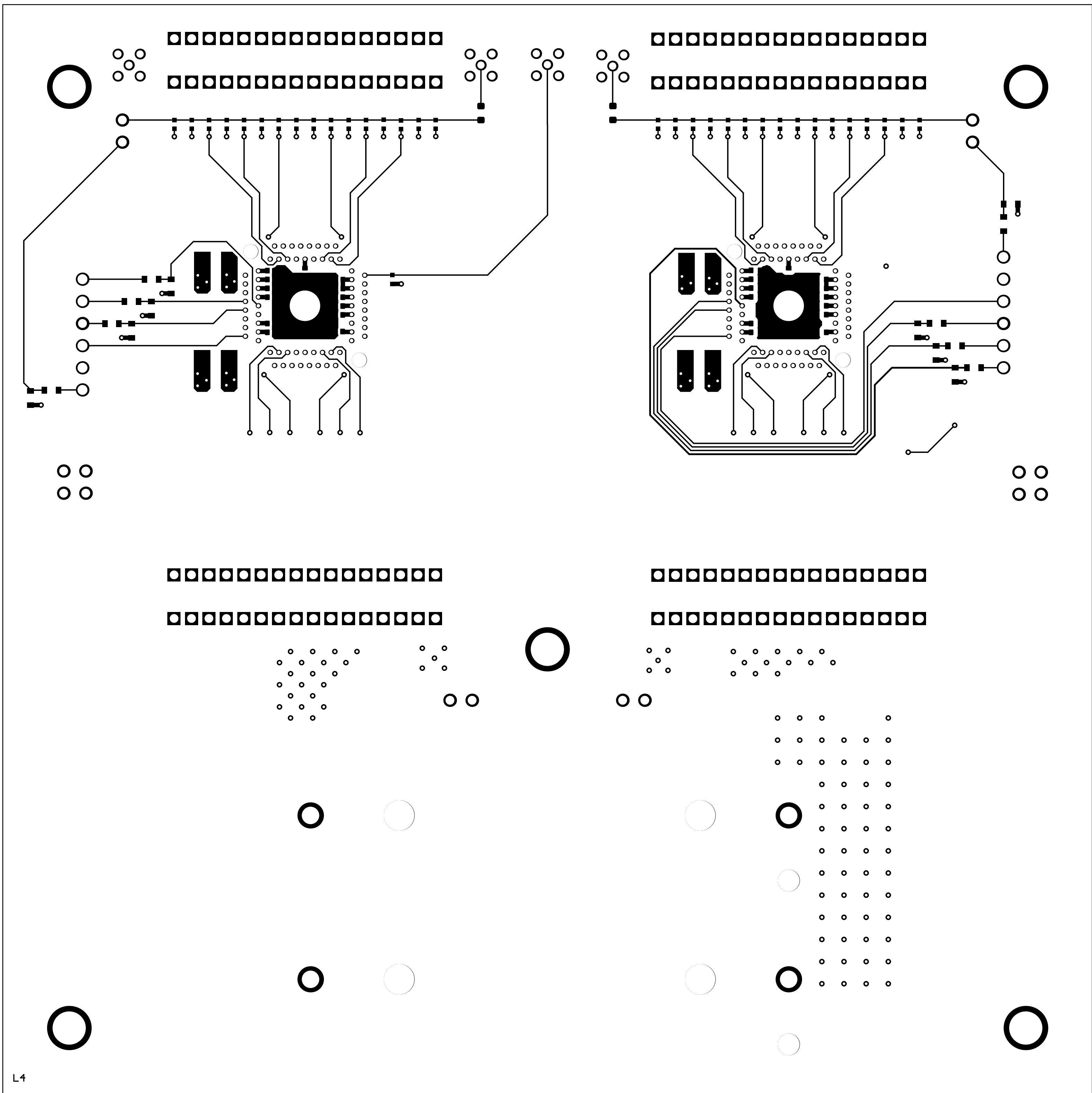
Designer: AS/KPL	Revision: .Version	File: IDL_16_016.PcbDoc	Sheet 1 of 1	Code: IDL_16_016
Drawn By: KPL	Modif. Date: Date	Variant: [No Variations]	PCB	
Approved By: Gary S. Varner	Print Date: 1/9/2017	Signature:	Size: A3 H	ID: CSA_V3_Radiation_Boa
Title: Top Layer 1 GTL				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory



Designer: AS/KPL	Revision: .Version	File: IDL_16_016.PcbDoc	Sheet 1 of 1	Code: IDL_16_016
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Approved By: Gary S. Varner	Print Date: 1/9/2017	Signature:	Size: A3 H	ID: CSA_V3_Radiation_Boa
Title: GND Plane Layer 2 GP1				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory

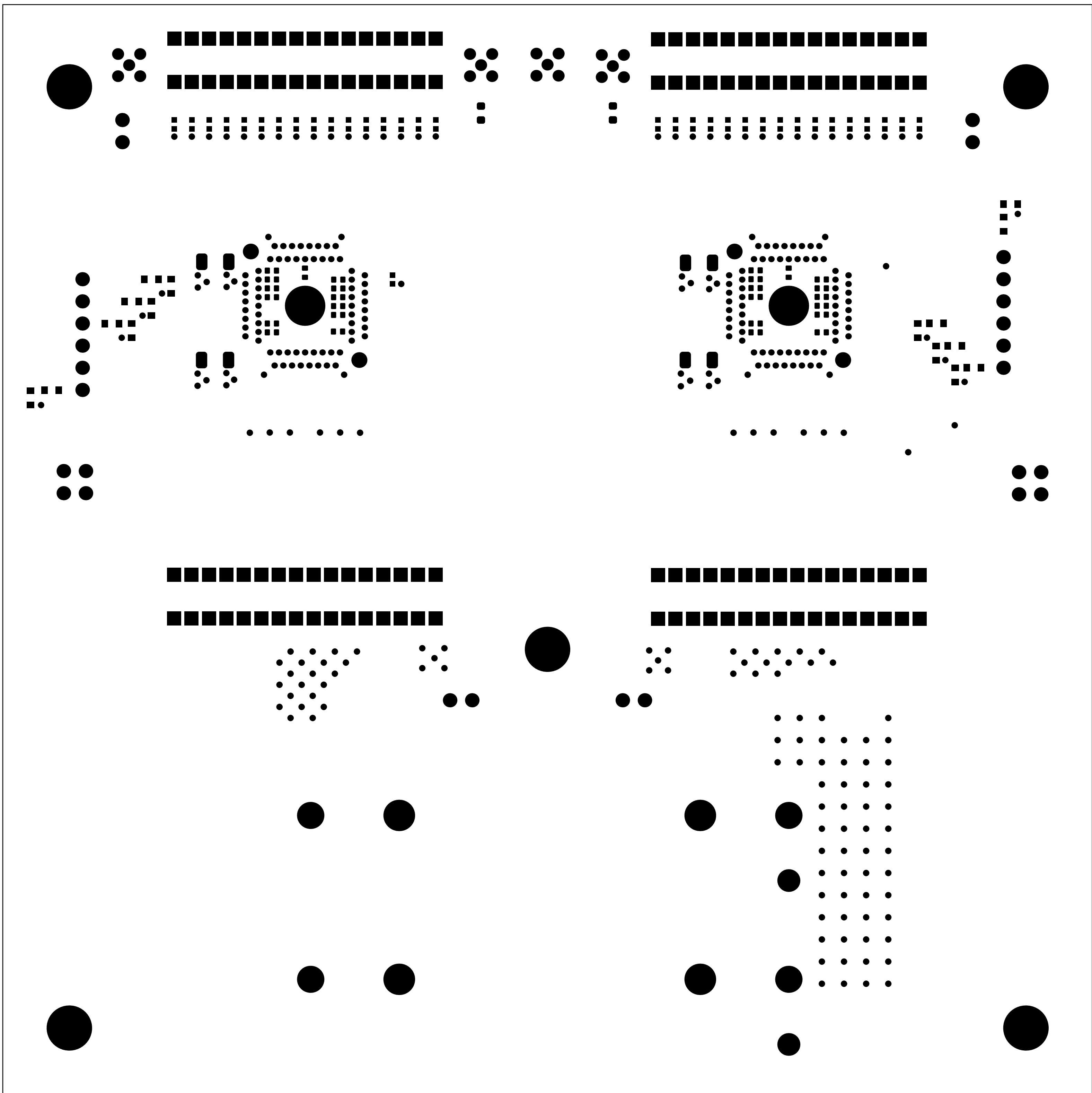


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Drawn By: KPL	Modif. Date: Date	Variant: [No Variations]	PCB	
Approved By: Gary S. Varner	Print Date: 1/9/2017	Signature:	Size: A3 H	ID: CSA_V3_Radiation_Boa
Title: PWR Plane Layer 3 GP2				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory



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Designer: AS/KPL	Revision: .Version	File: IDL_16_016.PcbDoc	Sheet 1 of 1	Code: IDL_16_016
Drawn By: KPL	Modif. Date: Date	Variant: [No Variations]	PCB	
Approved By: Gary S. Varner	Print Date: 1/9/2017	Signature:	Size: A3 H	ID: CSA_V3_Radiation_Boa
Title: Bottom Layer 4 GBL				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory



Designer: AS/KPL	Revision: .Version	File: IDL_16_016.PcbDoc	Sheet 1 of 1	Code: IDL_16_016
Drawn By: KPL	Modif. Date: Date	Variant: [No Variations]	PCB	
Approved By: Gary S. Varner	Print Date: 1/9/2017	Signature:	Size: A3 H	ID: CSA_V3_Radiation_Boa
Title: Bottom Solder Mask GBS				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory

