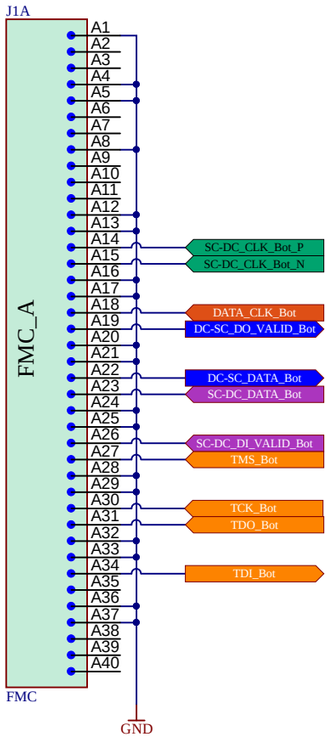
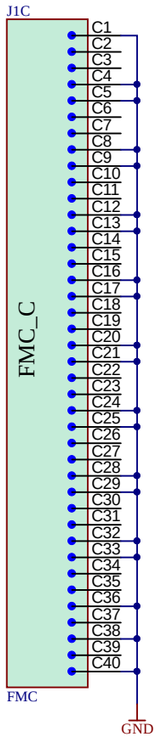
High Energy Physics Group
Instrumentation Development Laboratory
2505 Correa Road, Honolulu, HI 96822

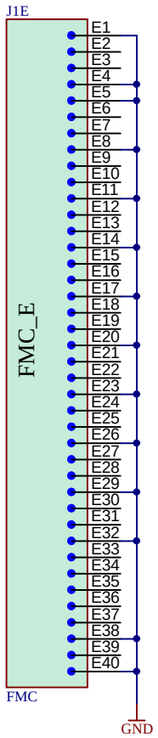
Production Documentation for:

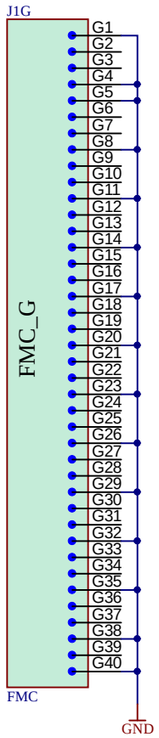
Project Name:	***BMD***
Board Name:	***SCROD_TO_FMC_BOARD***
IDL num:	***IDL_17_009***
Revision:	***A***
Variant:	***[No Variations]***
Designer:	***Khanh Le***
Drawn by:	***Khanh Le***
Approved by:	***Gary S. Varner***

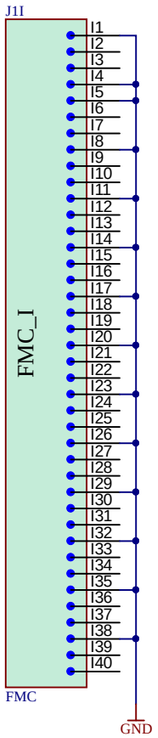
High Energy Physics Group, Instrumentation Development Lab		Designer:	Khanh Le	IDLAB design #:	IDL_17_009
Project name:	**BMD**	Drawn By:	Khanh Le	Revision:	A
		Approved By:	Gary S. Varner	Variant:	[No Variations]
Board name:	**SCROD_TO_FMC_BOARD**			Modif. Date:	5/8/2017
				Sheet	1 of 3

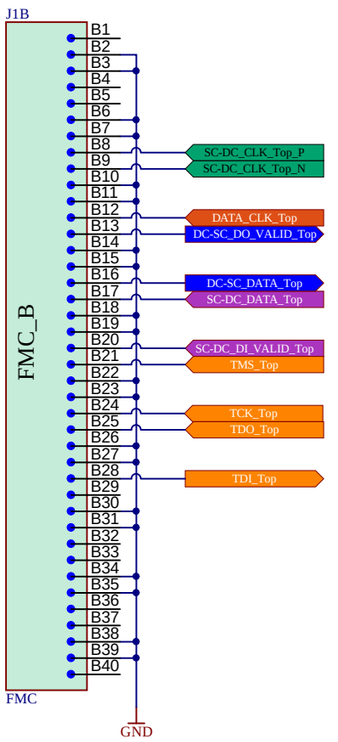


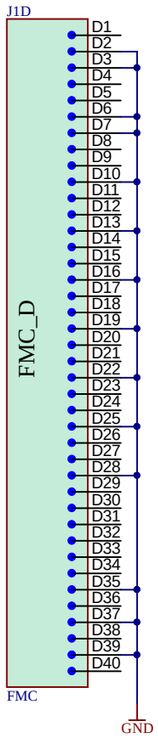


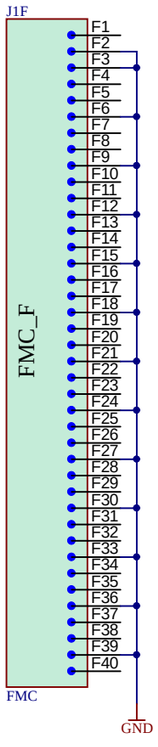


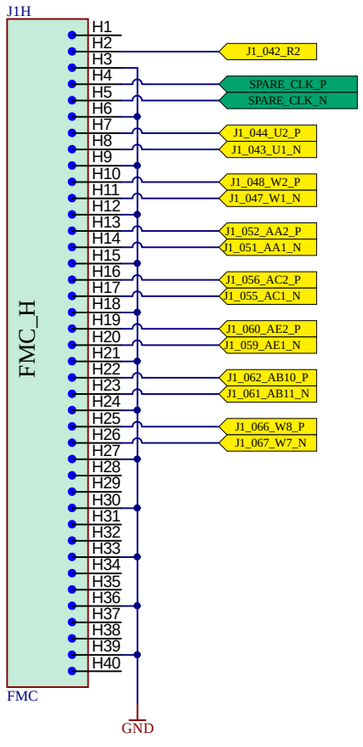


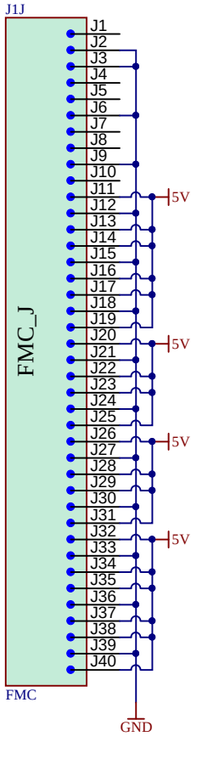




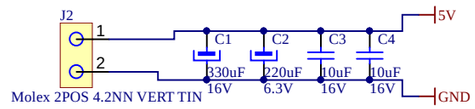


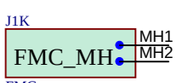






Note: To power SCROD from the FMC_CONN_BOARD
-Solder RAW1,RAW2, RAW1_GND, RAW2_GND
test points together and input 5V to power SCROD



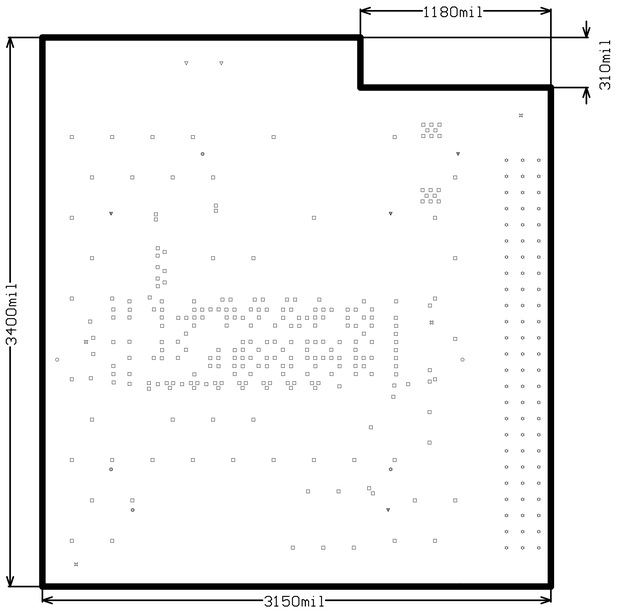


High Energy Physics Group, Instrumentation Development Lab	Designer: Khanh Le	IDLAB design #:	IDL_17_009
Board: SCROD_TO_FMC_BOARD	Drawn By: Khanh Le	Revision:	A
	Approved By: Gary S. Varner	Variant:	[No Variations]
Sheet Title: FMC_CONN		Modif. Date:	5/9/2017
		Sheet 2 of 3	

UNIVERSITY of HAWAI'I® MĀNOA

High Energy Physics Group, Instrumentation Development Lab	Designer: Khanh Le	IDLAB design #:	IDL_17_009
Board: SCROD_TO_FMC_BOARD	Drawn By: Khanh Le	Revision:	A
	Approved By: Gary S. Varner	Variant:	[No Variations]
Sheet Title: SCROD_CONN		Modif. Date:	5/9/2017
		Sheet	3 of 3

UNIVERSITY of HAWAI'I® MĀNOA



Notes:

1. Board shall be fabricated - performace class II as per IPC-6011 and IPC6012
2. PCB manufacturer logo, P/N, revision and/or date code of manufacturing
   shall be printed in top solder mask (not over pcb traces, allowed over copper plane).
   The date code shall be in the format: "WWYY" where WW=week and YY= year, max height 0.15 inches
3. Silkscreen printed on both sides
4. Material: high temperature FR4 class epoxy glass rated UL94V-0. UL symbol and rating shall be marked farside
   35um copper for external layers and 18um for all internal layers
   Must be RoHS compliant and survive a lead-free assembly max reflow of 260 deg C (5 passes)
   Td rating: >340 deg C
   Tg = 150 deg C (min)
5. Solder mask: SMOBC per IPC-SM-840C, class T must be Rohs compliant, 0.001" max measured over bare copper plating,
   must clear all lands as indicated on gerber solder mask layers, color= GREEN
6. Finish: electro-less nickel immersion gold (ENIG), 0.05-0.125um Au over 3-6um Ni - over bare copper only
7. Solderability test: Category 2 of J-STD-003
8. Finished boards shall not have nicks, scratches, voids, exposed copper, poor plating or misdrilled holes
9. All holes sizes are after plating
10. PCB manufacturer may add copper thieving as needed to improve manufacturability,
    thieving to be 0.030" round pads at 0.050" spacing.
    Thieving will have a minimum of 0.100" clearance from existing copper and should not be placed under surface mounted devices
11. PCB manufacturer may use tear drops to improve annular rings as long as DRC rules are followed
12. All via connections to power and ground planes are solid
13. All unconnected pads on inner signal layers are removed
14. All finished boards are to be 100% electrically tested
15. Unless otherwise indicated, all linear toleracnes shall be XX.X +/-0.2mm and XX.XX +/- 0.1mm
16. Gerber file GM1 shows board outline (milling line)
17. Table 1 shows Layer stack details

Table 1a: Layer Stack Details in mils for IDL_17_009 Rev.A

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack
1	Top Overlay					
2	Top Solder	Solder Resist	0.40mil	3.5		
3	Top Layer	Copper	1.38mil			
4	Dielectric 1	FR-4	9.00mil	4.65		
5	MID GND	Copper	1.42mil			
6	Dielectric 2	FR-4	37.61mil	4.65		
7	MID PWR	Copper	1.42mil			
8	Dielectric 3	FR-4	9.00mil	4.65		
9	Bottom Layer	Copper	1.38mil			
10	Bottom Solder	Solder Resist	0.40mil	3.5		
11	Bottom Overlay					

Table 1b: Layer Stack Details in mm for IDL_17_009 Rev.A

Layer	Name	Material	Thickness	Constant	Board Layer Stack	Board Layer Stack
1	Top Overlay					
2	Top Solder	Solder Resist	0.010mm	3.5		
3	Top Layer	Copper	0.035mm			
4	Dielectric 1	FR-4	0.229mm	4.65		
5	MID GND	Copper	0.036mm			
6	Dielectric 2	FR-4	0.955mm	4.65		
7	MID PWR	Copper	0.036mm			
8	Dielectric 3	FR-4	0.229mm	4.65		
9	Bottom Layer	Copper	0.035mm			
10	Bottom Solder	Solder Resist	0.010mm	3.5		
11	Bottom Overlay					

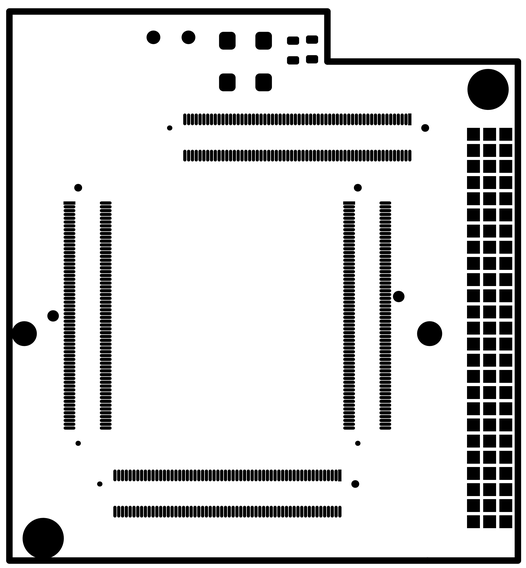
Table 2: Drill Details for IDL_17_002 Rev.A

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape
⊠	2	50.00mil (1.270mm)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded
▽	2	60.00mil (1.524mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded
○	2	100.00mil (2.540mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded
⊠	2	150.00mil (3.810mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded
◎	4	27.56mil (0.700mm)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded
▽	4	43.31mil (1.100mm)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded
☼	75	50.00mil (1.270mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rectangle
□	264	12.00mil (0.305mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded
	355 Total						

Designer: Khanh Le	Revision: .Version	File: IDL_17_009.PcbDoc	Sheet 1 of 1	Code: **IDL_17_009**
Drawn By: Khanh Le	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **SCROD_TO_FMC_BOARD**
Approved By: Gary S. Varner	Print Date: 5/9/2017	Signature:	Size: A3 H	

Title: Drill Drawing and Dimensions GD1

University of Hawaii at Manoa
High Energy Physics Group
Instrumentation Development Laboratory

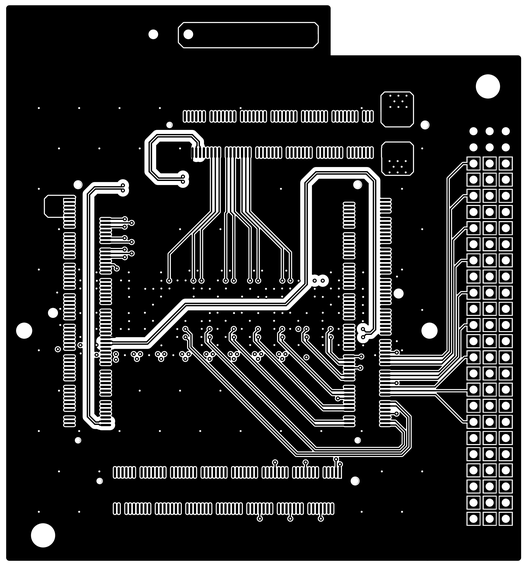


Designer: Khanh Le	Revision: .Version	File: IDL_17_009.PcbDoc	Sheet 1 of 1
Drawn By: Khanh Le	Modif. Date: Date	Variant: [No Variations]	PCB
Approved By: Gary S. Varner	Print Date: 5/9/2017	Signature:	Size: A3 H

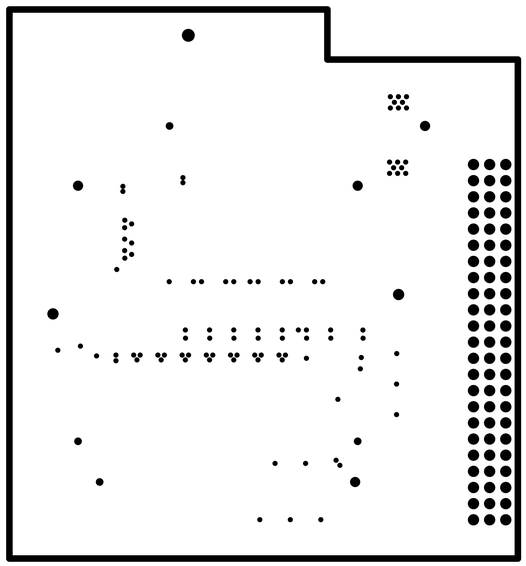
Title:
Top Solder Mask GTS

Code: **IDL_17_009**
ID: **SCROD_TO_FMC_BOARD**

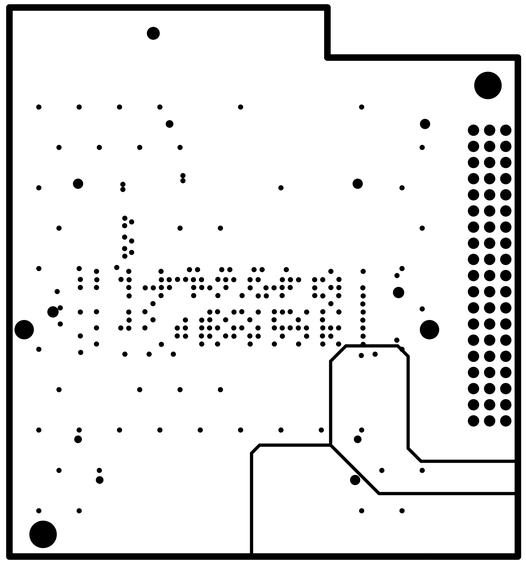
University of Hawaii at Manoa
High Energy Physics Group
Instrumentation Development Laboratory



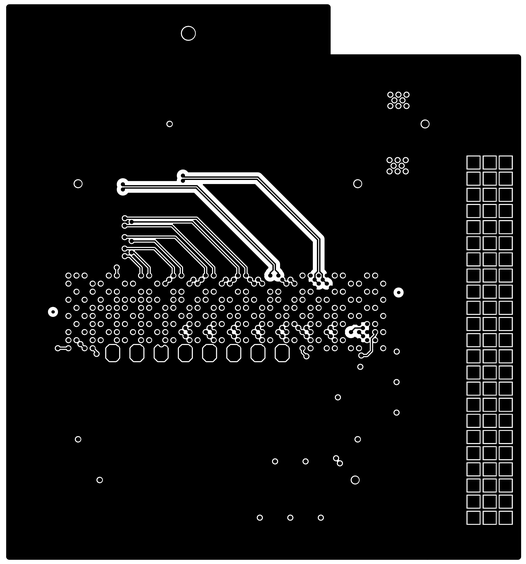
Designer: Khanh Le	Revision: .Version	File: IDL_17_009.PcbDoc	Sheet 1 of 1	Code: **IDL_17_009**
Drawn By: Khanh Le	Modif. Date: Date	Variant: [No Variations]	PCB	
Approved By: Gary S. Varner	Print Date: 5/9/2017	Signature:	Size: A3 H	ID: **SCROD_TO_FMC_BOARD**
Title: Top Layer 1 GTL				**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**



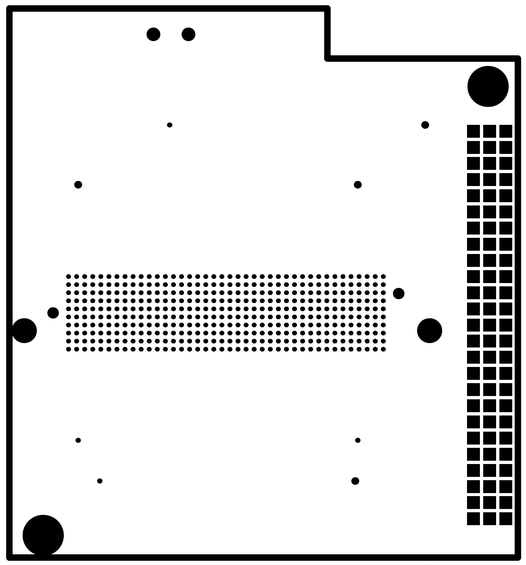
Designer: Khanh Le	Revision: .Version	File: IDL_17_009.PcbDoc	Sheet 1 of 1	Code: **IDL_17_009**
Drawn By: Khanh Le	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **SCROD_TO_FMC_BOARD**
Approved By: Gary S. Varner	Print Date: 5/9/2017	Signature:	Size: A3 H	
Title: GND Plane Layer 2 GP1				**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**



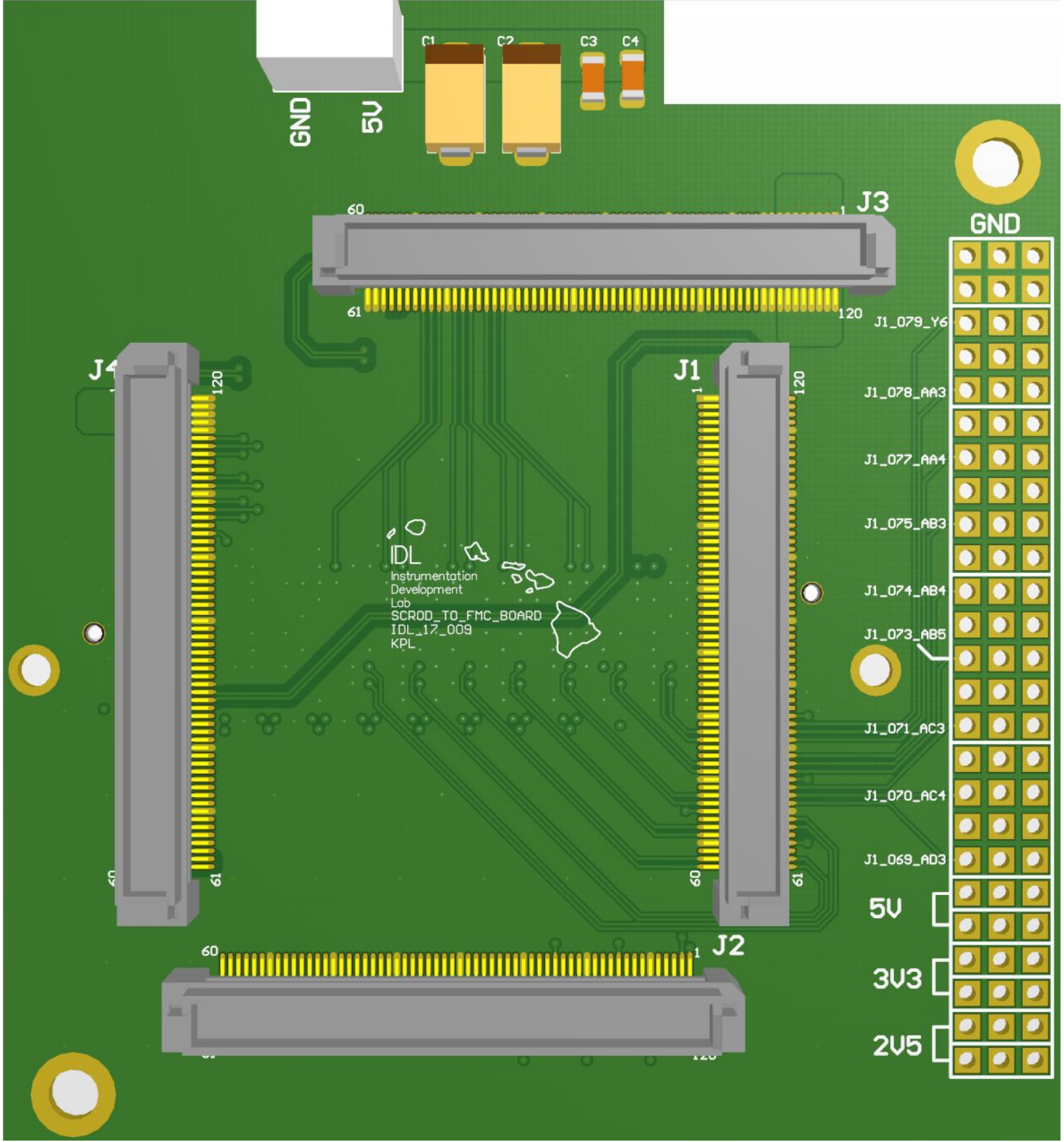
Designer: Khanh Le	Revision: .Version	File: IDL_17_009.PcbDoc	Sheet 1 of 1	Code: **IDL_17_009**
Drawn By: Khanh Le	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **SCROD_TO_FMC_BOARD**
Approved By: Gary S. Varner	Print Date: 5/9/2017	Signature:	Size: A3 H	
Title: PWR Plane Layer 3 GP2				**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**

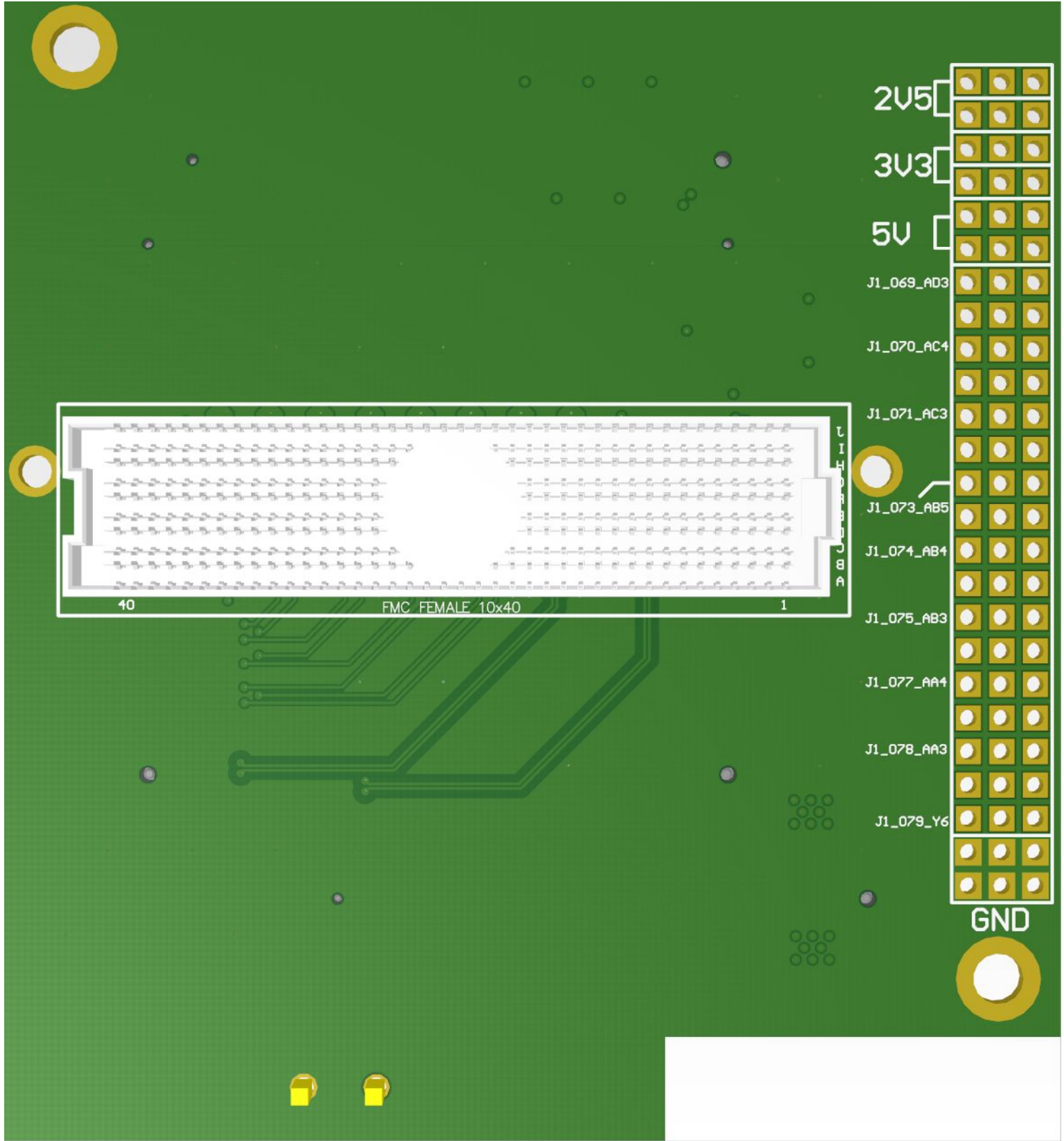


Designer: Khanh Le	Revision: .Version	File: IDL_17_009.PcbDoc	Sheet 1 of 1	Code: **IDL_17_009**
Drawn By: Khanh Le	Modif. Date: Date	Variant: [No Variations]	PCB	
Approved By: Gary S. Varner	Print Date: 5/9/2017	Signature:	Size: A3 H	ID: **SCROD_TO_FMC_BOARD**
Title: Bottom Layer 4 GBL				**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**



Designer: Khanh Le	Revision: .Version	File: IDL_17_009.PcbDoc	Sheet 1 of 1	Code: **IDL_17_009**
Drawn By: Khanh Le	Modif. Date: Date	Variant: [No Variations]	PCB	ID: **SCROD_TO_FMC_BOARD**
Approved By: Gary S. Varner	Print Date: 5/9/2017	Signature:	Size: A3 H	**University of Hawaii at Manoa** **High Energy Physics Group** **Instrumentation Development Laboratory**
Title: Bottom Solder Mask GBS				


GND
5V
C1
C2
C3
C4
J3
60
1
61
120
GND
J1_079_Y6
J1_078_AA3
J1_077_AA4
J1_075_AB3
J1_074_AB4
J1_073_AB5
J1_071_AC3
J1_070_AC4
J1_069_AD3
5V
3V3
2V5
J4
120
61
J1
1
120
60
61
IDL
Instrumentation
Development
Lab
SCROD_TO_FMC_BOARD
IDL_17_009
KPL
J2
60
1


2V5
3V3
5V
J1_069_AD3
J1_070_AC4
J1_071_AC3
J1_073_AB5
J1_074_AB4
J1_075_AB3
J1_077_AA4
J1_078_AA3
J1_079_Y6
GND
J1
40
FMC_FEMALE_10x40
1