



UNIVERSITY
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MĀNOA

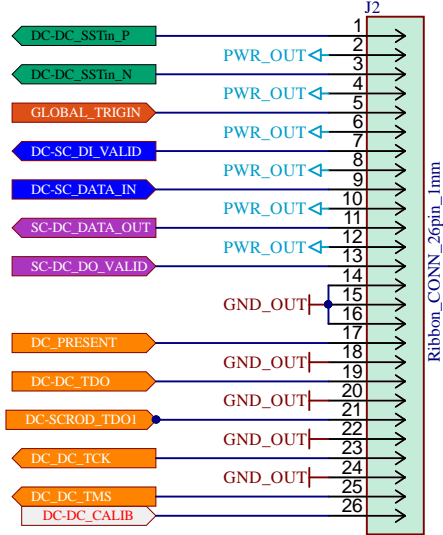
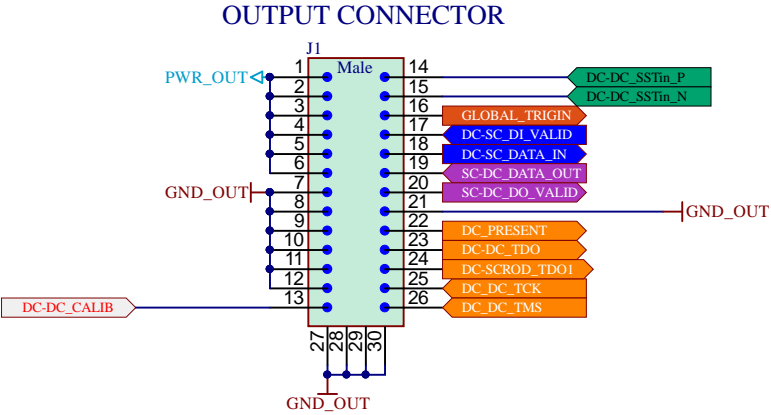
High Energy Physics Group
Instrumentation Development Laboratory
2505 Correa Road, Honolulu, HI 96822

Production Documentation for:

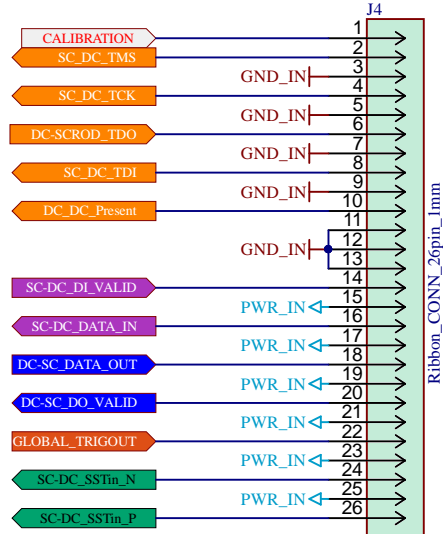
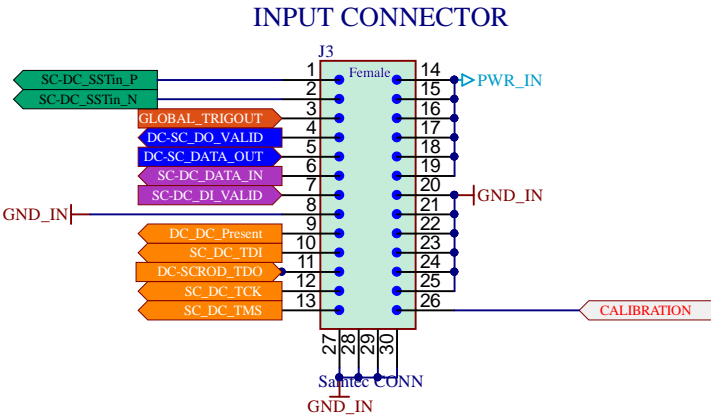
Project Name: *BMD*
Board Name: *BMD CONN BOARD*
IDL num: *IDL_16_017*
Revision: *A*
Variant: *[No Variations]*

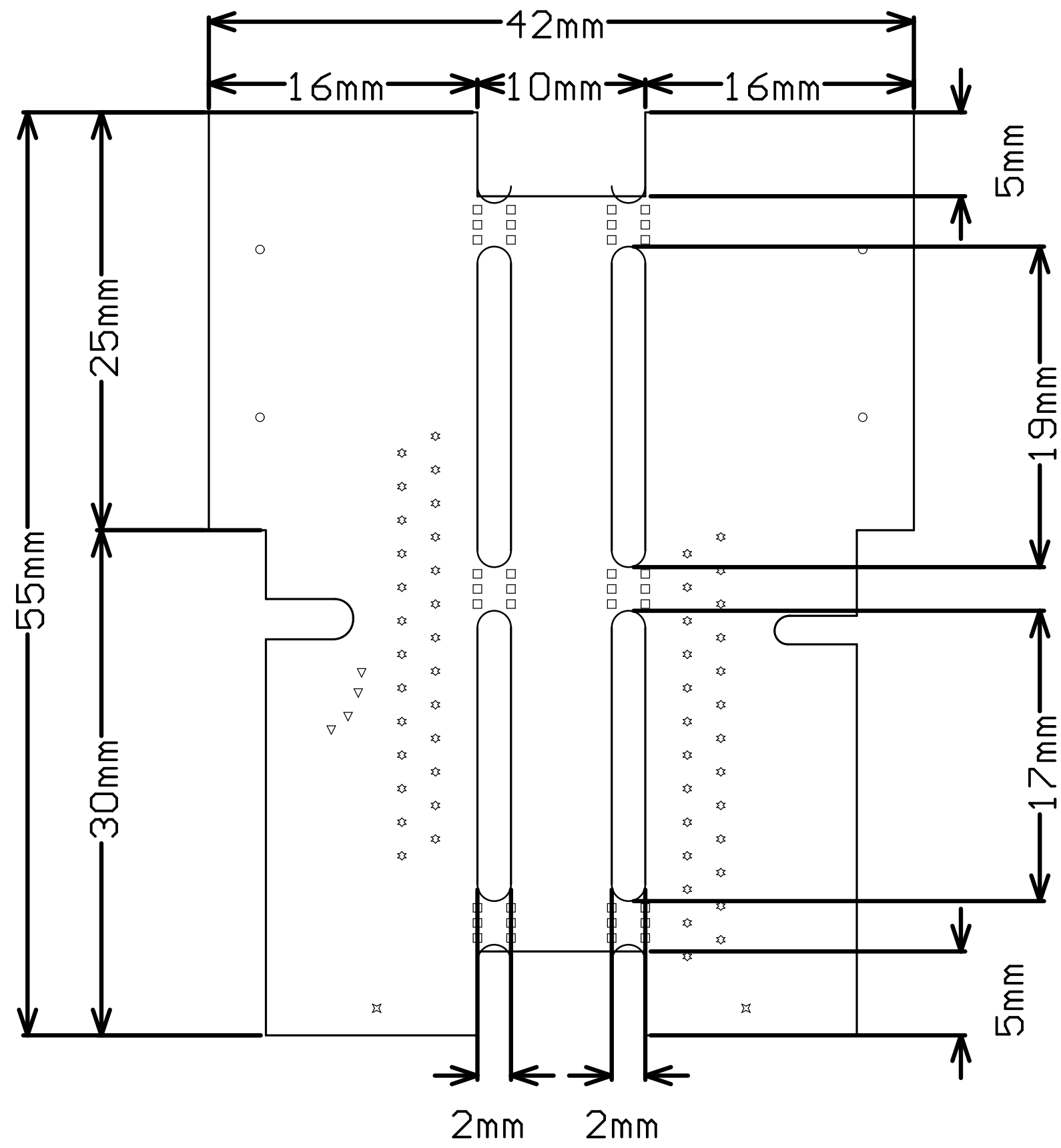
Designer: *Khanh Le*
Drawn by: *Khanh Le*
Approved by: *Gary S. Varner*

MALE CONNECTOR



FEMALE CONNECTOR





Notes:

- Board shall be fabricated - performace class II as per IPC-6011 and IPC6012
- PCB manufacturer logo, P/N, revision and/or date code of manufacturing shall be printed in top solder mask (not over pcb traces, allowed over copper plane).
The date code shall be in the format: "WWYY" where WW=week and YY= year, max height 0.15 inches
- Silkscreen not printed on both sides
- Material: high temperature FR4 class epoxy glass rated UL94V-0. UL symbol and rating shall be marked farside
35um copper for external layers and 18um for all internal layers
Must be RoHS compliant and survive a lead-free assembly max reflow of 260 deg C (5 passes)
Td rating: >340 deg C
Tg = 150 deg C (min)
- Solder mask: SMOBC per IPC-SM-840C, class T must be Rohs compliant, 0.001" max measured over bare copper plating, must clear all lands as indicated on gerber solder mask layers, color= GREEN
- Finish: electro-less nickel immersion gold (ENIG), 0.05-0.125um Au over 3-6um Ni - over bare copper only
- Solderability test: Category 2 of J-STD-003
- Finished boards shall not have nicks, scratches, voids, exposed copper, poor plating or misdrilled holes
- All holes sizes are after plating
- PCB manufacturer may add copper thieving as needed to improve manufacturability, thieving to be 0.030" round pads at 0.050" spacing.
Thieving will have a minimum of 0.100" clearance from existing copper and should not be placed under surface mounted devices
- PCB manufacturer may use tear drops to improve annular rings as long as DRC rules are followed
- All via connections to power and ground planes are solid
- All unconnected pads on inner signal layers are removed
- All finished boards are to be 100% electrically tested
- Unless otherwise indicated, all linear toleracnes shall be XX.X +/-0.2mm and XX.XX +/- 0.1mm
- Gerber file GM1 shows board outline (milling line)
- Table 1 shows Layer stack details

Additional notes:

- A1. Finished board thickness = 1.27mm +/- 0.1mm; measured over top/bottom copper and solder mask

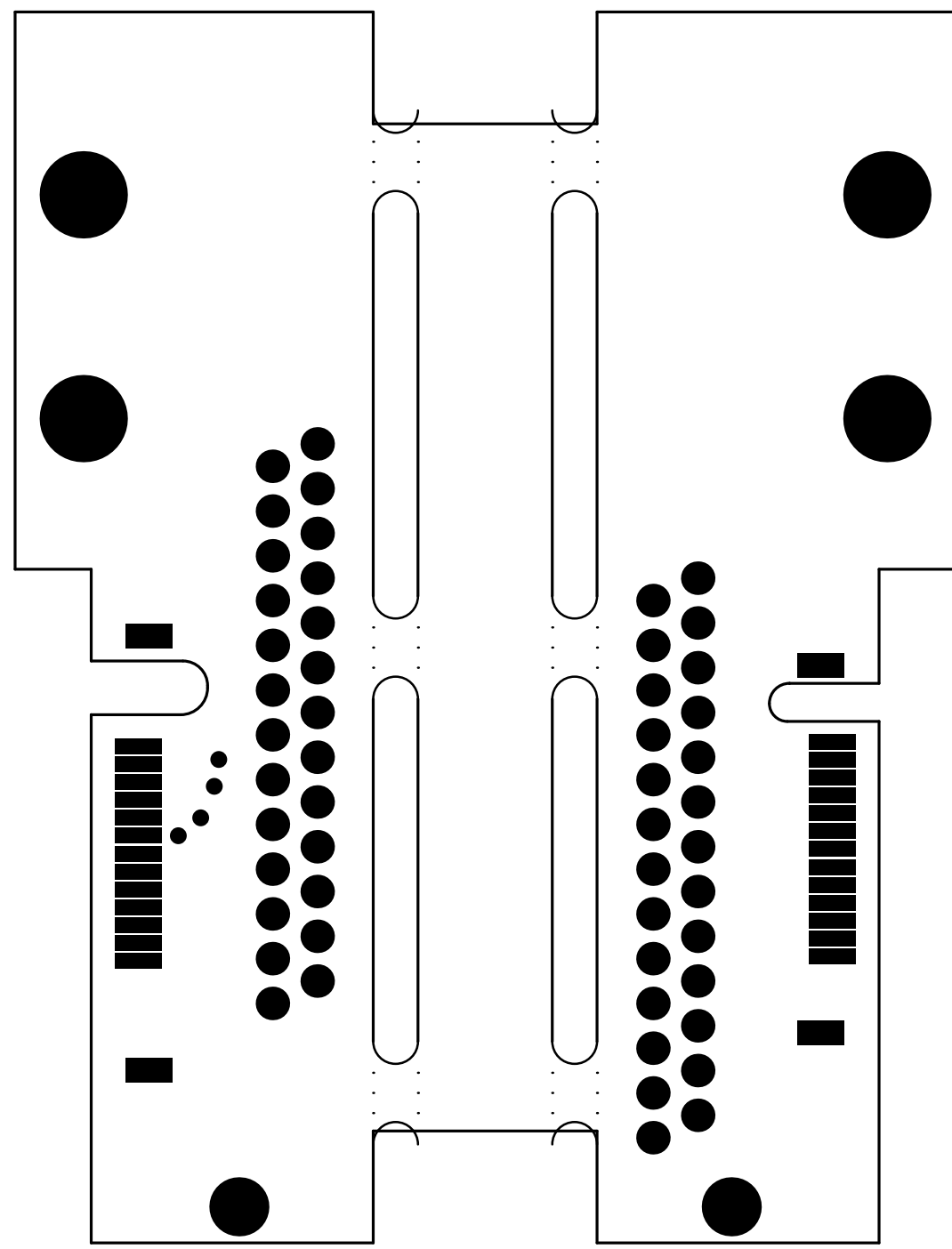
Table 1a: Layer Stack Details for IDL_16_017 Rev.A

Layer	Name	Material	Thickness	Constant	Board Layer	Stack	Board Layer	Stack
1	Top Overlay							
2	Top Solder	Solder Resist	0.010mm	3.5				
3	Top Layer	Copper	0.035mm					
4	Dielectric 1	FR-4	1.486mm	4.65				
5	Bottom Layer	Copper	0.035mm					
6	Bottom Solder	Solder Resist	0.010mm	3.5				
7	Bottom Overlay							

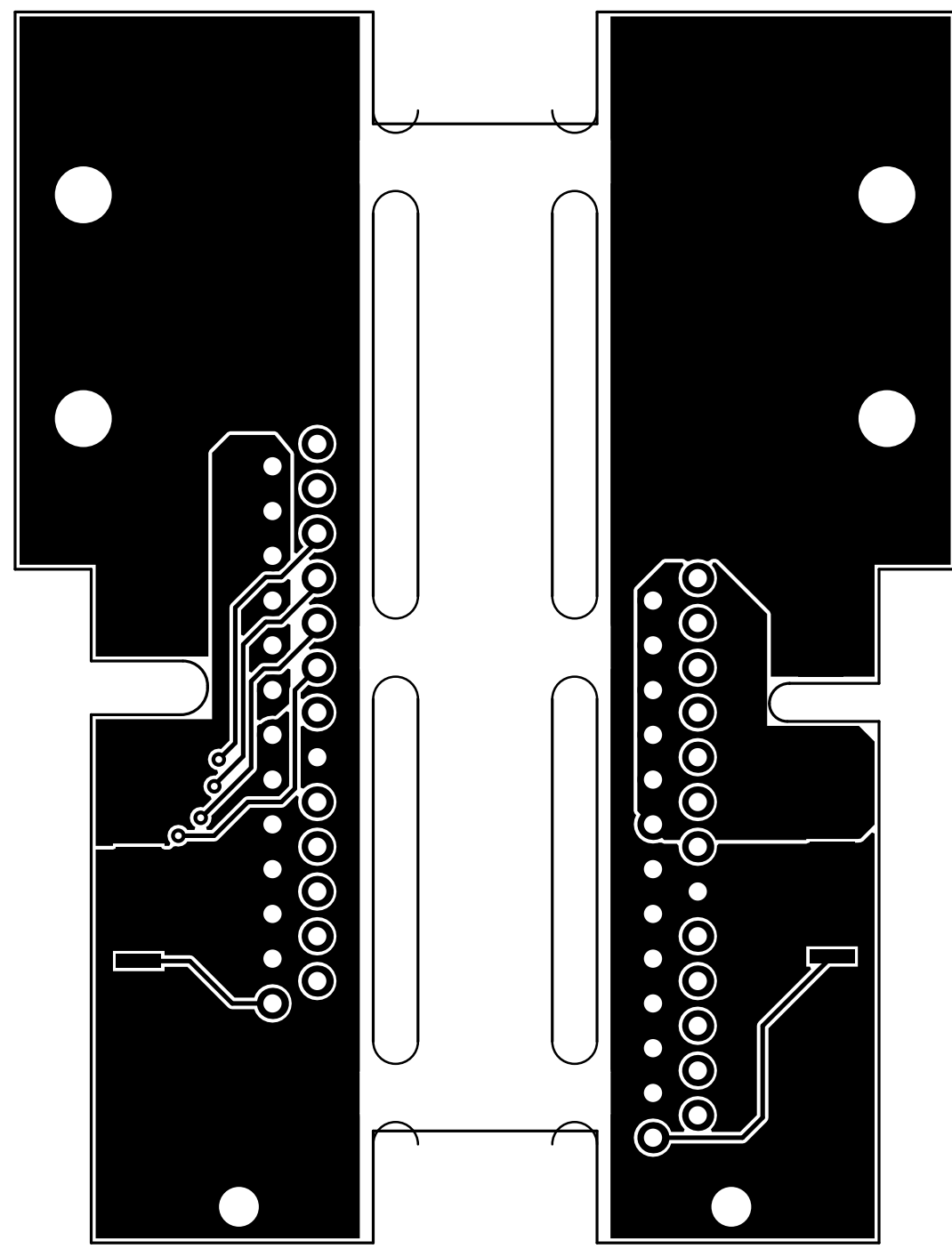
Table 2: Drill Details for IDL_16_017 Rev.A

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape
⌘	2	1.778mm <70.00mil>	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded
∇	4	0.305mm <12.00mil>	PTH	Round	Top Layer - Bottom Layer	Via	Rounded
○	4	2.540mm <100.00mil>	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded
□	36	0.600mm <23.62mil>	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded
☆	52	0.813mm <32.00mil>	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded
	98 Total						

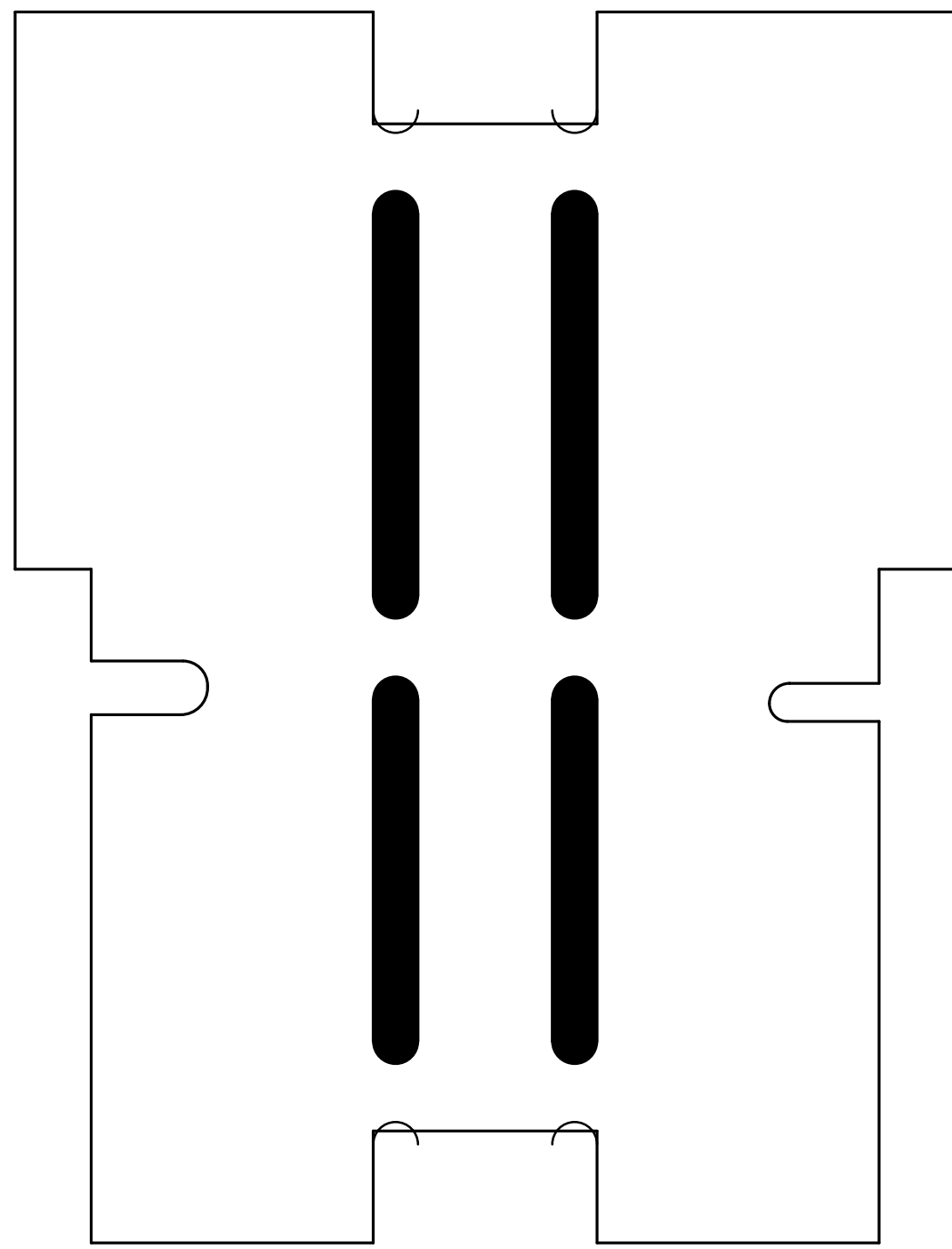
Designer: Khanh Le	Revision: .Version	File: IDL_16_017.PcbDoc	Sheet 1 of 1	Code: IDL_16_017 BMD CONN BOARD
Drawn By: Khanh Le	Modif. Date: Date	Variant: [No Variations]	PCB	
Approved By: Gary S. Varner	Print Date: 1/9/2017	Signature:	Size: A3 H	University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory
Title: Drill Drawing and Dimensions GD1				



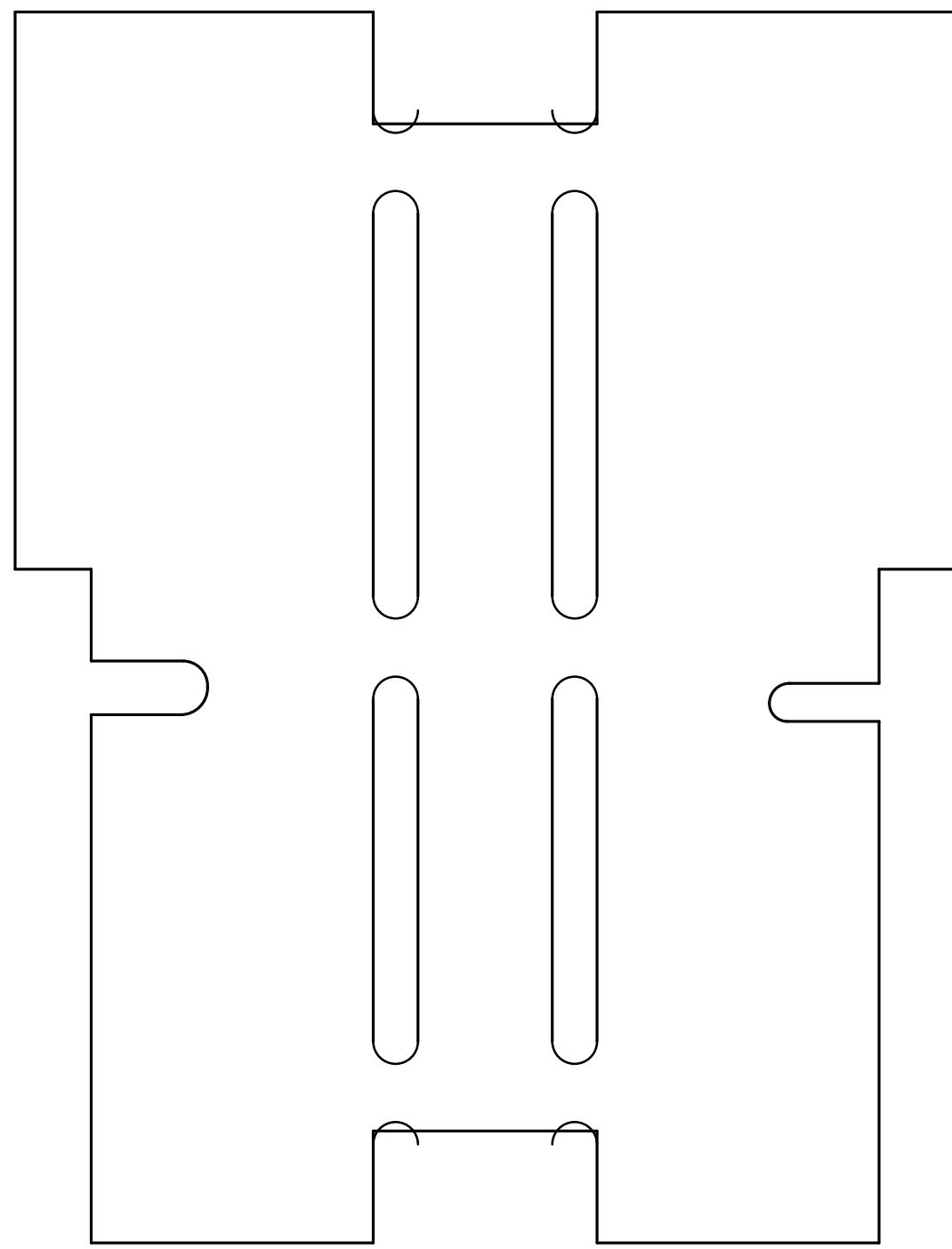
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Drawn By: Khanh Le	Modif. Date: Date	Variant: [No Variations]	PCB	
Approved By: Gary S. Varner	Print Date: 1/9/2017	Signature:	Size: A3 H	ID: BMD CONN BOARD
Title: Top Solder Mask GTS				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory



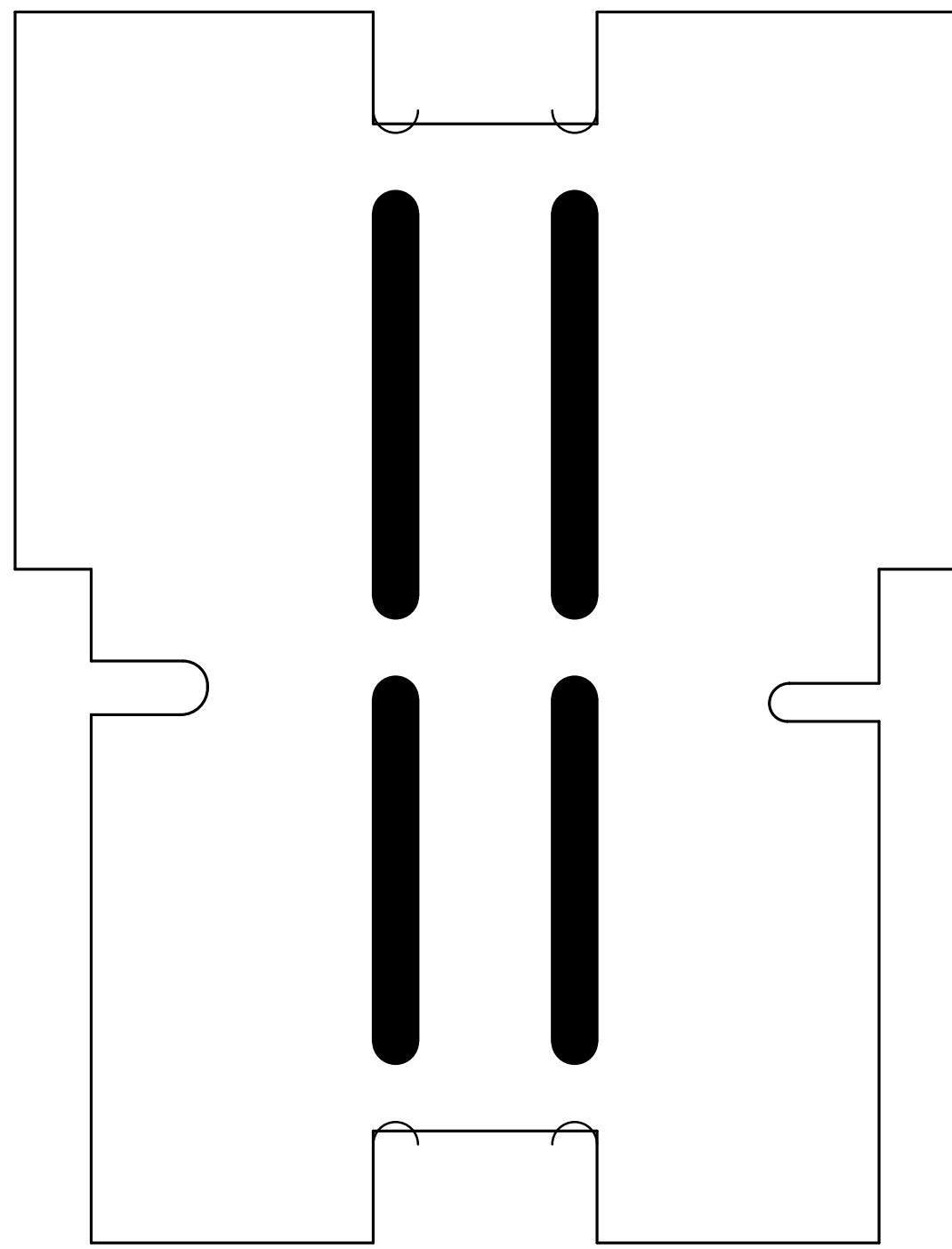
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Drawn By: Khanh Le	Modif. Date: Date	Variant: [No Variations]	PCB	
Approved By: Gary S. Varner	Print Date: 1/9/2017	Signature:	Size: A3 H	ID: BMD CONN BOARD
Title: Top Layer 1 GTL				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory



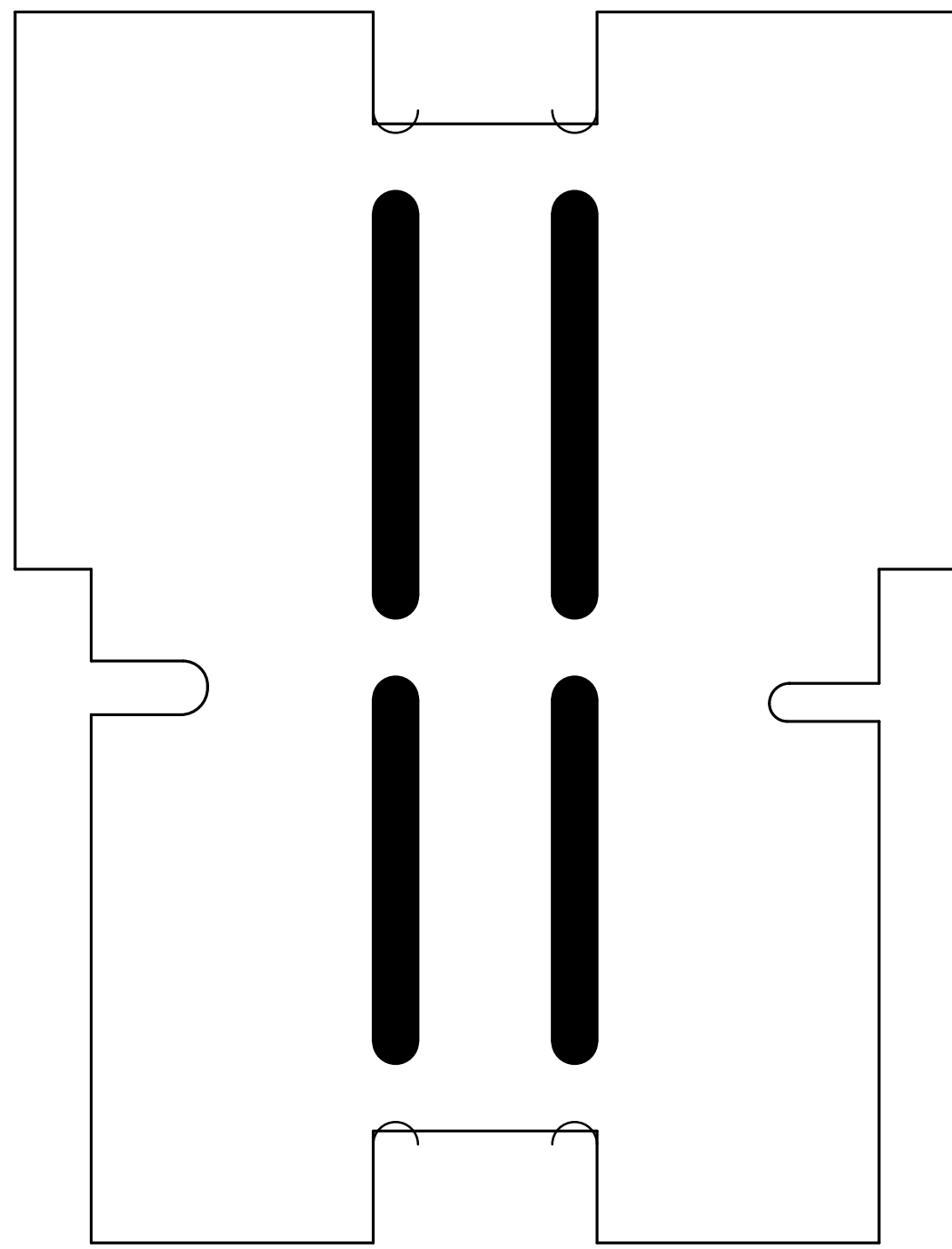
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Approved By: Gary S. Varner	Print Date: 1/9/2017	Signature:	Size: A3 H	ID: BMD CONN BOARD
Title: PWR Plane Layer 2 GP1				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory



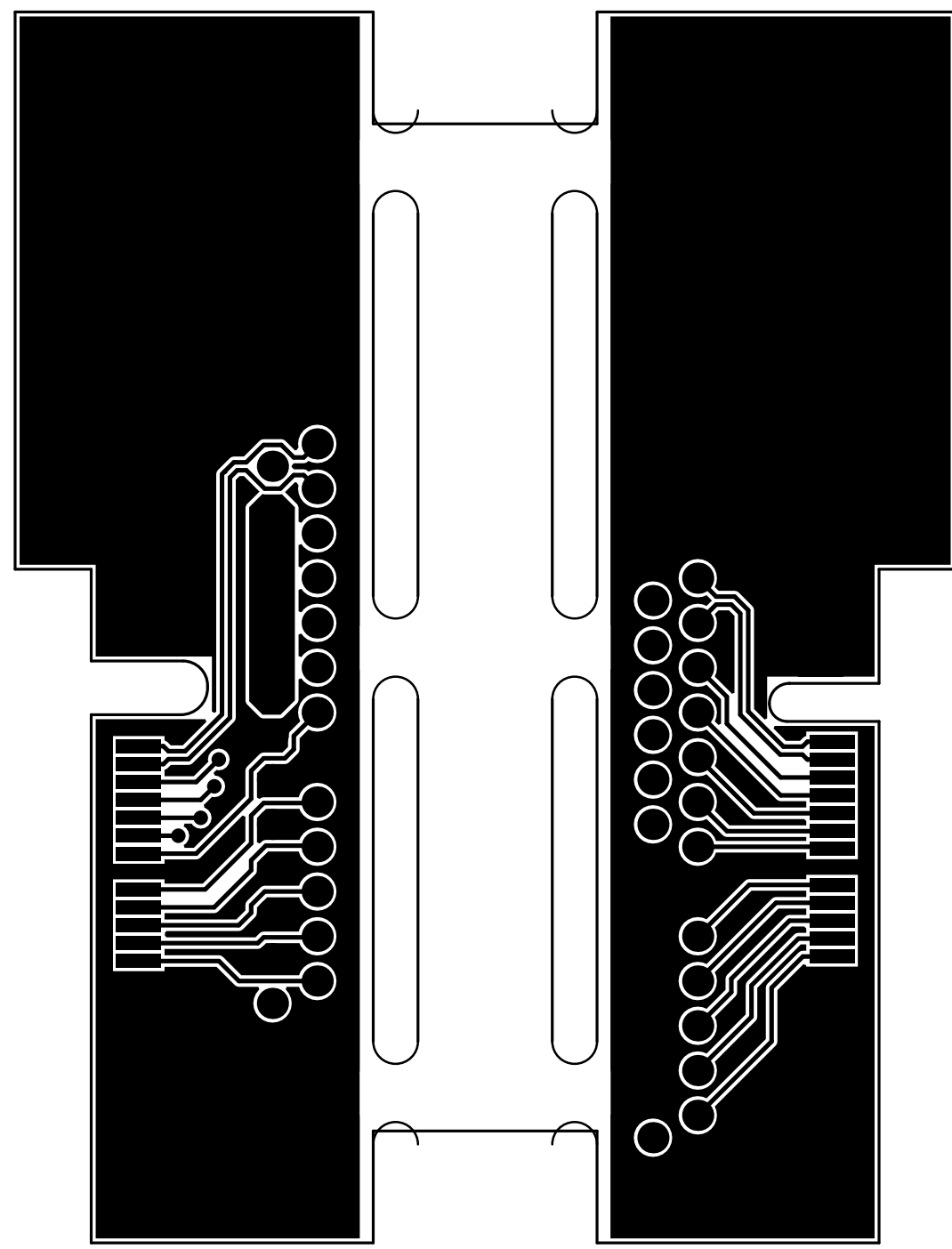
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Approved By: Gary S. Varner	Print Date: 1/9/2017	Signature:	Size: A3 H	ID: BMD CONN BOARD
Title: MID SIG Layer 3 GML1				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory



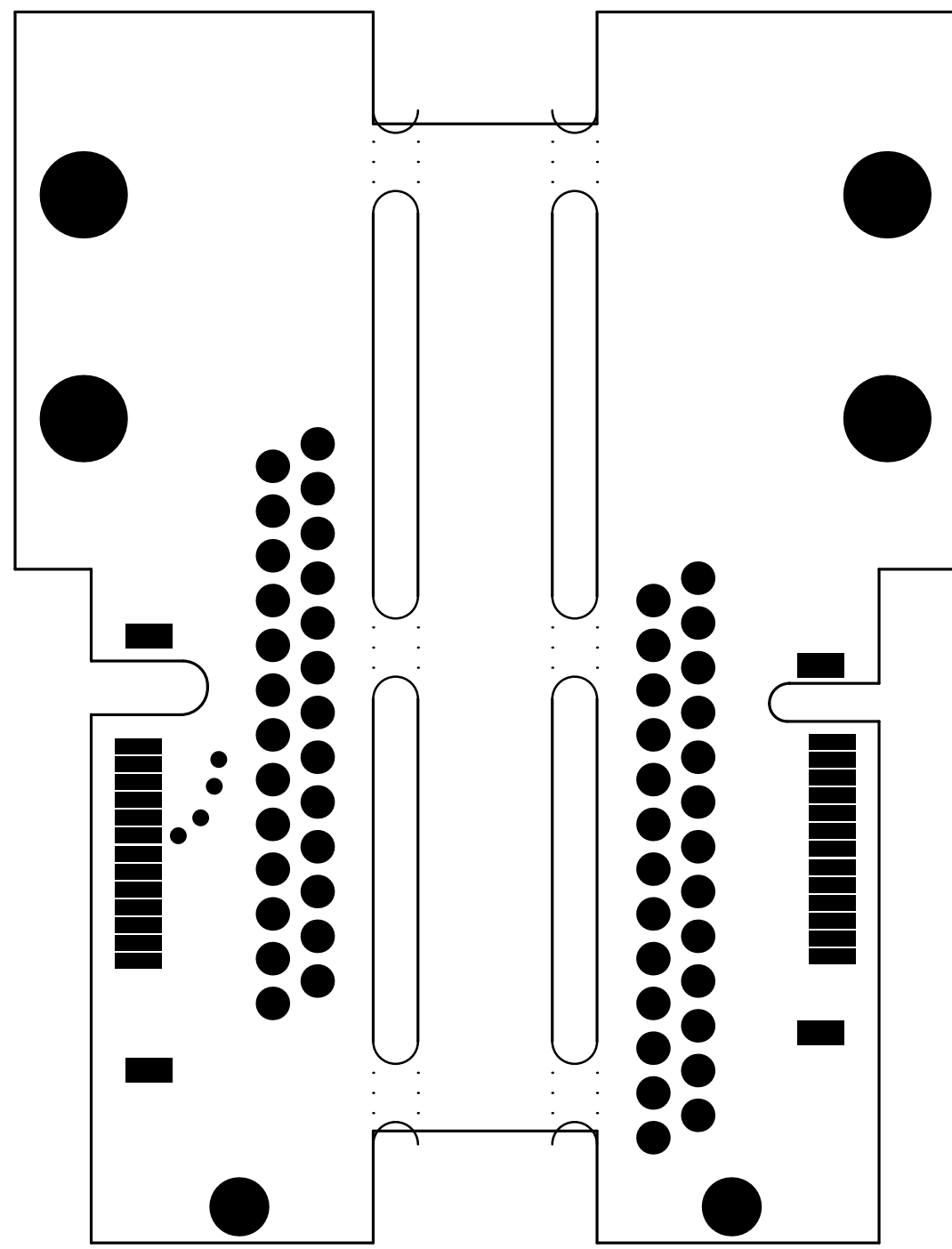
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Approved By: Gary S. Varner	Print Date: 1/9/2017	Signature:	Size: A3 H	ID: BMD CONN BOARD
Title: PWR Plane Layer 4 GP2				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory



Designer: Khanh Le	Revision: .Version	File: IDL_16_017.PcbDoc	Sheet 1 of 1	Code: IDL_16_017
Drawn By: Khanh Le	Modif. Date: Date	Variant: [No Variations]	PCB	
Approved By: Gary S. Varner	Print Date: 1/9/2017	Signature:	Size: A3 H	ID: BMD CONN BOARD
Title: GND Plane Layer 5 GD2				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory



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Drawn By: Khanh Le	Modif. Date: Date	Variant: [No Variations]	PCB	
Approved By: Gary S. Varner	Print Date: 1/9/2017	Signature:	Size: A3 H	ID: BMD CONN BOARD
Title: Bottom Layer 6 GBL				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory



Designer: Khanh Le	Revision: .Version	File: IDL_16_017.PcbDoc	Sheet 1 of 1	Code: IDL_16_017
Drawn By: Khanh Le	Modif. Date: Date	Variant: [No Variations]	PCB	
Approved By: Gary S. Varner	Print Date: 1/9/2017	Signature:	Size: A3 H	ID: BMD CONN BOARD
Title: Bottom Solder Mask GBS				University of Hawaii at Manoa High Energy Physics Group Instrumentation Development Laboratory

