**mRich HODOSCOPE Daughter Card and SCROD\_RJ-45**

**Status Report**

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**Printed Circuit Boards Discussed**

|  |  |  |
| --- | --- | --- |
| **IDL Ref #** | **Official Board Name** | **Report Descriptor** |
| IDL\_18\_014 | BMD Center DC RevB | HODOSCOPE Daughtercard |
| IDL\_18\_020 | SCROD to RJ-45 Connector Board | SCROD\_RJ-45 Board |
| IDL\_15\_002 | SCROD\_RevA5 | SCROD |

1. **Introduction**

The current main objective for the HODOSCOPE Daughtercard (HODOSCOPE) is to have a working proof of concept. Once hardware and firmware functionality has been verified, partially populated boards will be sent to Georgia State University for completion. A complete set of hardware tests have been conducted on the HODOSCOPE including smoke tests, power consumption measurements, FPGA programmability, and amplifier channel functionality tests. Three boards were used for testing and they are now at various stages of population. This report will mainly go over the status of the boards and the results of the tests. If the measured amplifier characteristics meet the needs of the mRICH, then the HODOSCOPE design has passed all hardware tests.

In addition to working on the hardware side of the HODOSCOPE proof of concept, the HMB Daughtercard and the SCROD firmware for the Spartan6 were adapted. Also, Nathan organized and took inventory of the parts kits for each mRICH board. The only missing component is the NP0 500 pF ceramic capacitor for the HODOSCOPE. A requisition form was sent to Matt Andrew on June 1. Nathan also made a task list for all parts of the mRich project the lab is working on. Tasks pertaining to the HODOSCOPE and SCROD-RJ-45, except for the firmware tests, have their statuses updated. The rest of the tasks need to be updated. The inventory and task list spreadsheets were shared with all members of the project and the IDL gmail account.

1. **Board Population Status**

To be ready for the Fermilab beam test, the mRICH needs 4 HODOSCOPE boards (5 including a backup). Three HODOSCOPE boards have been partially populated by Nathan, William, and Julien. We labeled each iteration with “Itr. #”on a piece of masking tape on the RJ-45 connector. Below is a table showing what sections have been populated for each board. Iteration 1 and 2 had their amplifier channels modified for testing, so they need to be recompleted. Note, power rail coupling capacitors may not have been populated, because they were not necessary for hardware testing. Iteration 1 may not be reusable, but the other two are viable specimens (see section 3).

*Table 1. Y = fully Populated, N = incomplete/not populated*

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Iteration #** | **Power: regulators, barrier diode, and passives** | **High Voltage:**  **UltraVolt, barrier diode, and passives** | **Spartan6 FPGA, JTAG connector, and passives** | **TargetX FPGA and Passives** | **DACs and passives** | **Flash memory and passives** | **Amplifier Channel 1 and VPED circuit** |
| 1 | Y | Y | N | N | N | N | N |
| 2 | Y | Y | Y | N | N | N | N |
| 3 | Y | Y | Y | Y | Y | Y | N |

Two to three more HODOSCOPE boards must be populated to meet the quota.

One SCROD\_RJ-45 board is required for the beam test (two including a backup). Currently, there are two SCROD\_RJ-45 boards that have been fully populated. One is currently in use for firmware testing. Therefore, no more SCROD\_RJ-45 boards need to be populated.

1. **Smoke Test and Power Consumption**

Iteration 1 suffered several shorts during its smoke testing. The most devastating was caused by the crossing of the power input and ground nets when the USB connector was improperly mounted (see section 6). It is likely that the barrier diode, D1, was destroyed, because board was powered for a relatively long time while the power and ground nets were crossed. Most of the board was fully populated, which made it difficult to determine other sources of shorts, especially after we discovered the USB issue. By the time all shorts were resolved, most of the board was depopulated. Some of the pads have gone through extensive power cycling, so they may be damaged. We recommend that the board be not reused.

After Iteration 1, the smoke tests were done modularly with population, instead of on a completed board. The first test was done when the voltage regulator circuits were populated. The board was hooked up to a DC power supply whose output voltage was +5.0V and the current limit was 1A. If the there was no drop in the supply’s output and no current drawn, the first smoke test was passed. The next test was conducted when one amplifier channel and the high voltage circuit was added. If there is no drop in the output and less than 100 mA in current draw the second test was passed. The final test was conducted with the Spartan6, the JTAG connector circuits were populated. Power consumption was measured before and after FPGA programming. The regulator outputs were also verified at this time. Table 2 shows the power drawn from the DC supply by iteration 2 during each test. Both iteration 2 and 3 passed the smoke tests.

*Table 2. Iteration 2 Power Consumption as Displayed on the DC Power Supply*

|  |  |  |  |
| --- | --- | --- | --- |
| **Testing Stage** | **Voltage Output** | **Current Draw** | **Power** |
| Regulator Circuit | +5.00V | 0.00A | 0.0W |
| HV module and amplifier channel | +5.00V | 0.009A | 0.0W |
| Spartan6 before programming | +5.00V | 0.024A | 0.1W |
| Spartan6 after programming | +5.00 | 0.052A | 0.2W |

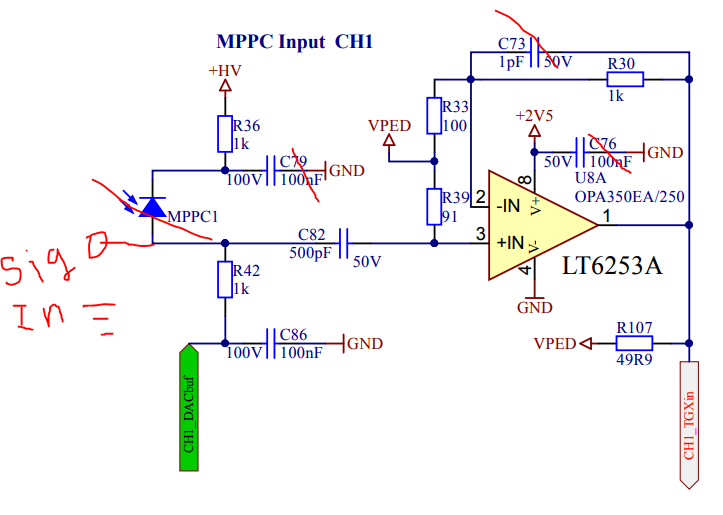
The SCROD\_RJ-45 board with SCROD mounted already passed smoke testing prior to May 12. HODOSCOPE Iteration 3 RJ-45 port was hooked up to the interconnect, and no major changes in power was noticed. We are uncertain what the power consumption of the interconnect and the HODOSCOPE is when communication is active between the SCROD and HODOSCOPE.

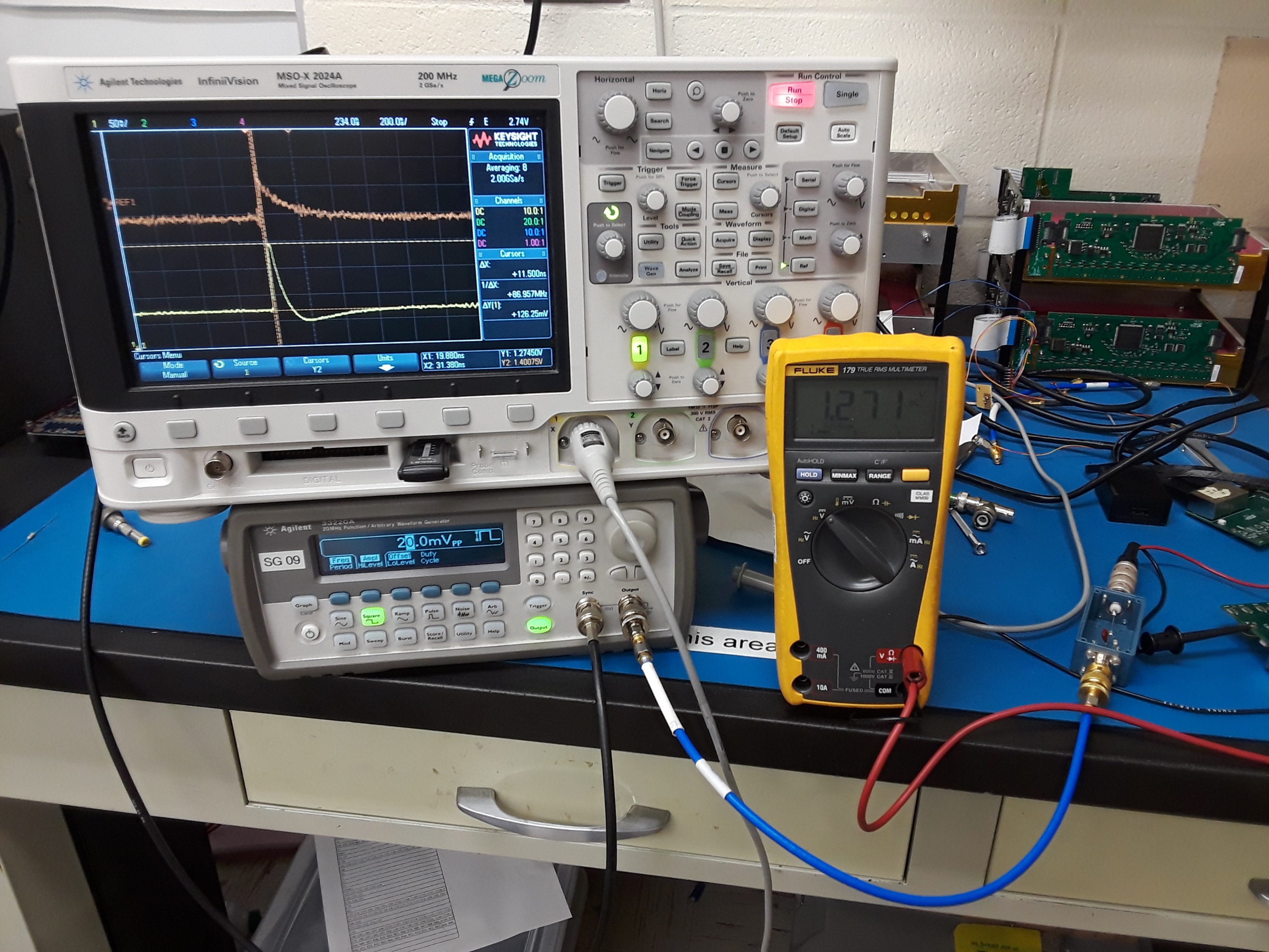
1. **HODOSCOPE DC Amplifier Channel Test**

**4.1 Methods and Setup**

The test was conducted on the amplifier channel 1 of iteration 1 and iteration 2, separately. To mimic an MPPC pulse, we shaped a square wave with CR high pass filter (HPF). The HPF had a time constant of 50 ns (1nF and 50Ω filter was found) before being injected into the amplifier circuit. The square wave had a frequency of 1kHz and an edge time of 5ns. We placed the shaper as close to the circuit as possible, and the output impedance of the function generator was set to 50Ω to minimize reflection and input attenuation. During testing, VPED was varied from 0.8 to 1.42V, and no effect was observed.

The original amplifier circuit was modified for the test. The 1kΩ termination resistor R42 was removed to avoid double terminating the input. Julien suggested that the 1 pF feedback capacitor C73 be removed as well. Figure 1 shows the set up and the modified amplifier circuit. On the oscilloscope, both the input signal (after the shaper) and output signal were observed. To calculate measured gain, we took the ratio of the peak-peak output to input voltages measured by the oscilloscope (see Figure 2). We averaged the signals over 8 periods to eliminate measured noise.



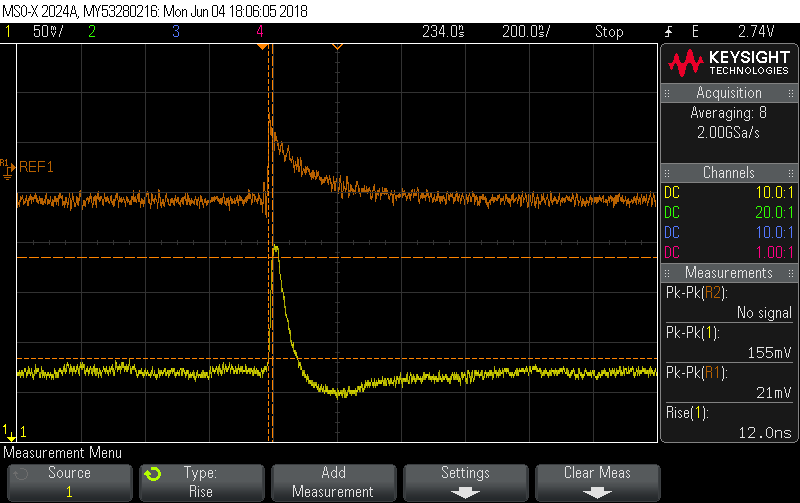
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1. (b)

*Figure 1. (a) Test Setup: Multimeter monitors VPED, blue box is the CR shaper. (b) Modified amplifier schematic. Crossed out components are open circuits. No MPPC, coupling capacitors and termination resistor removed.*

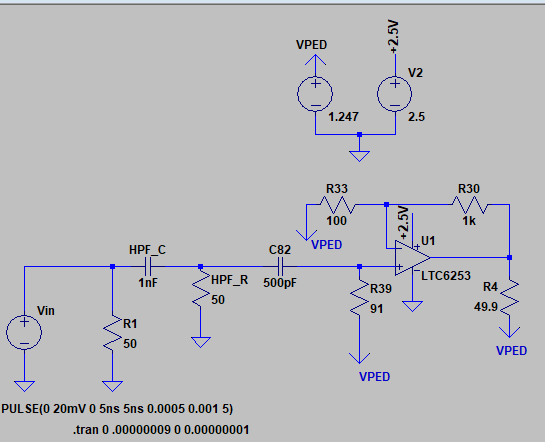
**4.2 Results and Analysis**

The amplifier circuit had a measured voltage gain of 6 up to 8 and an output rise time of 12 ns. When simulated in LTSPICE (see Figure 3 and 4) the amplifier circuit had a voltage gain of 10 and a rise time of ~15 ns. The ideal rise time was 5ns. In LTSPICE the 1nF capacitor was raised to 2nF to see what effect the HPF capacitor had (see Figure 5). The gain was attenuated to 8.59, but the rise time was also ~15ns. Simulated results are very close in agreement with our circuit analysis, where we treated the circuit as a non-inverting amplifier and VPED as ground. Accounting for the lowest open loop gain, the voltage gain of the circuit was 10.98 [1].

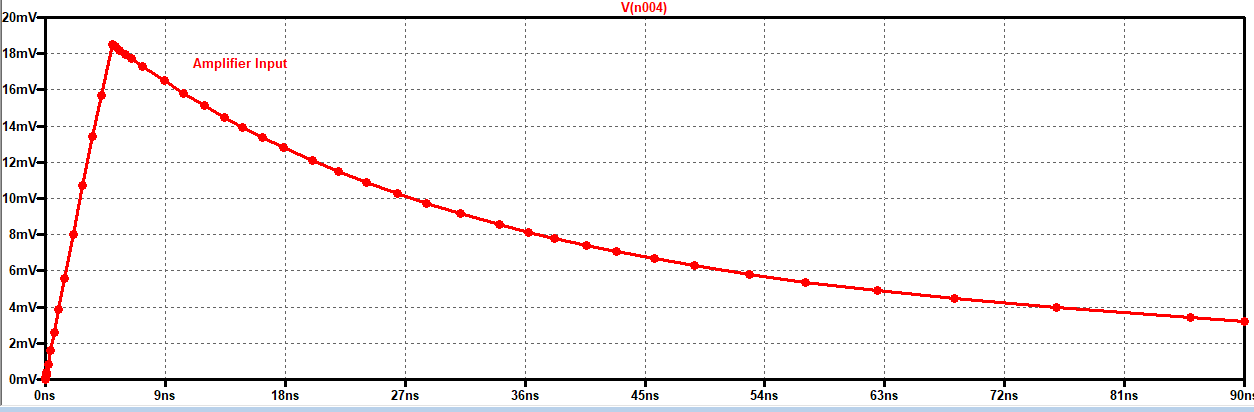


*Figure 2. (Orange) input signal after shaping. (Yellow) output signal. On the right margin are the peak to peak voltages and output rise time. “Pk-Pk{R1}” is the input voltage and “Pk-Pk[1]” is the output voltage. Rise[1] is the output rise time.*

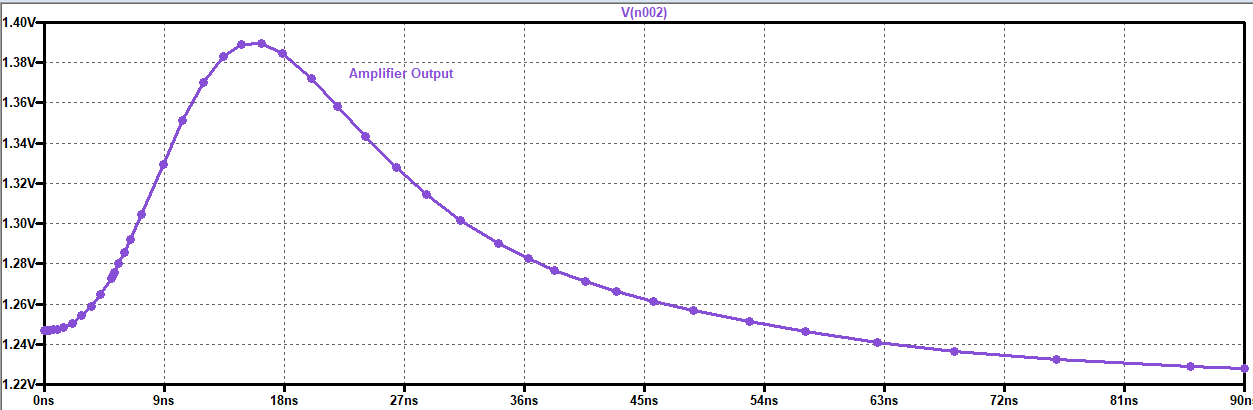
If R1 is removed, and the gain of the amplifier with a 1nF shaper is closer to ~8, which is near within what was measured. These facts suggest that our circuit analysis was right, and the gain discrepancy is sourced somewhere between the function generator and the CR shaper output. Perhaps we mistook the output resistance of the function generator for a resistance to ground instead a series resistance. The simulation shows this is a likely case. When R1 is removed and “Vin” is given a series resistance of 50Ω, the gain was around 7. If we can confirm that the issue lies in the transmission line or termination, then the amplifier is behaving as expected, and we can confirm its functionality.



*Figure 3. LTSPICE simulation of amplifier circuit under test.*

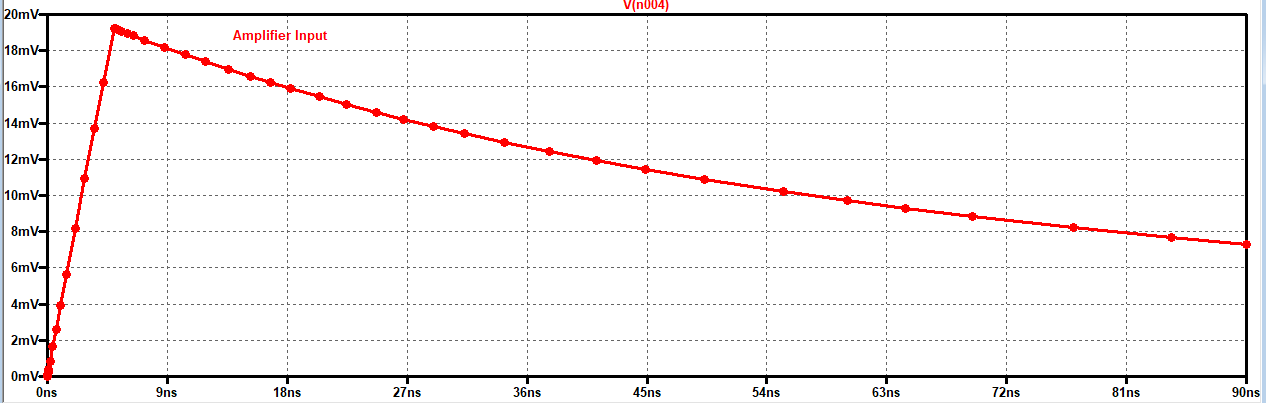
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(a)

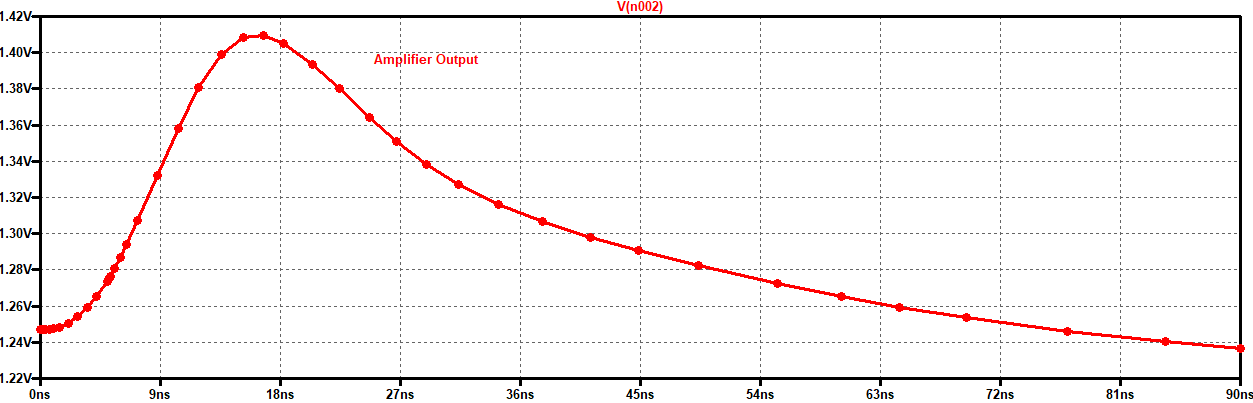


(b)

*Figure 4. LTSPICE waveforms for 1nF CR shaper (a) Amplifier input, within half a period of the shaped pulse. Peak-Peak voltage is about 18.1mV. (b) Amplifier output within half a period. Peak to Peak voltage is 180 mV. Voltage gain is 10. Rise time is ~15 ns.*



(a)



(b)

*Figure 5. LTSPICE waveforms for 2nF CR shaper (a) Input peak-peak voltage 19.8mV. (b) Output peak-peak voltage is 170mV. Voltage gain is 8.59 and rise time is ~15ns.*

1. **Firmware Status**

Existing Spartan6 firmware for both boards needed to be adapted from previous projects. Isar was in charge of modifying the serial communication firmware. The UCF files for the SCROD and HODOSCOPE have been updated by Nathan. Nathan updated the port list of the TOP files. Some of the old signals needed to be expanded into vectors. Nathan modified the old signals throughout the TOP file wherever he was certain of their purpose and left the rest to Isar’s discretion.

1. **Issues:**

There a few small issues with the HODOSCOPE. Most severely, the soldermask for the USB connector calls for the head to mounted on the wrong side. Currently the reference designator and the outline are on the top layer, but the head must be on the bottom layer or else the power input and ground nets will be crossed when the USB cable is connected (see figure #). This is confusing to the one who is populating the board. Eventually, the soldermask should be moved to the bottom side, but for now section 7 gives instructions on how the USB connector should populated.

Other issues are on the schematic. First, the flash memory supply is shown to fed by +1.8V. This net is not found anywhere else on the schematic, and we verified it was not connected to either the +2.5V or +1.2V power rails. Also, on the “GAIN” pins of the DACS one of two jumpers need to be populated to either raise the DAC output by two or one. It is not specified which gain R28 and R29 correspond to. Finally, there is an obsolete formula next to the VPED circuit that can be removed. Documentation issues were not resolved as we were focused on completing the main objective.

1. **Instructions for Population**

The following are tips for populating the HODOSCOPE. We hope these tips will make future population less confusing and faster.

* **D1:** cathode is on pin 1, marked by dot. Cathode should face PWR pin of J1.
* **D2:** cathode marked by 4 lines, known as a the cathode band. Cathode should face inward, and the anode should face outer edge of board.
* **USB:** The connector head should be on the opposite side of the white outline and reference designator J1, or else the power input net and ground will be reversed. ***Remove when soldermask issue is resolved.***
* **Capacitors:** Electrolytic capacitors mark their positive terminal with a bar or dot.

1. **Conclusion**

With the hardware testing complete, firmware functionality testing is all that is left of the HODOSCOPE proof of concept stage. Please refer to Isar for a complete update on the firmware. The next task is to finish populating 5 HODOSCOPE boards. If we can hire more students, we can populate the boards with all sections but 14 amplifier channels missing. If we are short on manpower, we can get 5 boards with FPGAs and power circuits populated before sending it to Virginia for William to complete.

**References**

[1] “OPAx350 High-Speed, Singly-Supply, Rail-toRail Operation Amplifiers MicroAmplifier Series”. Texas Instruments.