What is at hand right now?.

- The latest PMT_SiREAD Board Design [IDL_Ref# IDL_19_004] Documents including PCB, Gerbers and Schematics can be accessed from the https://www.phys.hawaii.edu/~idlab/taskAndSchedule/PCBs/PCBs_homepage.html
- All the 25 fabricated boards are placed in a Box near mRICH station in IDLAB.
- All the required components including op-amps (MSOP package) arrived (June 14, 2019) are placed in the same box on the mRICH station table.
- Out of 25 fabricated boards, at the moment two boards are soldered one with all the components including ASICS while second one with FPGA and power regulators only for testing purpose.
- These boards are Placed on the table close to mRICH station close to Power Supply.
- Temporary JTAG connector was made with soldered wires because of different size of JTAG connector attached to cable and the one which is on the PMT board.
- Both soldered Boards are tested and their FPGA's are Programmed there is no issue right now and can proceed to the next steps for the Further development of FW and Program the FPGA's to complete the Readout chain.
- FW is pushed by Nathan Park, For PMT_SIREAD FW Only SCROD Communication and register processes are available in FW, which can be pulled from github mRICH-FW or HMB-FW on the development branch. The revised FW project is called SiREAD_FW.

This Firmware will be integrated with the Readout FW developed by Ben.