IDLAB – mRICH (SiREAD Based PMT Board Design)

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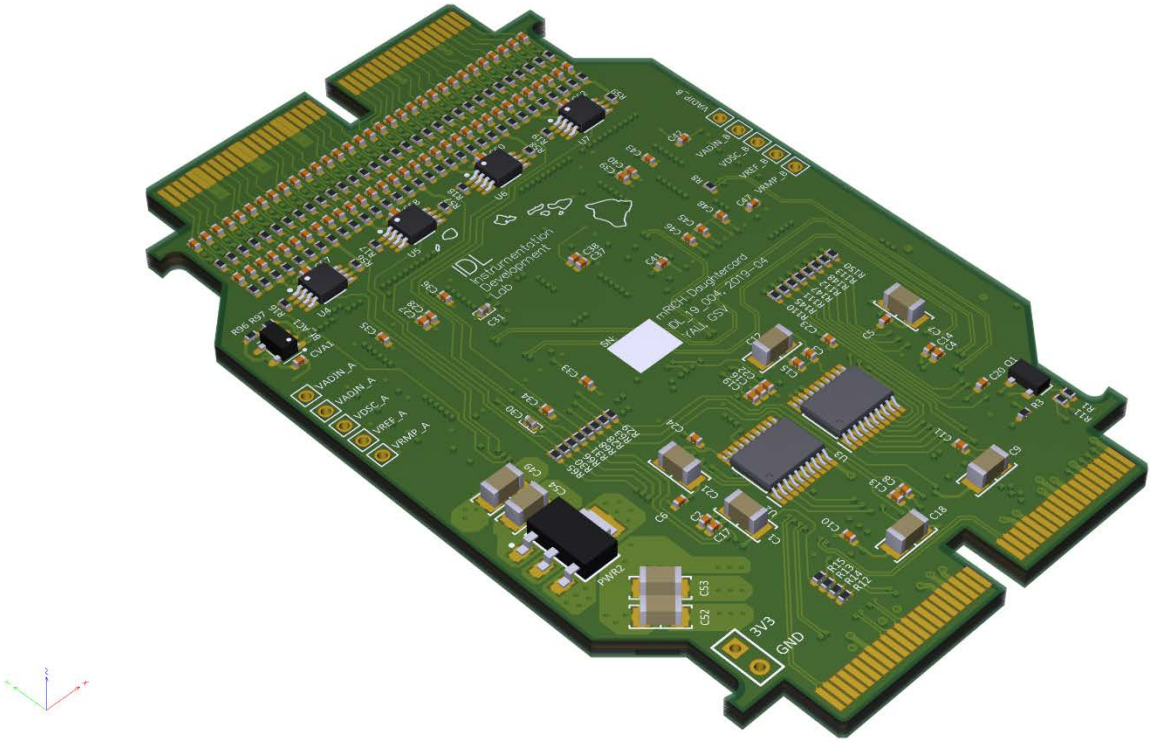
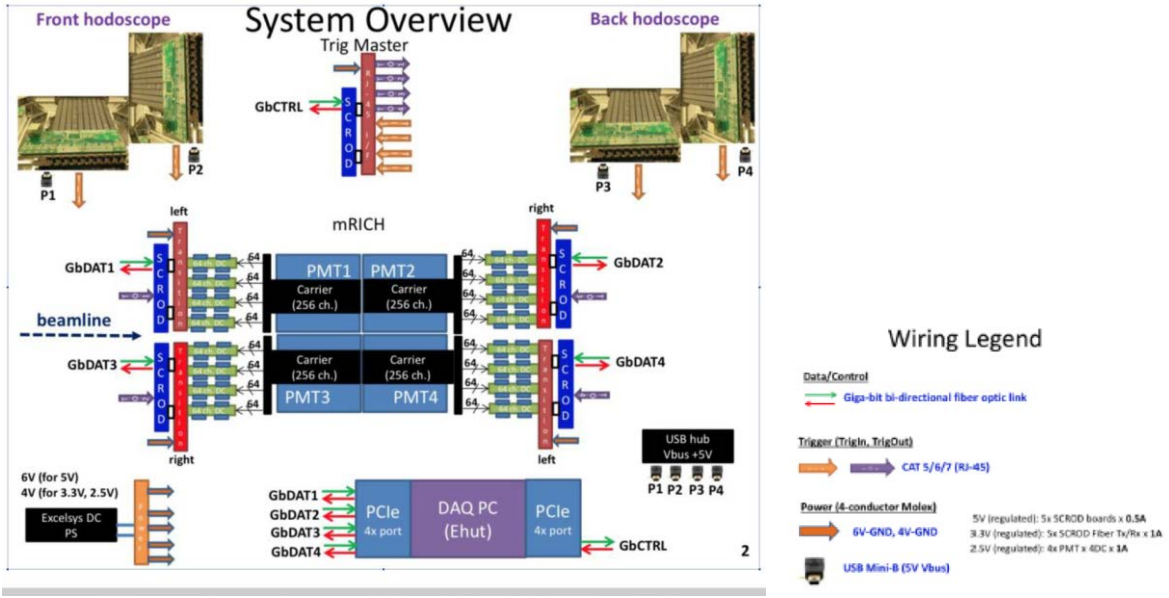
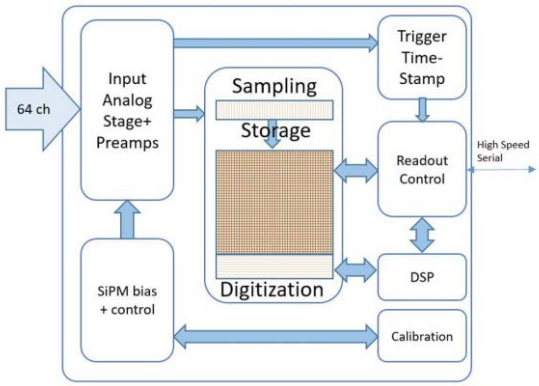


This PMT Board is basically a readout board designed for the Modular Rich (mRICH) ring imaging Cherenkov technology (RICH) which is a Key PID detectors Developed for the future electron Ion collider experiment under the eRD14 collaboration. The Position of these PMT Daughter cards in the broader system is obvious from the following Figure.



These PMT Boards are based on 2 SiREAD chips, The SiREAD is capable of analog signal conditioning and up to 1 Gigasample/sec waveform sampling with the ability to service 32 channels. The SiREAD is a System-on-Chip with built-in SiPM biasing, calibration, and digitization control on the analog side and feature extraction and digital signal processing on the digital side so that it is user friendly and robust to pileup. The block diagram is shown below:



The most updated ALTIUM design Files (Schematic+PCB+Layers Settings etc) is available on Desktop of the Lenovo core i7 Laptop in room WATT 225 in a Folder named “PMT_Board_Design”. The Folder includes the ALTIUM Libraries used also if needed can be downloaded from:

https://techdocs.altium.com/display/ADOH/Download+Libraries

To Get starting with the ALTIUM. There is a Folder with a name “ALTIUM” inside the Folder “PMT_Board_Design” A very detailed word document is placed in it which describe how to set up a project by using the project template. How and install and setup ALTIUM and the Design steps.

The Folder also contains Gerber files send to PCB Universe for Board Fabrication. It also contains SIREAD ASIC description including its schematic and its description. The same files are also available on the IDLab webpage with ID ref (IDL_19_004):

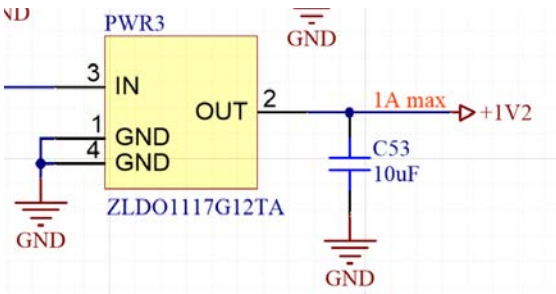
https://www.phys.hawaii.edu/~idlab/taskAndSchedule/PCBs/PCBs_homepage.html

- We need 16 Boards for mRICH but we have 25 Boards Fabricated.
- All the 25 fabricated Boards are placed in a Box near mRICH station in IDLAB.
- All the required components including op-amps (MSOP package) arrived today (June 14, 2019) are placed in the same box on the mRICH station table.
- Out of 25 fabricated boards, at the moment two boards are soldered one with all the components including ASICS while second one with FPGA and power regulators only for testing purpose.
- These boards are Placed on the table close to mRICH station close to Power Supply.
- Temporary JTAG connector was made with soldered wires because of different size of JTAG connector attached to cable and the one which is on the PMT board.
- Both soldered Boards are tested and their FPGA’s are Programmed there is no issue right now and can proceed to the next steps for the Further development of FW and Program the FPGA's to complete the Readout chain.

Two soldered Boards are shown below: (Need to solder components on more boards)

In order to apply power to the boards carefully apply 3.3 V to the right pin of the connector. This is just for the tests eventually it will be inserted to the carrier board from one end which will be connected to the PMT, while the other end will be connected to the SCROD (which will be connected via Ethernet cable with the PC) as shown in the bottom Figure on the next page.

It is optional to revise the design for the two minor changes but for now it is not required. Regulator's pin 4 should be connected to the output but accidentally connected to GND but for the solution for now a piece of Kapton tape was placed over the tab's pad for the 1.2V supply and can be repeated for other boards as it works and is tested. Also Pull up resistor (4.7k 5%) on pin 39 of FPGA is required (signal INIT_B) and need to connect to 2.5V_F which is also connected for the already soldered boards.



The FPGA on board is Spartan 6 XC6SLX9 whose data sheet can be accessed at:

https://www.xilinx.com/support/documentation/user_guides/ug385.pdf

PMT SiREAD Firmware (FW) is already started but is in development phase. FW is mostly pushed by Nathan Park. The detailed document is Present in the Folder named "FW_Doc" and is located on the Desktop of the Lenovo core i7 Laptop in room WATT 225. This document describes the layout of FW on the SCROD and (mRICH) DC FPGAs. The DCs are controlled by one Standard Controls and Read Out, and Data (SCROD) master board, which has its own FPGA that reads out data from the DCs and passes it to the user's PC.

The SCROD Rev A5 master board receives commands from the PC, relays commands to the DCs, and collects data from the DCs for the PC. Communication between PC and SCROD is maintained through a fiber optic Ethernet interface, while communication between the SCROD

and DCs are maintained through CAT-6 cables terminated with RJ45 connectors. The main components of the SCROD board include:

1. PCI express optical gigabit transceiver: interfaces with PC, sends and receive packets of information to and from PC.
2. Xilinx Spartan-6 FPGA(lx150T package): parses commands, communicates with Daughtercards, processes data, and sends data to and receives data from the optical transceiver.

For the PMT SiREAD FW mostly SCROD communication is done. The code can be accessed from git Repository on mRICH-FW or HMB-FW on the development branch. The revised FW project is called SiREAD_FW, while it needs to be integrated with Ben's (NALU Scientific) readout firmware

https://github.com/nathankp/HMB-FW/tree/development/EIC-Beamtest-FW/mRICH_hodo_DC_V1