**fADC250V2 – 250 MSPS Pipelined flash ADC**

- Fewer Parts
- Lower Power (56 W)
- SPI for config/read-back
- Test Vector Generation
- Newer Gen FPGAs.

- Tests - 3rd Qtr 2010.
- Engineering Run – 1st Qtr 2011.
- Production – 1st Qtr 2012 (300 units for Hall D).
GlueX Level 1 Timing

2.3μs measured latency

Front-end Crate

660ns estimated latency remaining

Global Trigger Crate

Trigger Distribution Crate

2.3μs (measured) + 660ns (estimated) < 3μs!