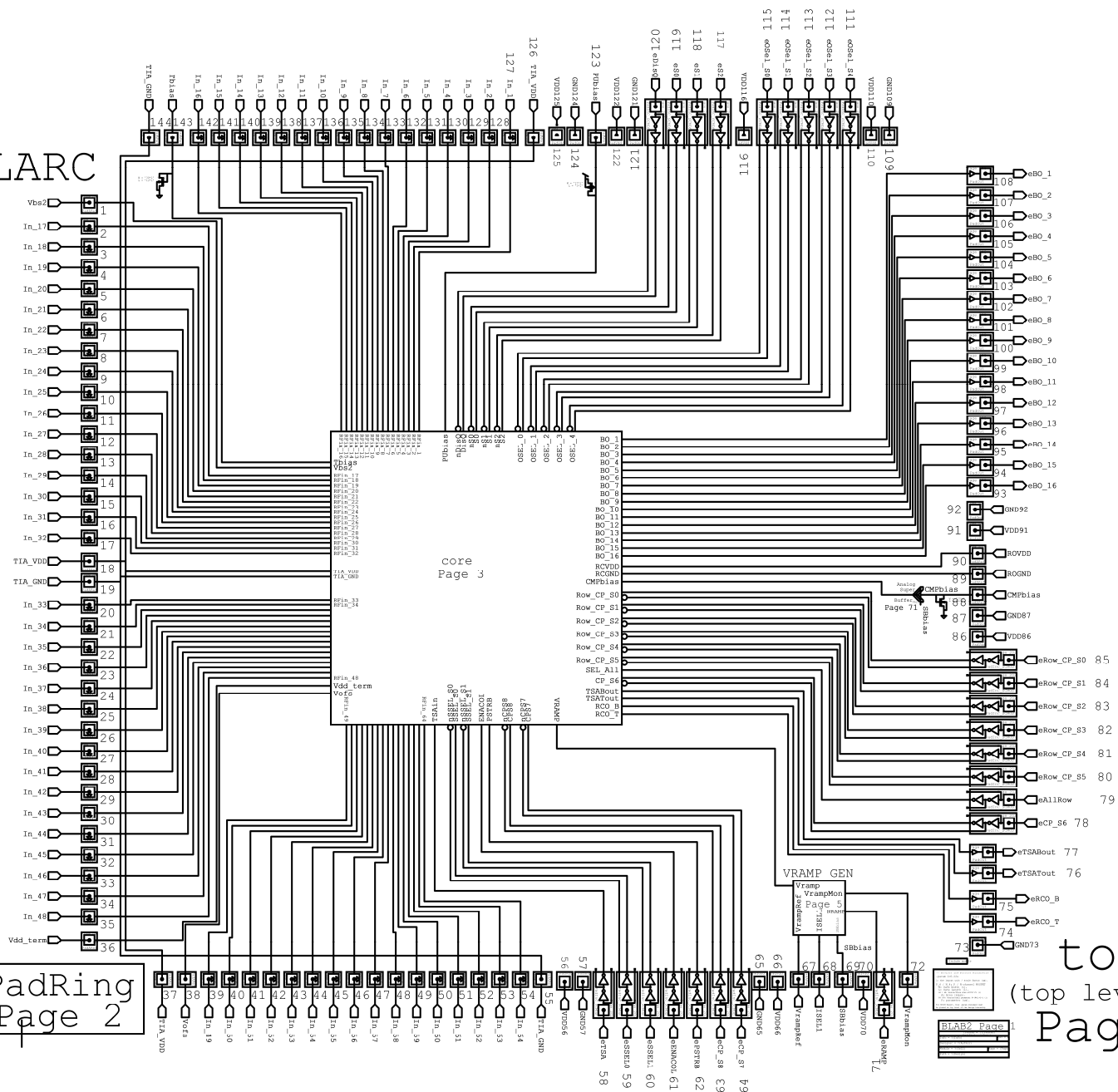


LARC

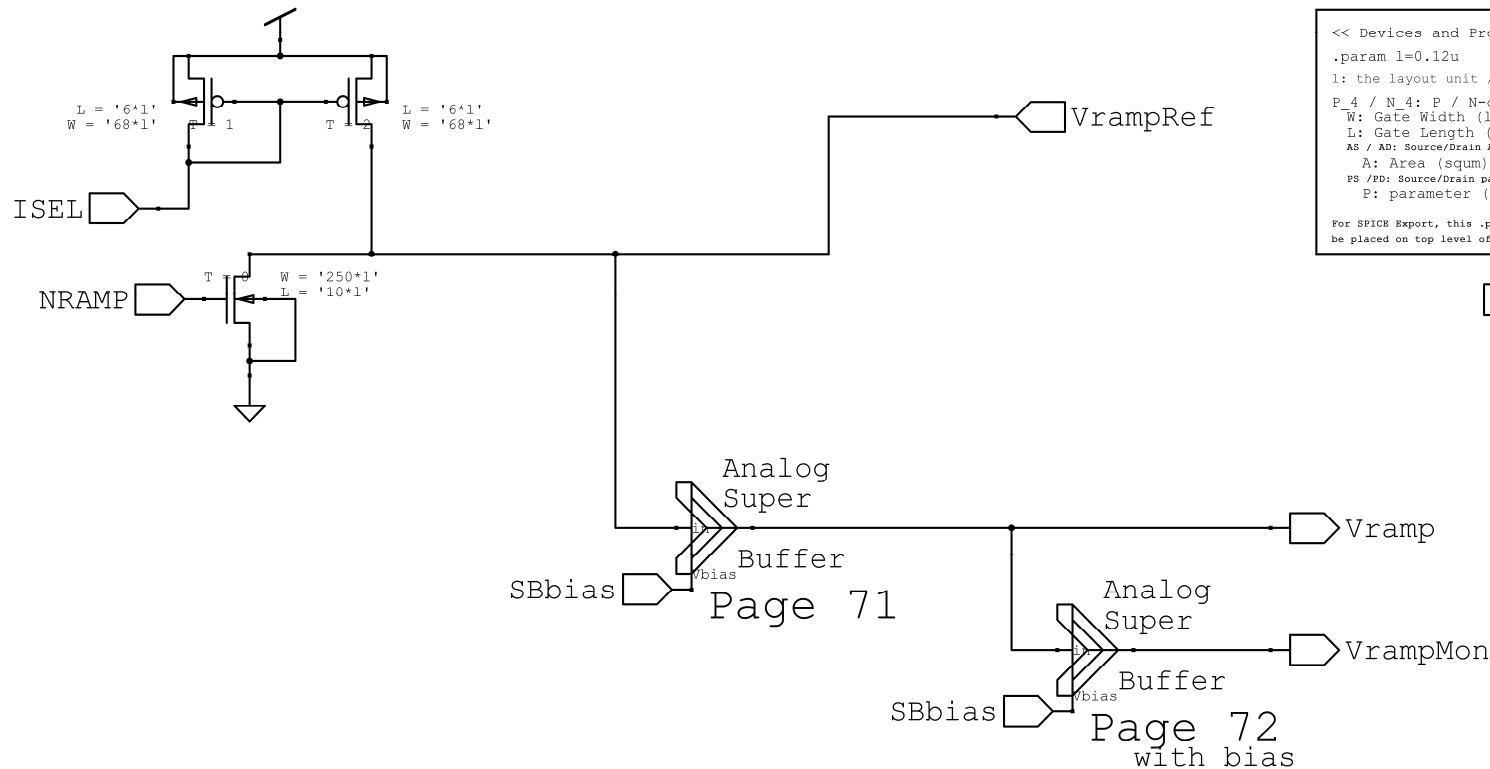
PadRing
Page 2



top
(top level sheet)
Page 1

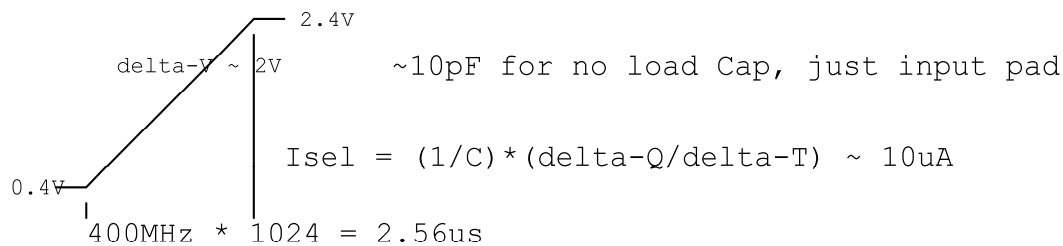
SIAB7 Page 1

Voltage Ramp Generator (VRAMP_GEN)



```
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
```

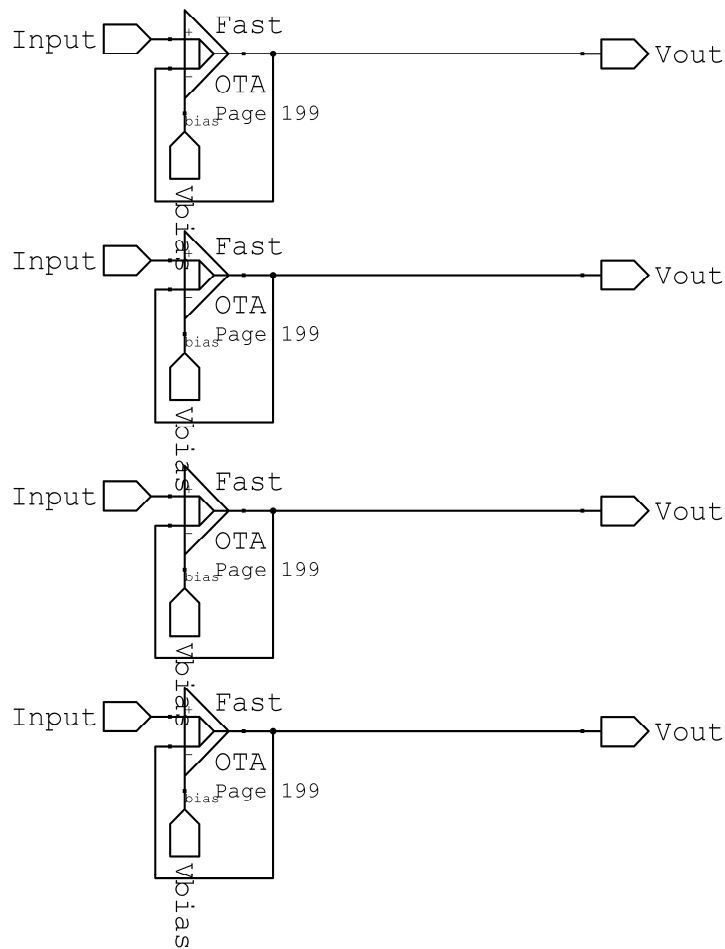


$$I_{sel} = (1/C) * (\Delta Q / \Delta T) \sim 10\mu A$$

Page 5

University of Hawai'i, Manoa		Tel = (808)956-2920
Instrument Development Lab (IDL)		Fax = (808)956-2930
2505 Correa Road, Honolulu, HI 96822		
Created = ?(Created)		Size = 5x7
Modified = ?(Date)		Rev = A
Info = ?(Info)		
Designer = ?(Author)		
Module = ?(Cell)		Page = {Page}
Path = ?(Design)		

Analog Output Super Buffer (ao_superbuff_wbias)



```
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P 4 / N 4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
```

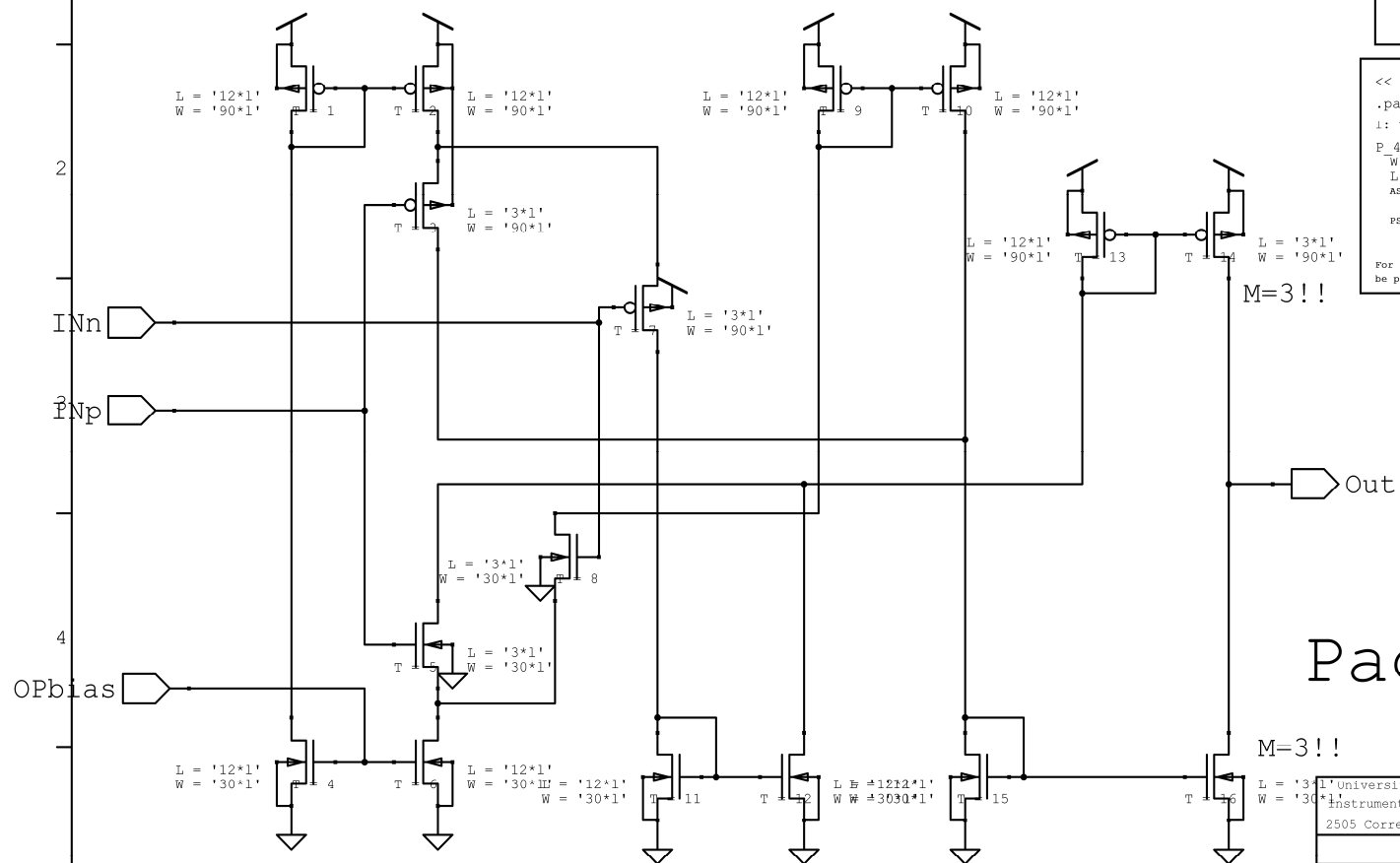
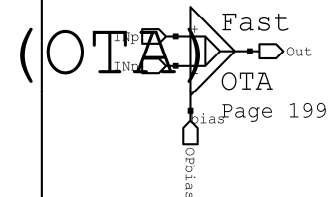
Include models

Page 72

University of Hawai'i, Manoa		Tel - (808)956-2920
Instrument Development Lab (IDL)		Fax - (808)956-2930
2505 Correa Road, Honolulu, HI 96822		
Created = ?{Created}		Size = 5x7
Modified = ?{Date}		
Info = ?{Info}		Rev = A 5
Designer = ?{Author}		
Module = ?{Cell}		Page = {Page}
Path = ?{Design}		

L = '12*1'
W = '30*1'

OTA for Fast performance



<< Devices and Process Parameters >>
 .param l=0.12u
 l: the layout unit / scale factor (um).
 P 4 / N 4: P / N-channel MOSFET
 W: Gate Width (l).
 L: Gate Length (l).
 AS / AD: Source/Drain Area A=W*L*1 (l)
 A: Area (squm).
 PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
 P: parameter (um).
 For SPICE Export, this .param statement must
 be placed on top level of the design hierarchy.

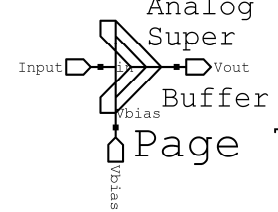
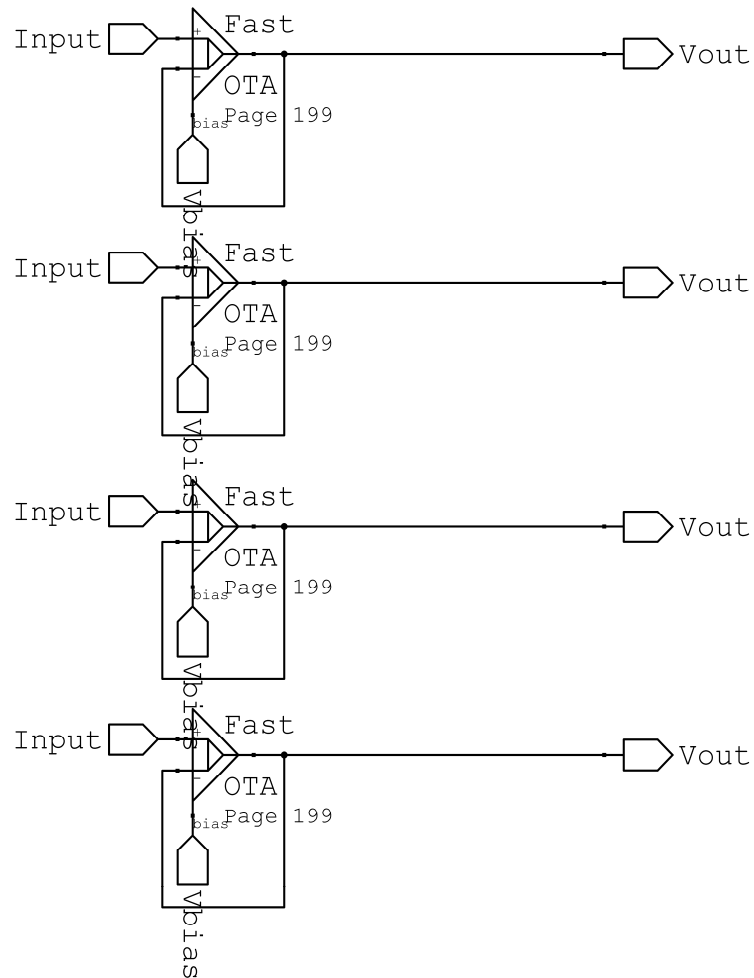
Include models

Page 199

M=3!!

University of Hawaii, Manoa		Tel = (808) 956-2920
Instrument Development Lab (IDL)		Fax = (808) 956-2930
2505 Correa Road, Honolulu, HI 96822		
Created = ?{Created}	Size = 5x7	
Modified = ?{Date}	Rev = A	
Info = ?{Info}		
Designer = ?{Author}		
Module = ?{Cell}		Page = {Page}
Path = ?{Design}		

Analog Output Super Buffer (ao superbuff)_{AT}



```
<< Devices and Process Parameters >>
.param l=0.12u
1: the layout unit / scale factor (um).
P_4 / N_4 : P / N-channel MOSFET
W: Gate Width (1l).
L: Gate Length (1l).
AS / AD: Source/Drain Area A=W*L*1 (1)
A: Area (squm).
PS / PD: Source/Drain perimeter P=(W+L)*2*1 (1)
P: parameter (um).

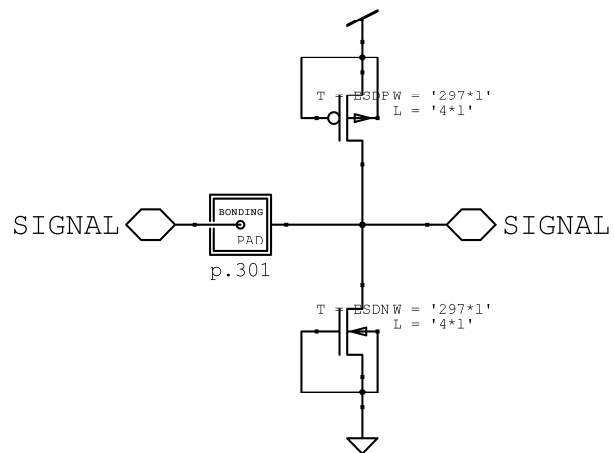
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
```

Include models

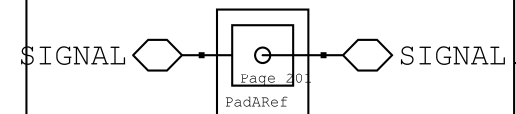
Page 71

University of Hawai'i, Manoa		Tel = (808) 956-2920
Instrument Development Lab (IDL)		Fax = (808) 956-2930
2505 Correa Road, Honolulu, HI 96822		
Created = ?{Created}		Size = 5x7
Modified = ?{Date}		
Info = ?{Info}		Rev = A
Designer = ?{Author}		
Module = ?{Cell}		Page = {Page}
Path = ?{Design}		

PadARef



Include models



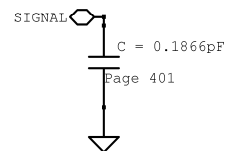
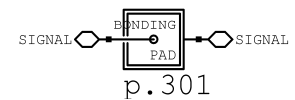
```
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
```

Page 201

University of Hawai'i, Manoa		Tel = (808)956-2920	
Instrument Development Lab (IDL)		Fax = (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created = ?{Created}		Size =	5x7
Modified = ?{Date}			Rev = A
Info = ?{Info}			
Designer = ?{Author}			
Module = ?{Cell}		Page = {Page}	
Path = ?{Design}			

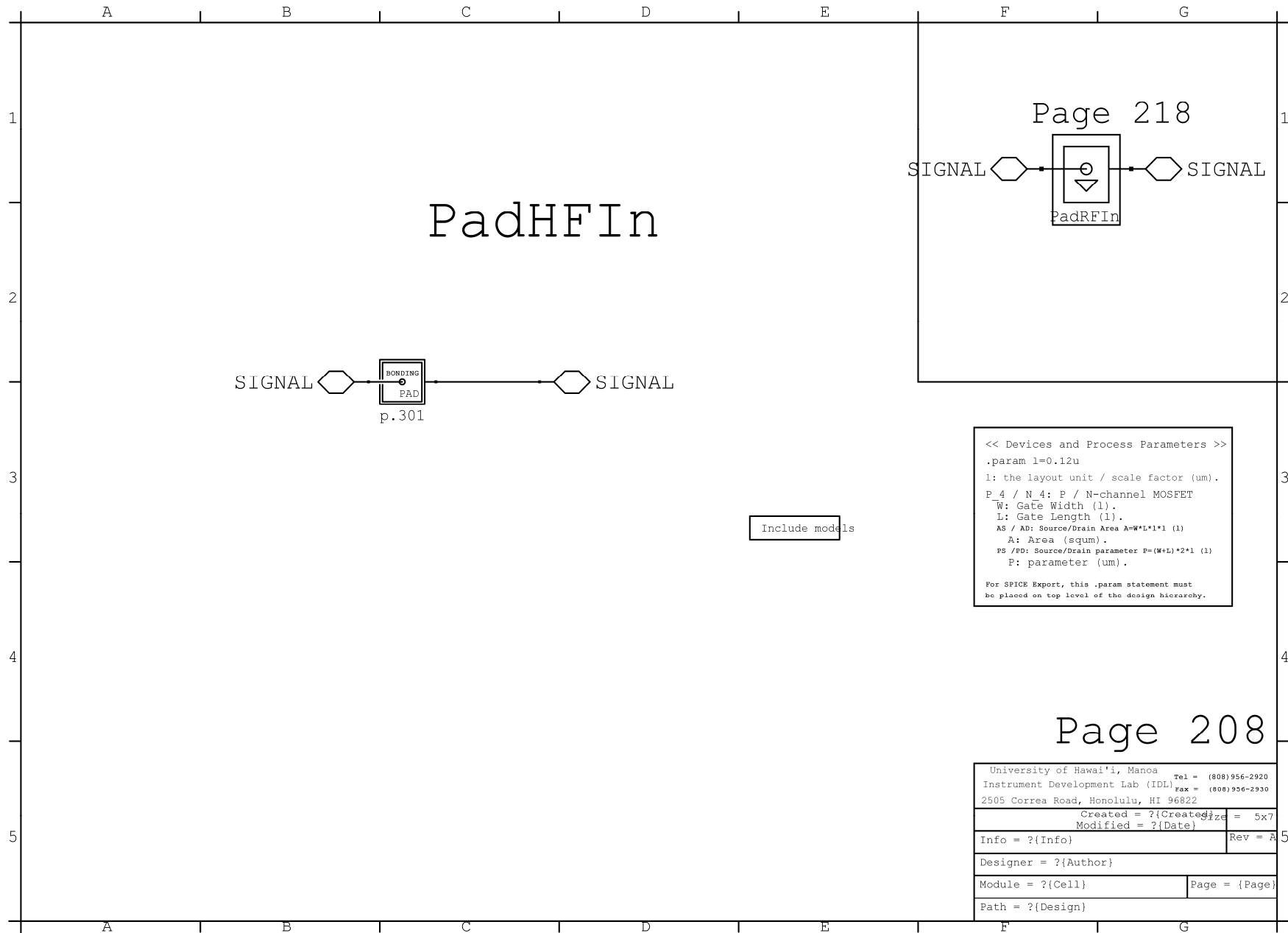
Pad_Bond

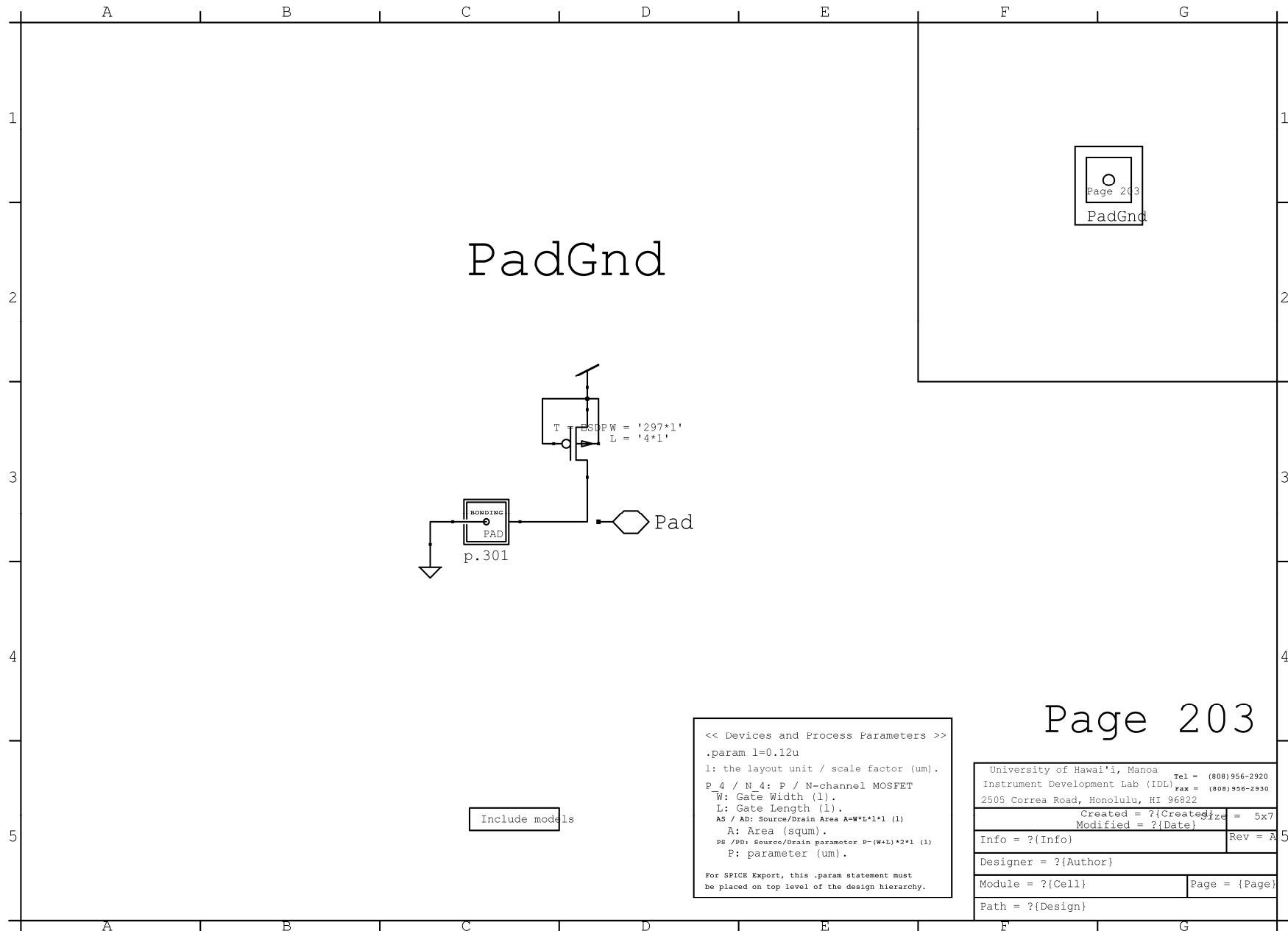


Page 401

Page 301

University of Hawai'i, Manoa		Tel = (808)956-2920	
Instrument Development Lab (IDL)		Fax = (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created = ?{Created}		Size = 5x7	
Modified = ?{Date}		Rev = A 5	
Info = ?{Info}			
Designer = ?{Author}			
Module = ?{Cell}		Page = {Page}	
Path = ?{Design}			





PadGnd

Page 203
PadGnd

T: SPW = '297*1'
L = '4*1'

BONDING
PAD
p.301

Pad

Include models

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P 4 / N 4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter B=(W*L)*2*1 (l)
P: parameter (um).

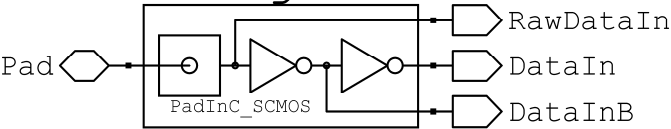
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.

Page 203

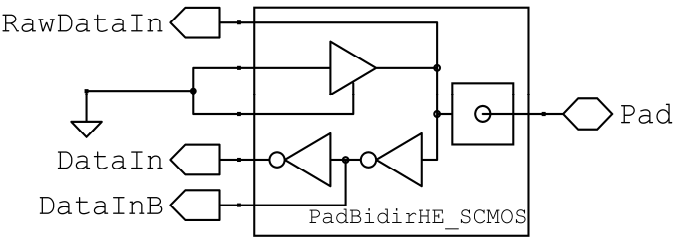
University of Hawai'i, Manoa		Tel = (808)956-2920	
Instrument Development Lab (IDL)		Fax = (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created = ?(Created)		Size = 5x7	
Modified = ?(Date)		Rev = A	
Info = ?(Info)			
Designer = ?(Author)			
Module = ?(Cell)		Page = {Page}	
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PadInC

Page 202



Page 210



Page 202

Include models

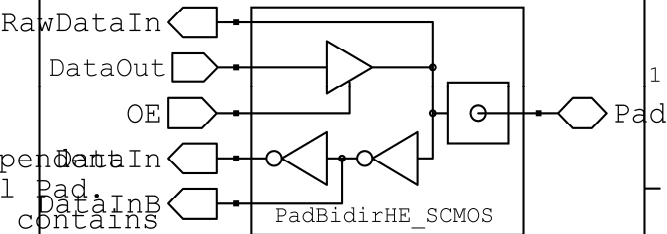
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.

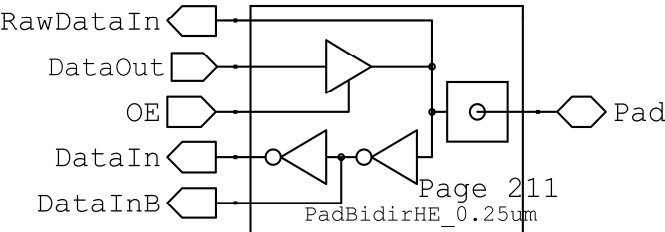
University of Hawai'i, Manoa		Tel = (808)956-2920	
Instrument Development Lab (IDL)		Fax = (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created = ?{Created}		Size = 5x7	
Modified = ?{Date}		Rev = A	
Info = ?{Info}			
Designer = ?{Author}			
Module = ?{Cell}		Page = {Page}	
Path = ?{Design}			

Bidirectional Pad

This module is the technology independent implementation of the Bidirectional Pad. It can be used for TPR, however it contains no information for exporting to Spice. In order to specify a technology for exporting to Spice, instance the appropriate PadBidirHE below.



Page 210

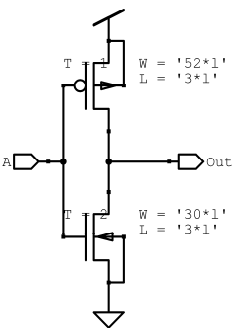
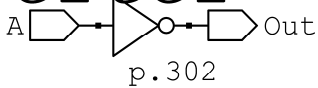


Page 210

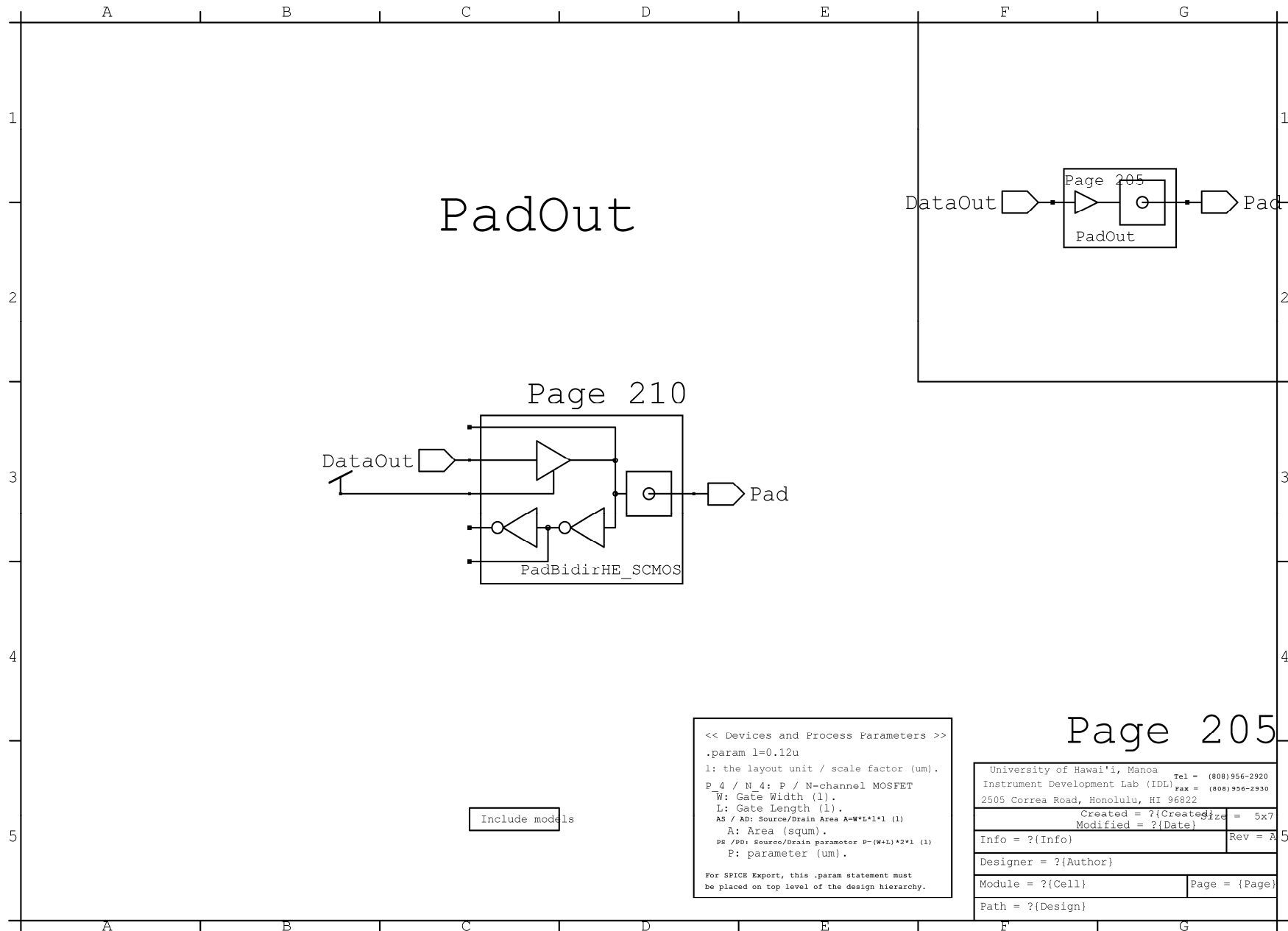
University of Hawai'i, Manoa		Tel = (808) 956-2920
Instrument Development Lab (IDL)		Fax = (808) 956-2930
2505 Correa Road, Honolulu, HI 96822		
Created = ?{Created}		Size = 5x7
Modified = ?{Date}		
Info = ?{Info}		Rev = A
Designer = ?{Author}		
Module = ?{Cell}		Page = {Page}
Path = ?{Design}		

Generic digital IO Inverter

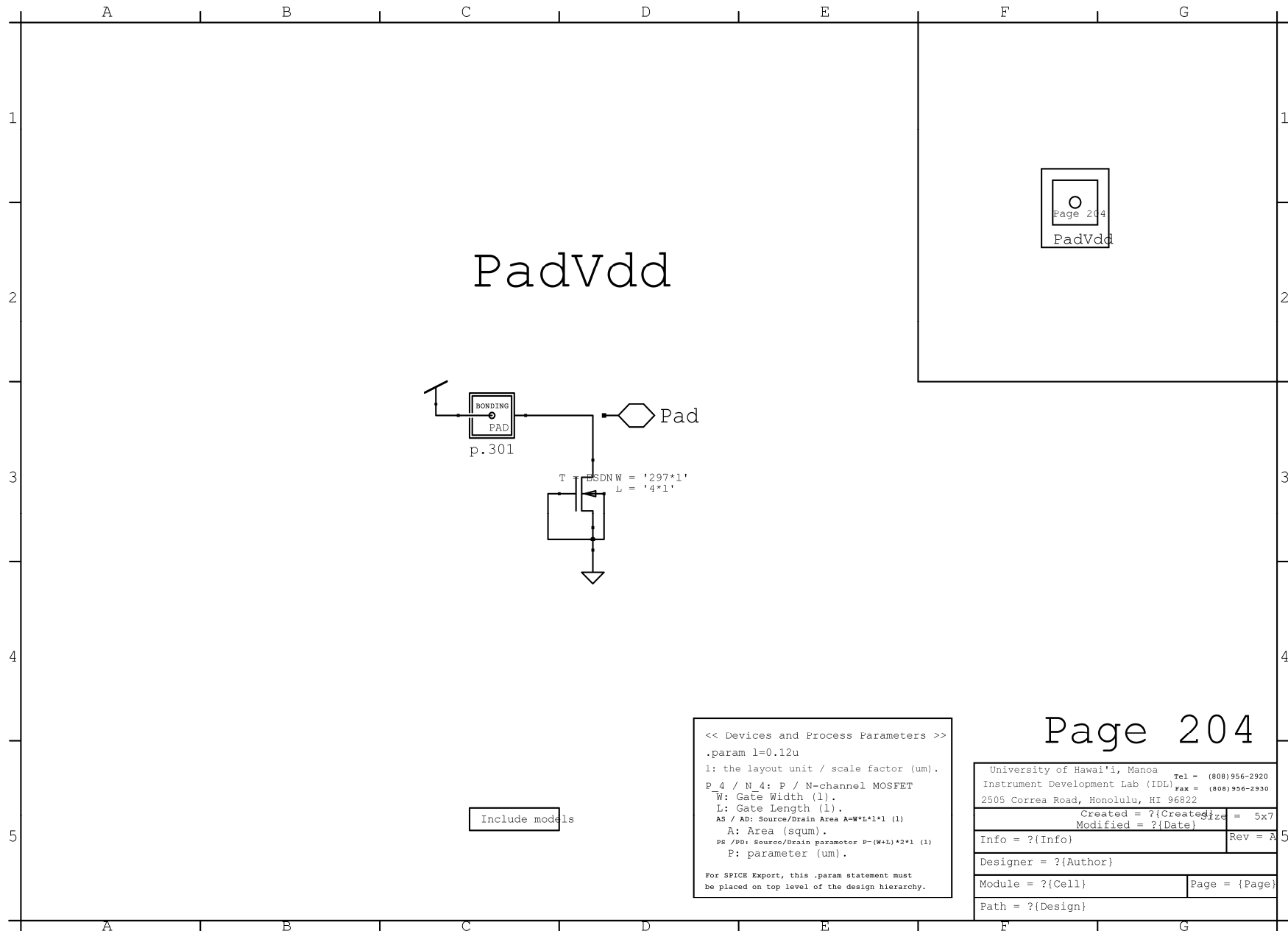
Inv



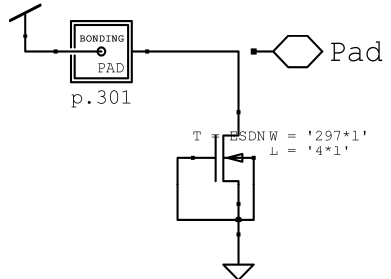
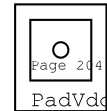
University of Hawai'i, Manoa		Tel = (808) 956-2920
Instrument Development Lab (IDL)		Fax = (808) 956-2930
2505 Correa Road, Honolulu, HI 96822		
Created = ?{Created}		Size = 5x7
Modified = ?{Date}		
Info = ?{Info}		Rev = A 5
Designer = ?{Author}		
Module = ?{Cell}		Page = {Page}
Path = ?{Design}		



<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P 4 / N 4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter B=(W*L)*2*1 (l)
P: parameter (um).
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.



PadVdd



Include models

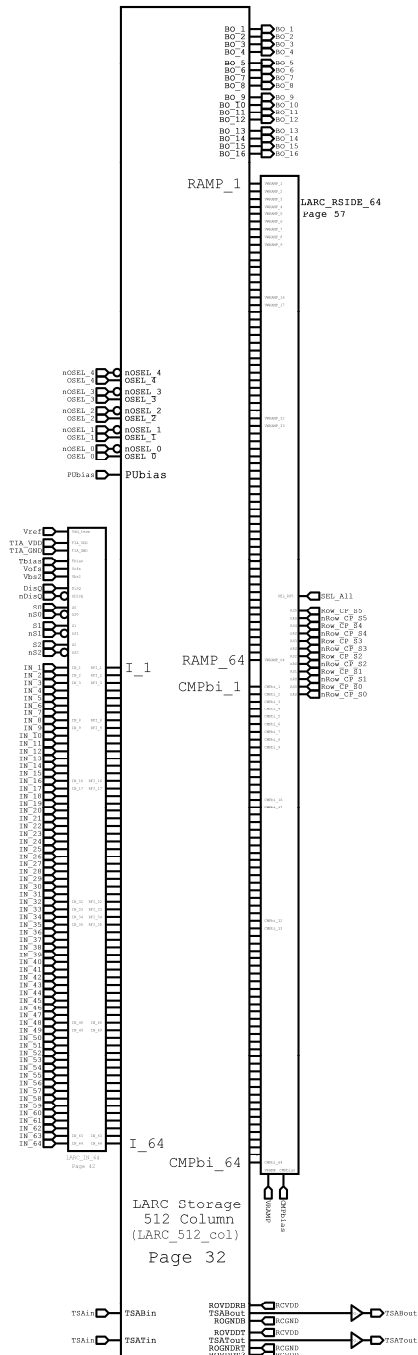
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P 4 / N 4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter B=(W*L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.

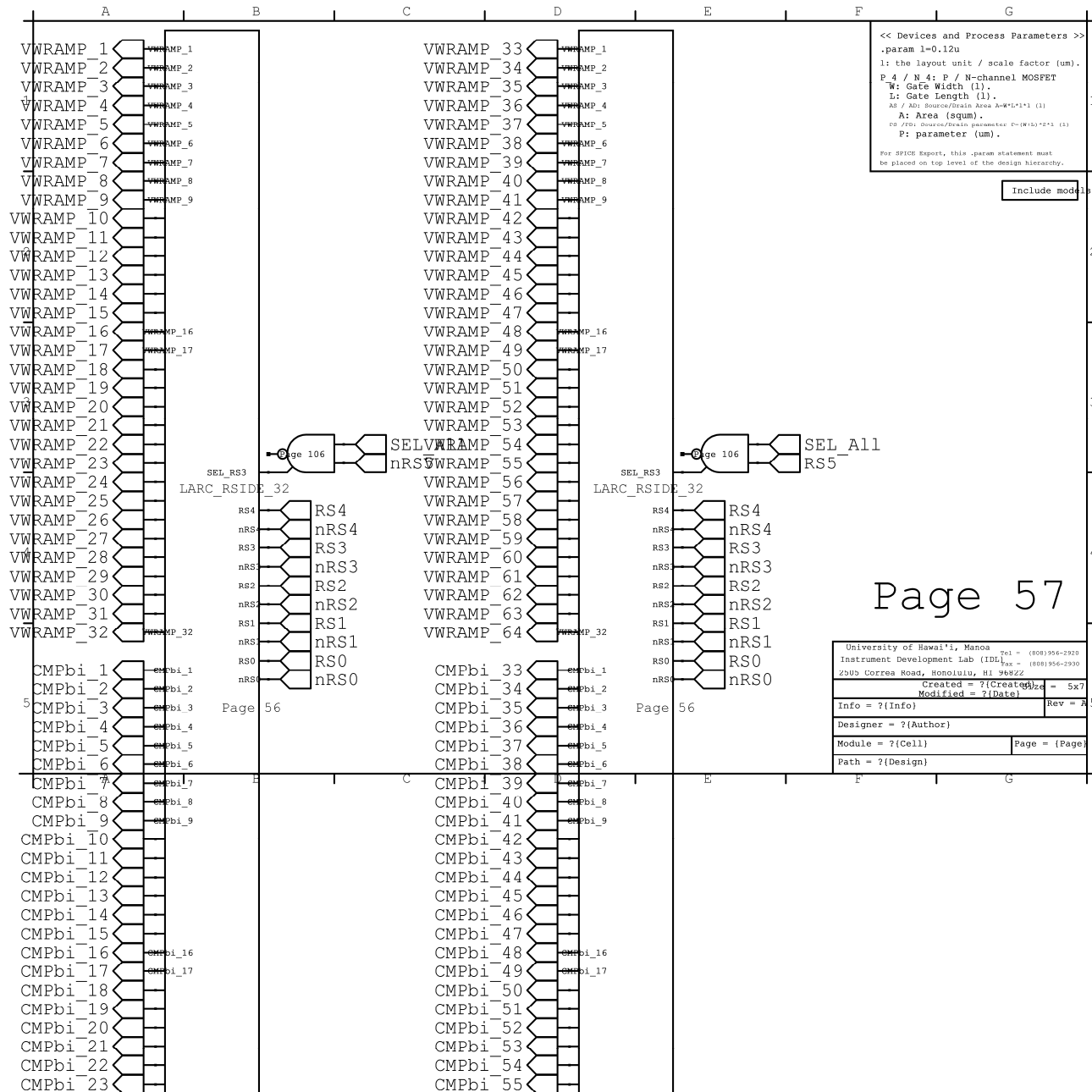
Page 204

University of Hawai'i, Manoa		Tel = (808)956-2920	
Instrument Development Lab (IDL)		Fax = (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created = ?(Created)		Size = 5x7	
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Info = ?(Info)			
Designer = ?(Author)			
Module = ?(Cell)		Page = {Page}	
Path = ?(Design)			

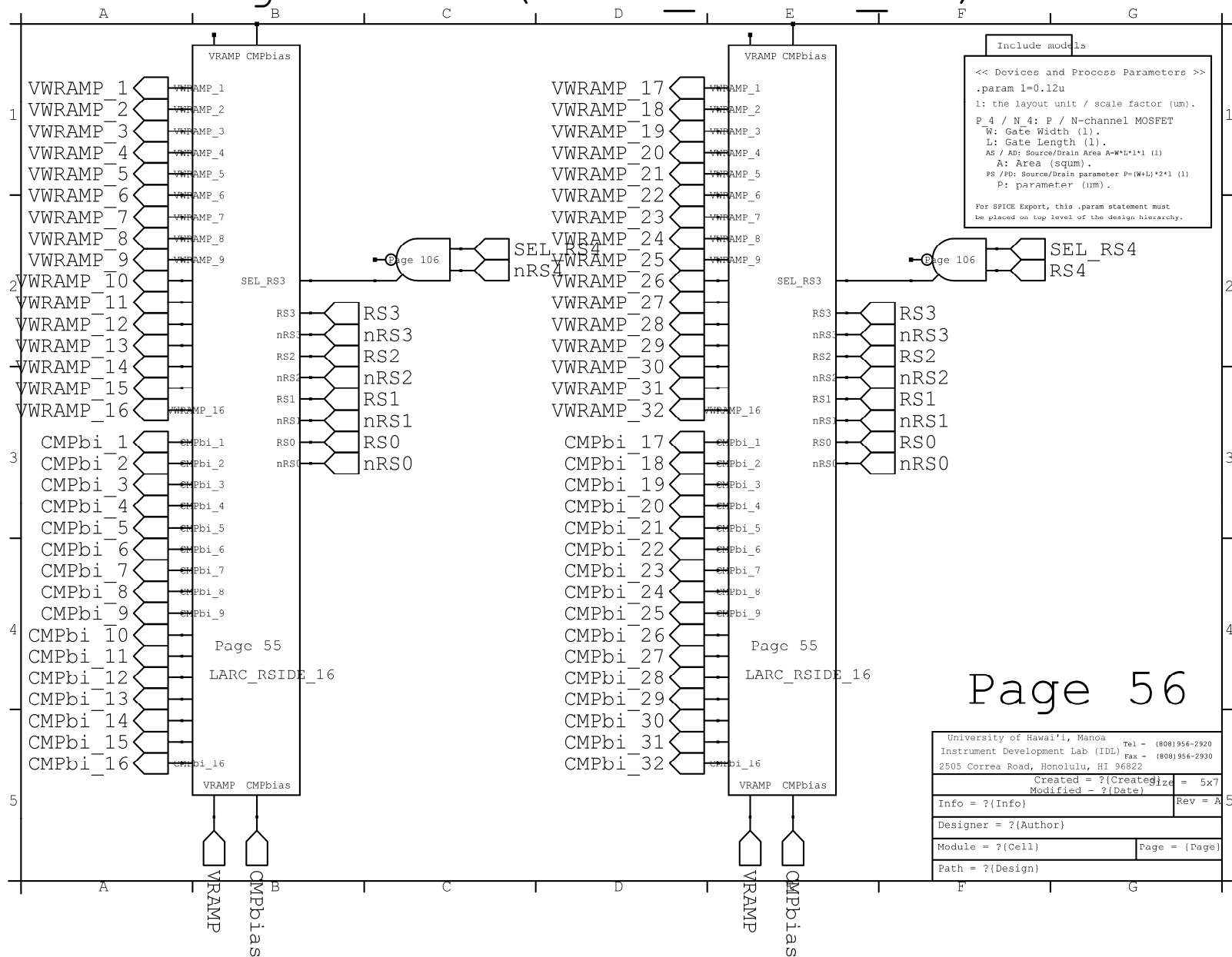
Page 3



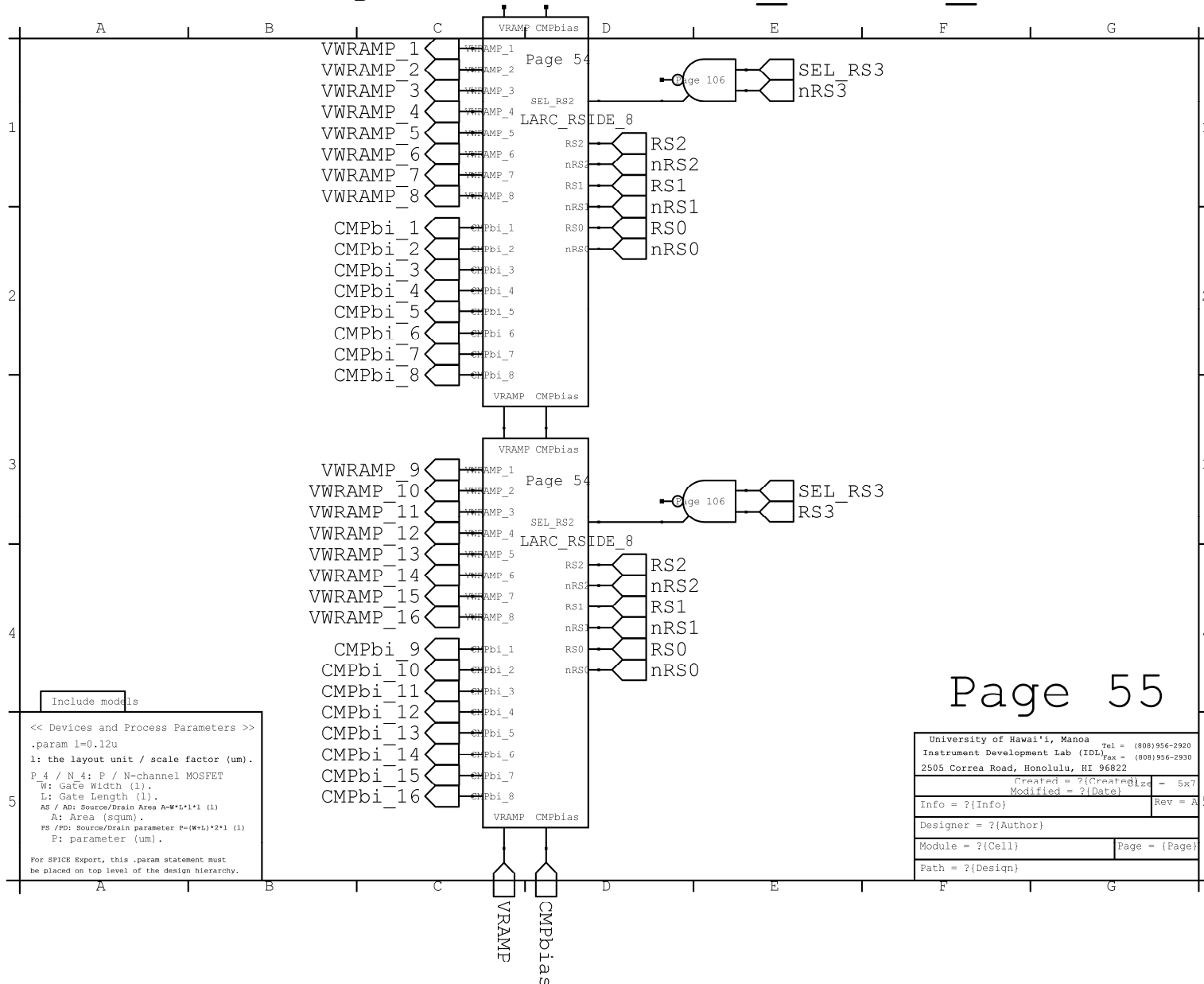
LARC RightSide (LARC RSIDE 64)



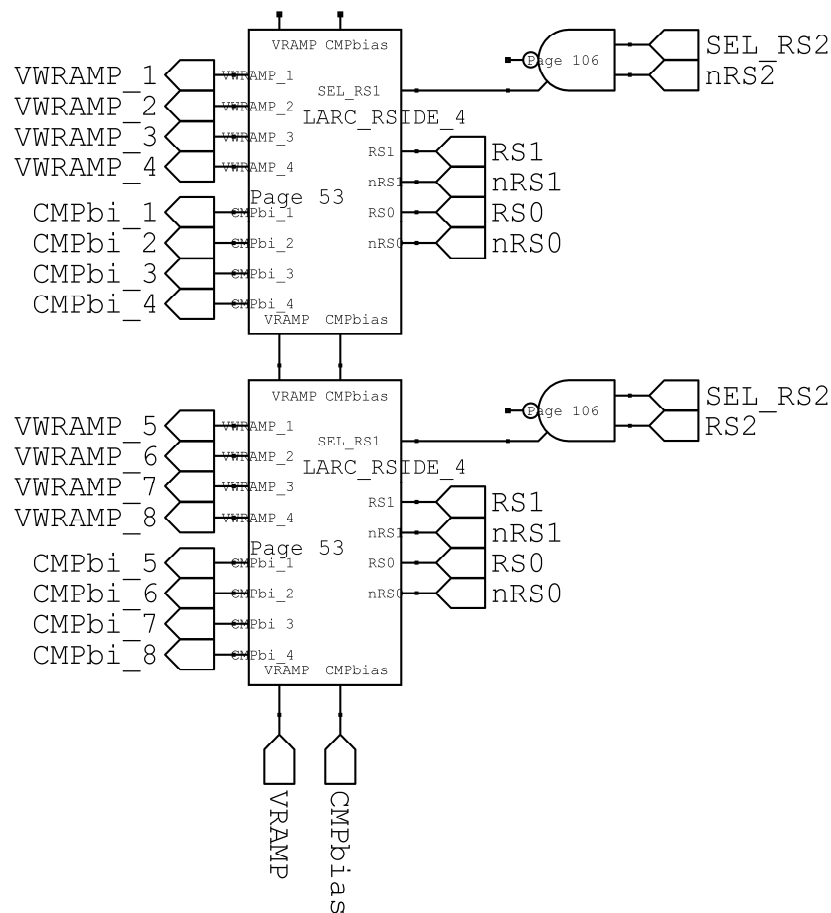
LARC RightSide (LARC RSIDE 32)



LARC RightSide (LARC_RSIDE_16)



LARC RightSide (LARC_RSIDE_8)



Page 54

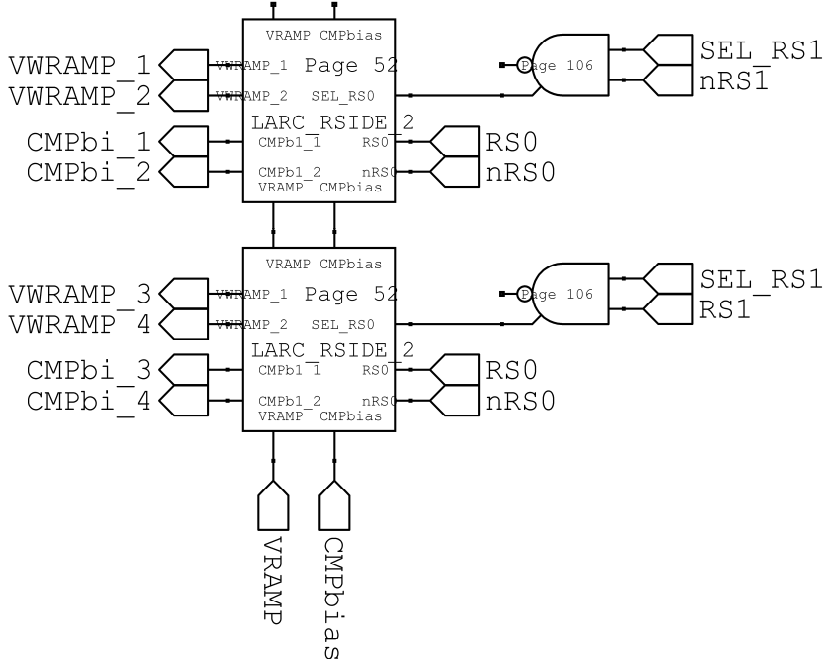
```
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A-W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).
```

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

Include models

University of Hawai'i, Manoa		Tel = (808)956-2920	
Instrument Development Lab (IDL)		Fax = (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created = ?{Created}		Size = 5x7	
Modified = ?{Date}		Rev = A	
Info = ?{Info}			
Designer = ?{Author}			
Module = ?{Cell}		Page = {Page}	
Path = ?{Design}			

LARC RightSide (LARC RSIDE 4)



```
<< Devices and Process Parameters >
.param l=0.12u
l: the layout unit / scale factor (um).

P 4 / N 4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A-W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
p: parameter (um).
```

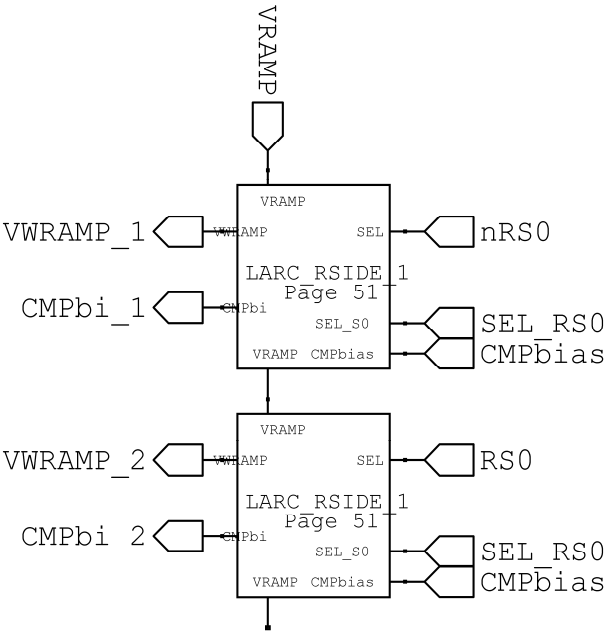
For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

Include models:

Page 53

University of Hawai'i, Manoa		Tel = (808) 956-2920	
Instrument Development Lab (IDL)		Fax = (808) 956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created = ?{Created}		Size = 5x7	
Modified = ?{Date}			
Info = ?{Info}			Rev = A
Designer = ?{Author}			
Module = ?{Cell}		Page = {Page}	
Path = ?{Design}			

LARC Rightside (LARC_RSIDE_2)



Page 52

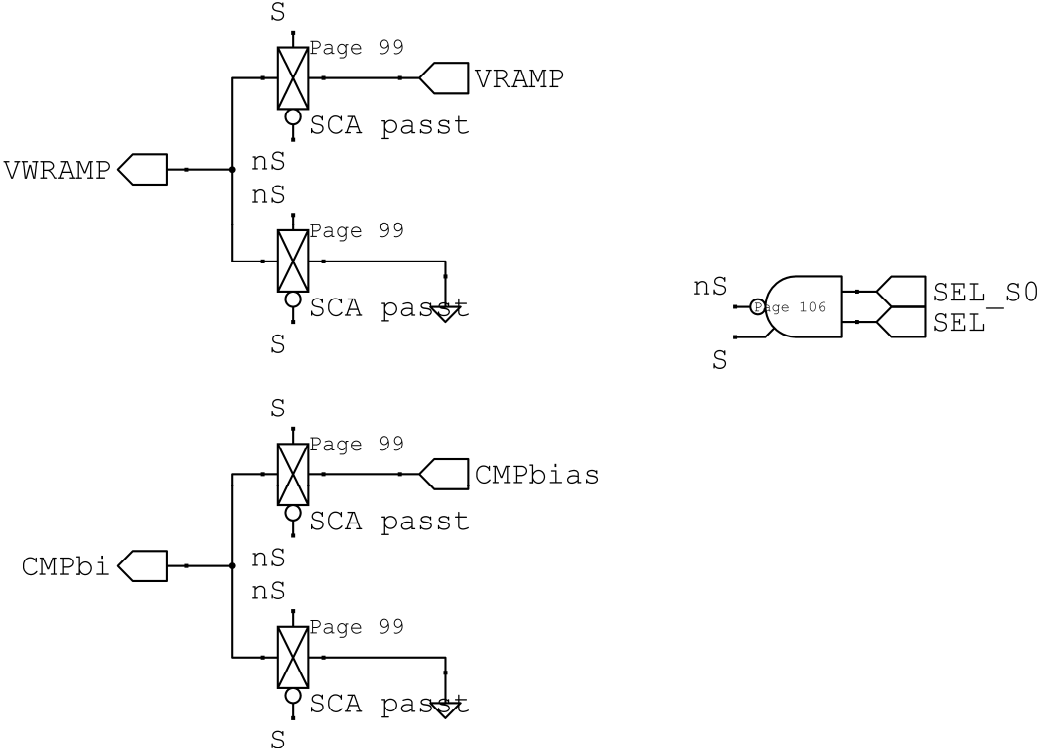
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A-W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

Include models

University of Hawai'i, Manoa		Tel = (808)956-2920	
Instrument Development Lab (IDL)		Fax = (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created = ?(Created)		Size = 5x7	
Modified = ?(Date)		Rev = A	
Info = ?(Info)			
Designer = ?(Author)			
Module = ?(Cell)		Page = {Page}	
Path = ?(Design)			

LARC RightSide Select (LARC RSIDE 1)



Page 51

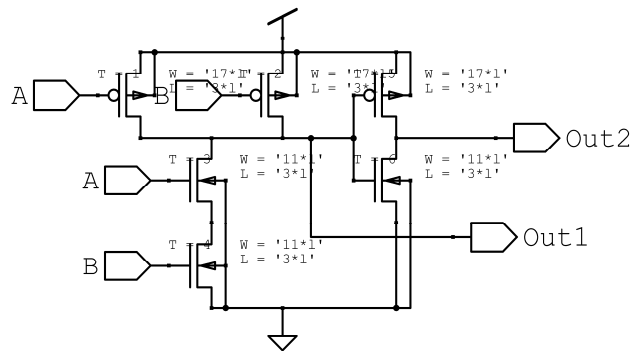
```
<< Devices and Process Parameters >
.param l=0.12u
l: the layout unit / scale factor (um).
P 4 / N 4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain perimeter P=(W+L)*2*1 (l)
P: parameter (um).
```

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

Include models

University of Hawai'i, Manoa		Tel = (808) 956-2920	
Instrument Development Lab (IDL)		Fax = (808) 956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created = {Created}		Size = 5x7	
Modified = {Date}			
Info = {Info}		Rev = A	
Designer = {Author}			
Module = {Cell}		Page = {Page}	
Path = {Design}			

NAND2C



[NETTRAN OUTPUT=<# SCMOS_NAND2C %A %B %Out1 %Out2]

```
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P 4 / N 4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).

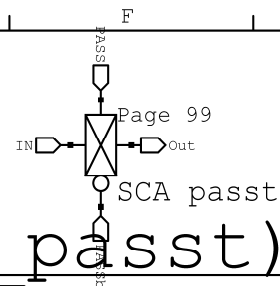
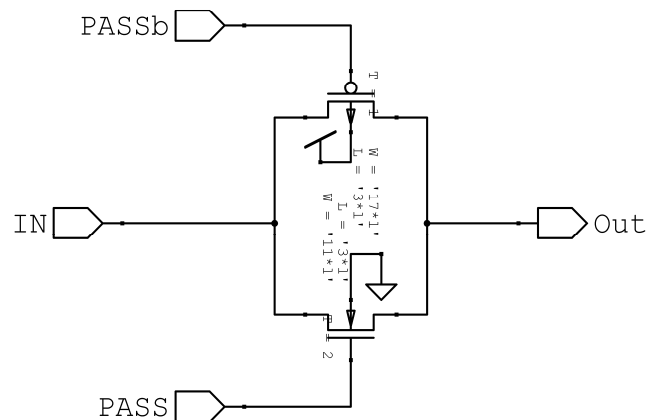
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
```

Page 106

University of Hawai'i, Manoa		Tel - (808)956-2920
Instrument Development Lab (IDL)		Fax - (808)956-2930
2505 Correa Road, Honolulu, HI 96822		
Created = ?(Created)		Size = 5x7
Modified = ?(Date)		Rev = A
Info = ?(Info)		
Designer = ?(Author)		
Module = ?(Cell)		Page = {Page}
Path = ?(Design)		

Include models

SCA Pass Transistor (big_passt)

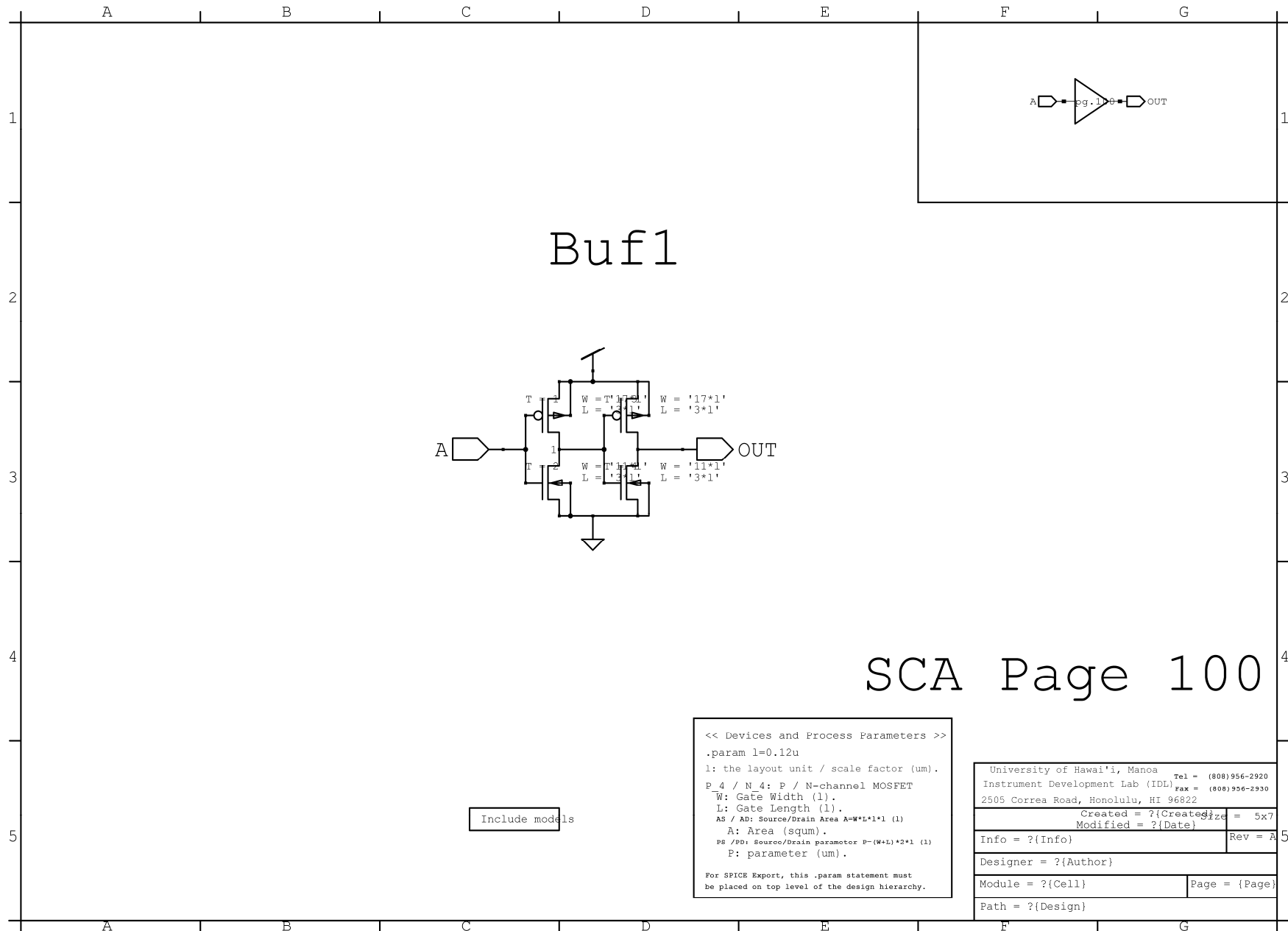


<< Devices and Process Parameters >>
.param l=0.3u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).

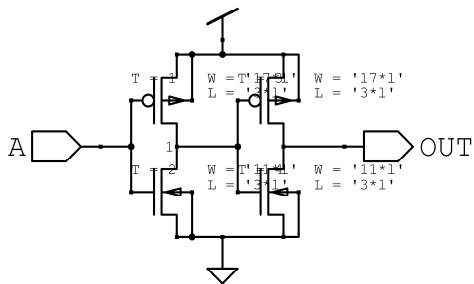
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.

Page 99

University of Hawai'i, Manoa		Tel = (808)956-2920
Instrument Development Lab (IDL)		Fax = (808)956-2930
2505 Correa Road, Honolulu, HI 96822		
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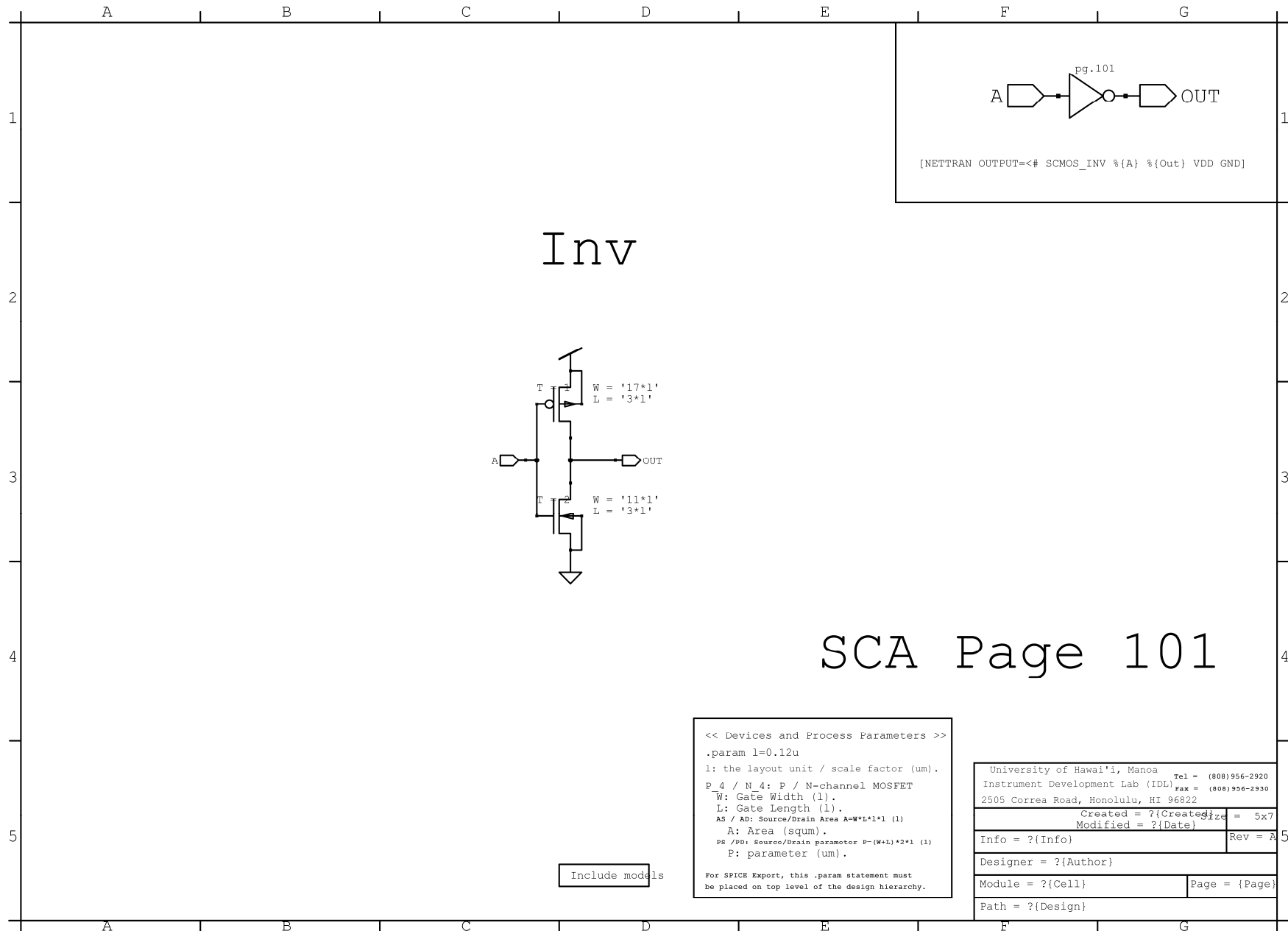


SCA Page 100

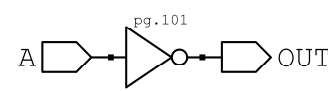
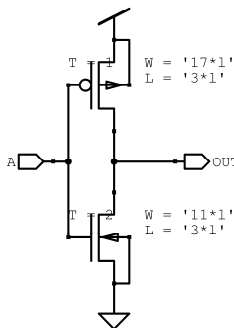
Include models

<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P 4 / N 4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter B=(W*L)*2*1 (l)
P: parameter (um).
For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.

University of Hawai'i, Manoa		Tel = (808)956-2920	
Instrument Development Lab (IDL)		Fax = (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
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Inv



[NETTRAN OUTPUT=<# SCMOS_INV %{A} %{Out} VDD GND]

SCA Page 101

<< Devices and Process Parameters >>
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l: the layout unit / scale factor (um).
P 4 / N 4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.

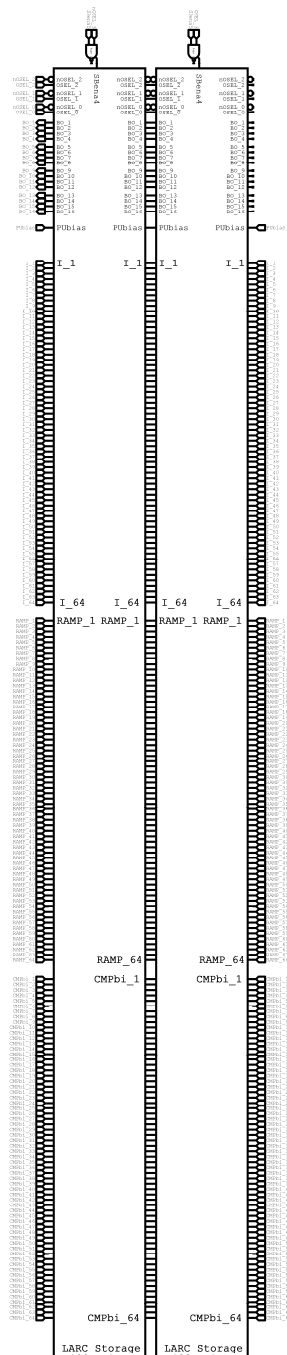
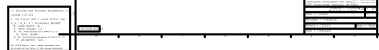
Include models

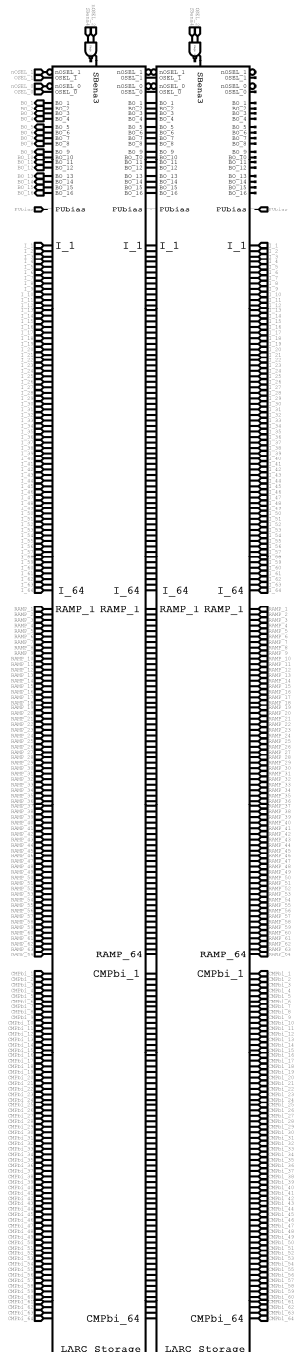
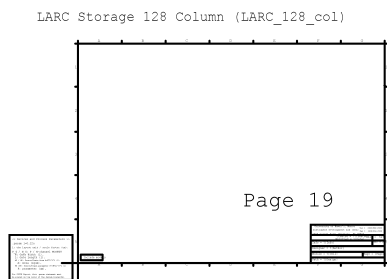
University of Hawai'i, Manoa		Tel = (808)956-2920	
Instrument Development Lab (IDL)		Fax = (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
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Info = ?{Info}			
Designer = ?{Author}			
Module = ?{Cell}		Page = {Page}	
Path = ?{Design}			

[illegible]

LARC Storage 256 Column (LARC_256_col)

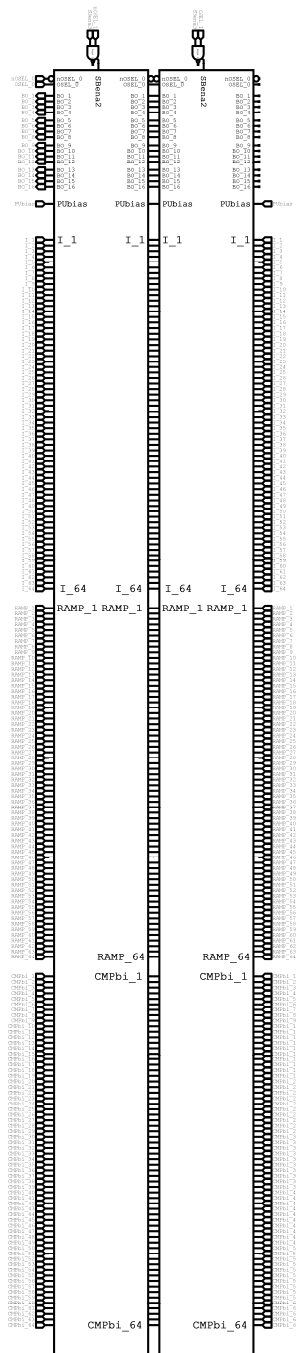
Page 31

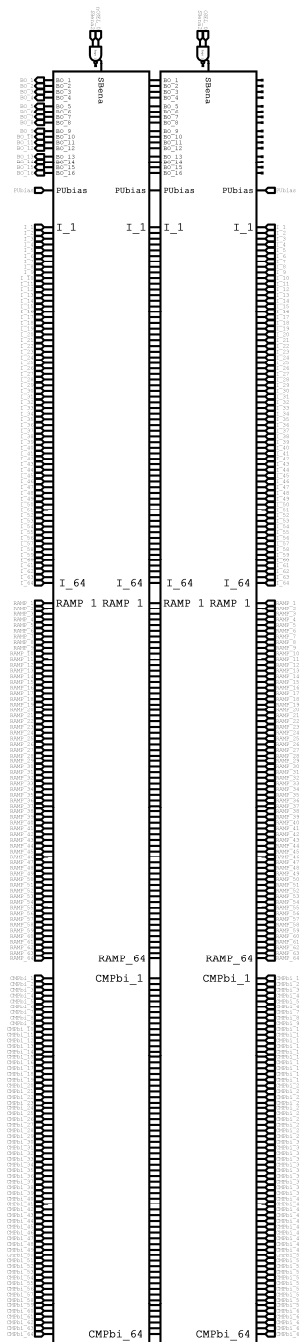




LARC Storage 64 Column (LARC_64_col)

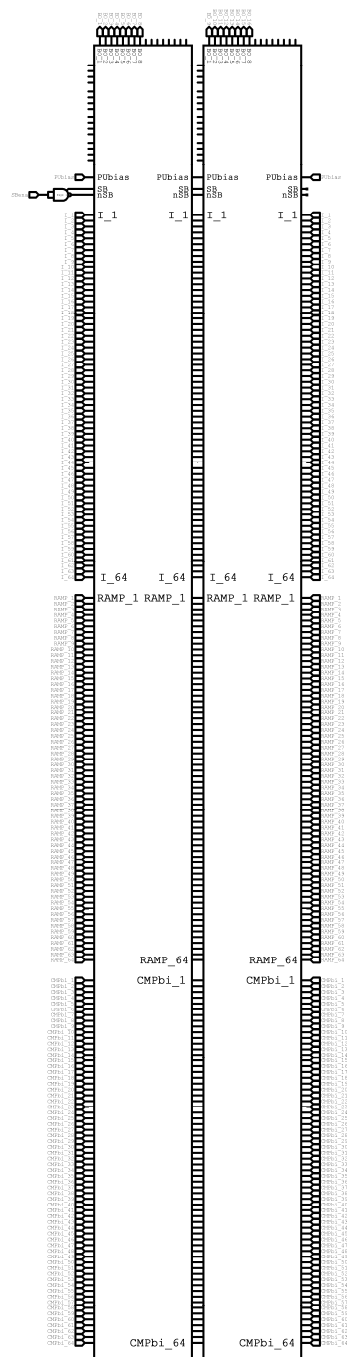
Page 18



[illegible]

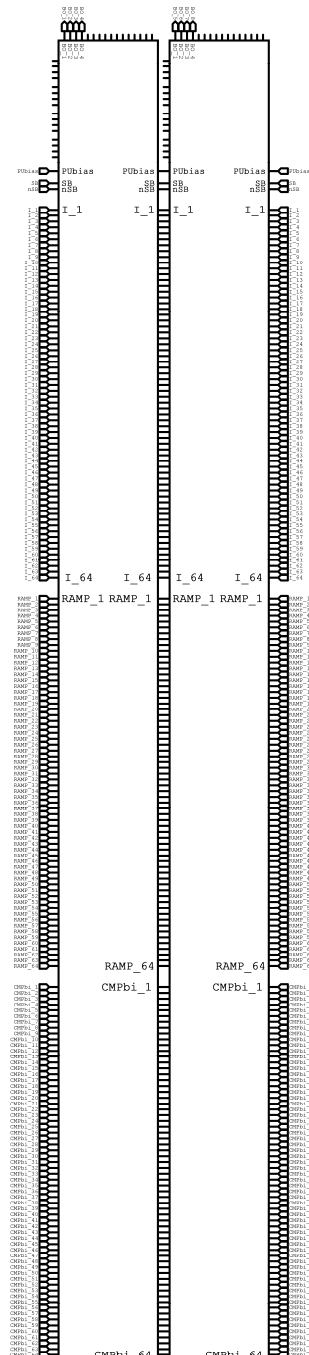
LARC Storage 16 Column (LARC_16_col)

Page 16

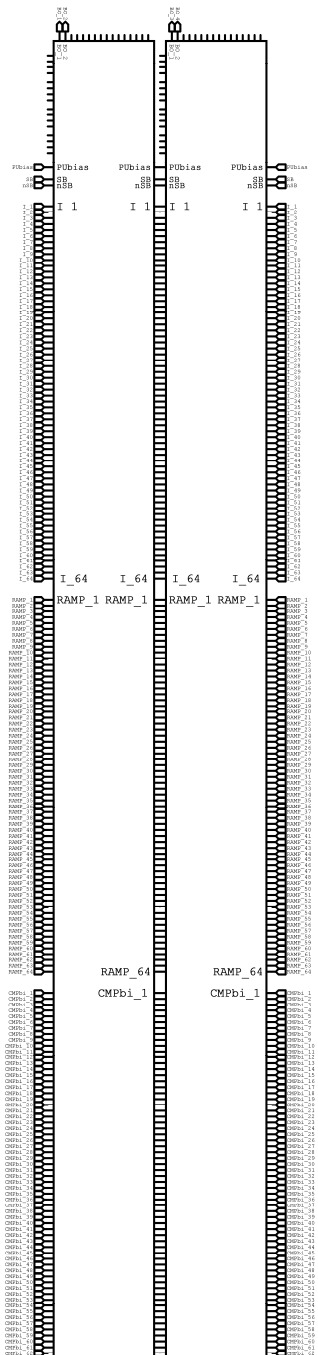
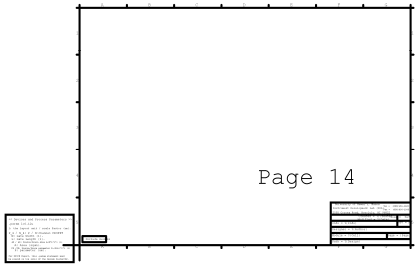


LARC Storage 8 Column (LARC_8_col)

Page 15



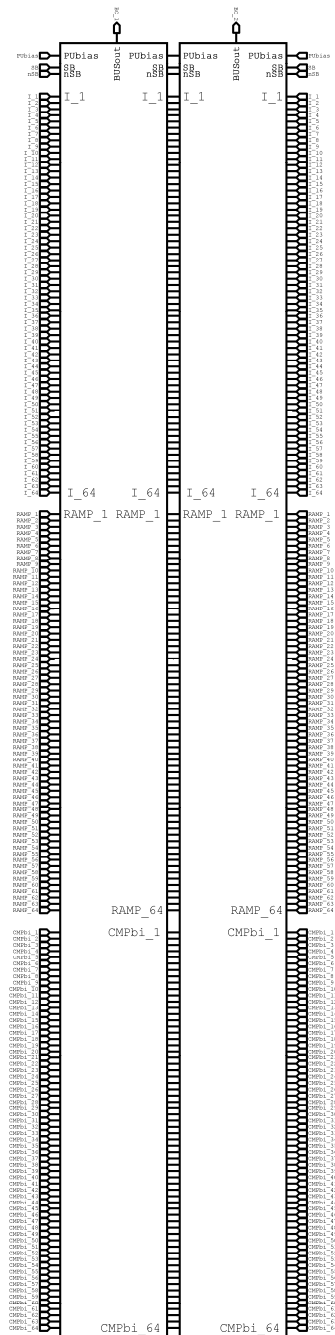
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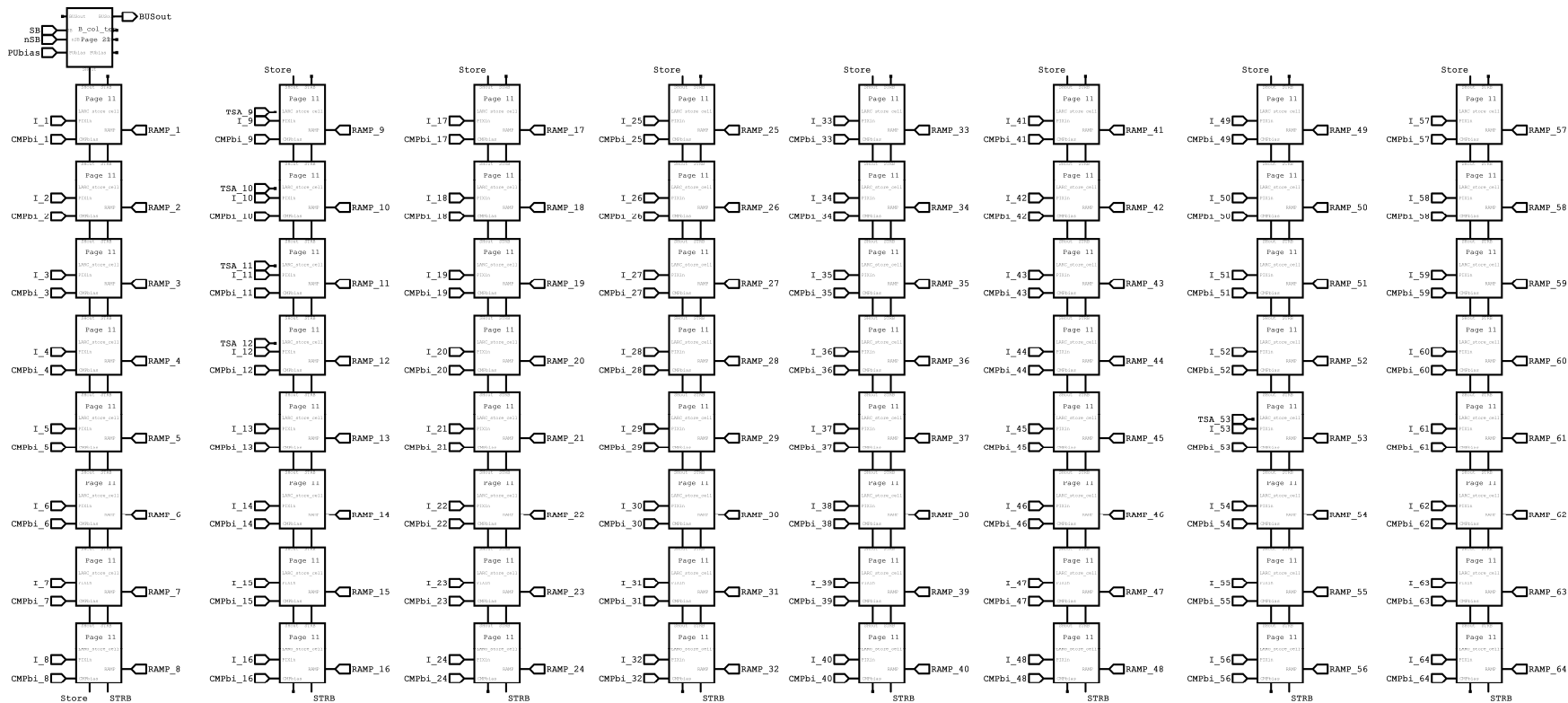


LARC Storage Double Column (LARC_2_col)

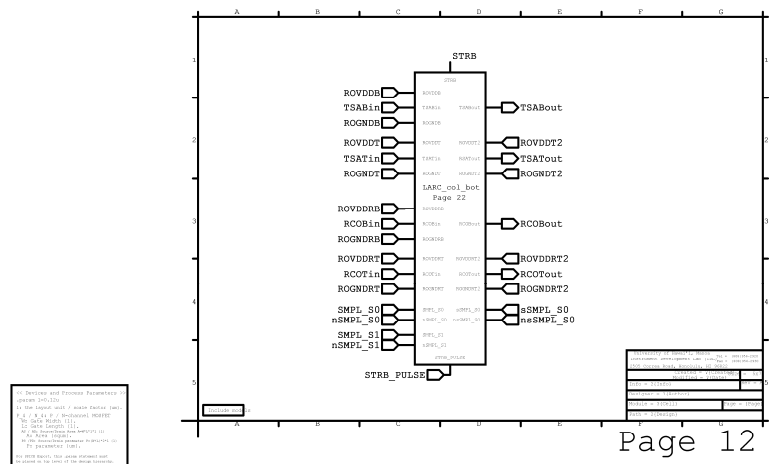
Page 13

1. LARC Storage Double Column (LARC_2_col)
2. LARC Storage Double Column (LARC_2_col)
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100. LARC Storage Double Column (LARC_2_col)

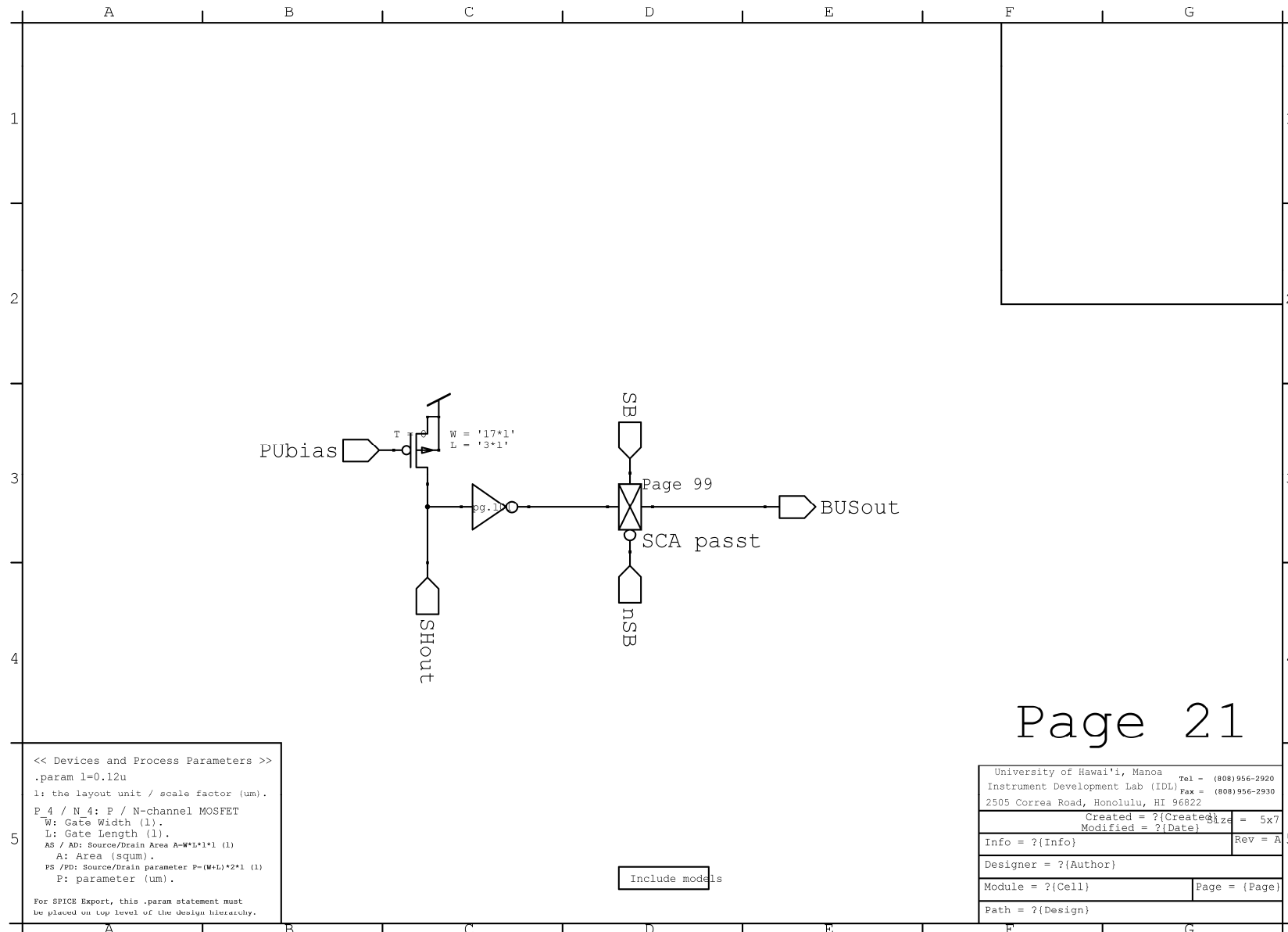




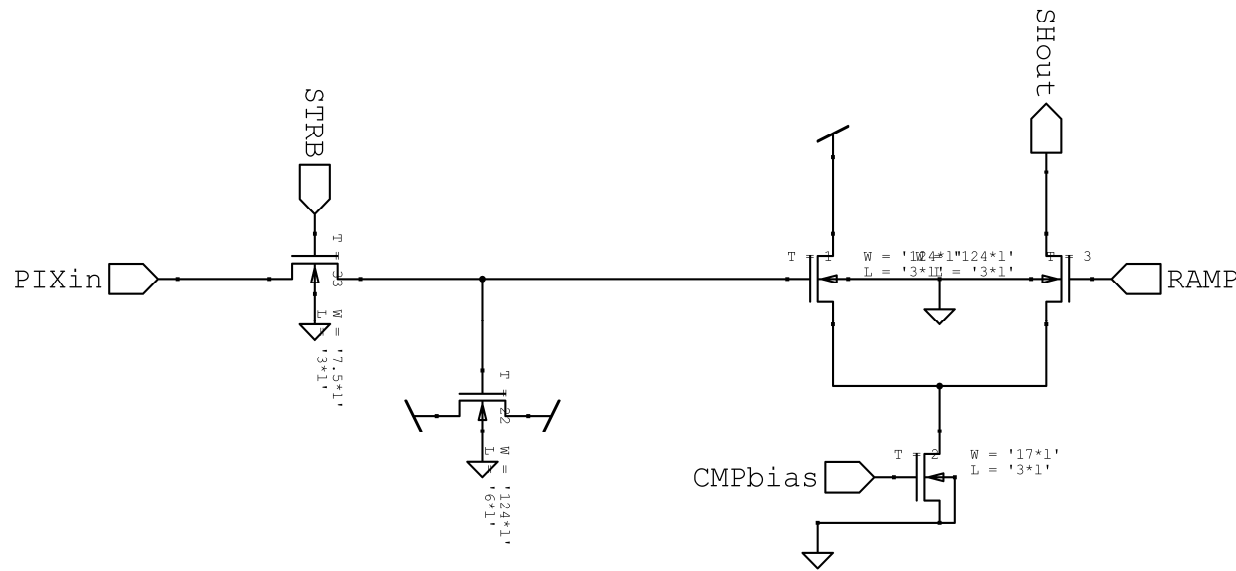
LARC Storage Single Column (LARC_single_col)



LARC Storage Column Top (LARC_col_top)



LARC Storage Cell (LARC_store_cell)



Capacitance = $18.88\mu\text{m} \times (0.72\mu\text{m} + 0.36\mu\text{m}) = \sim 90\text{fF}$

Page 11

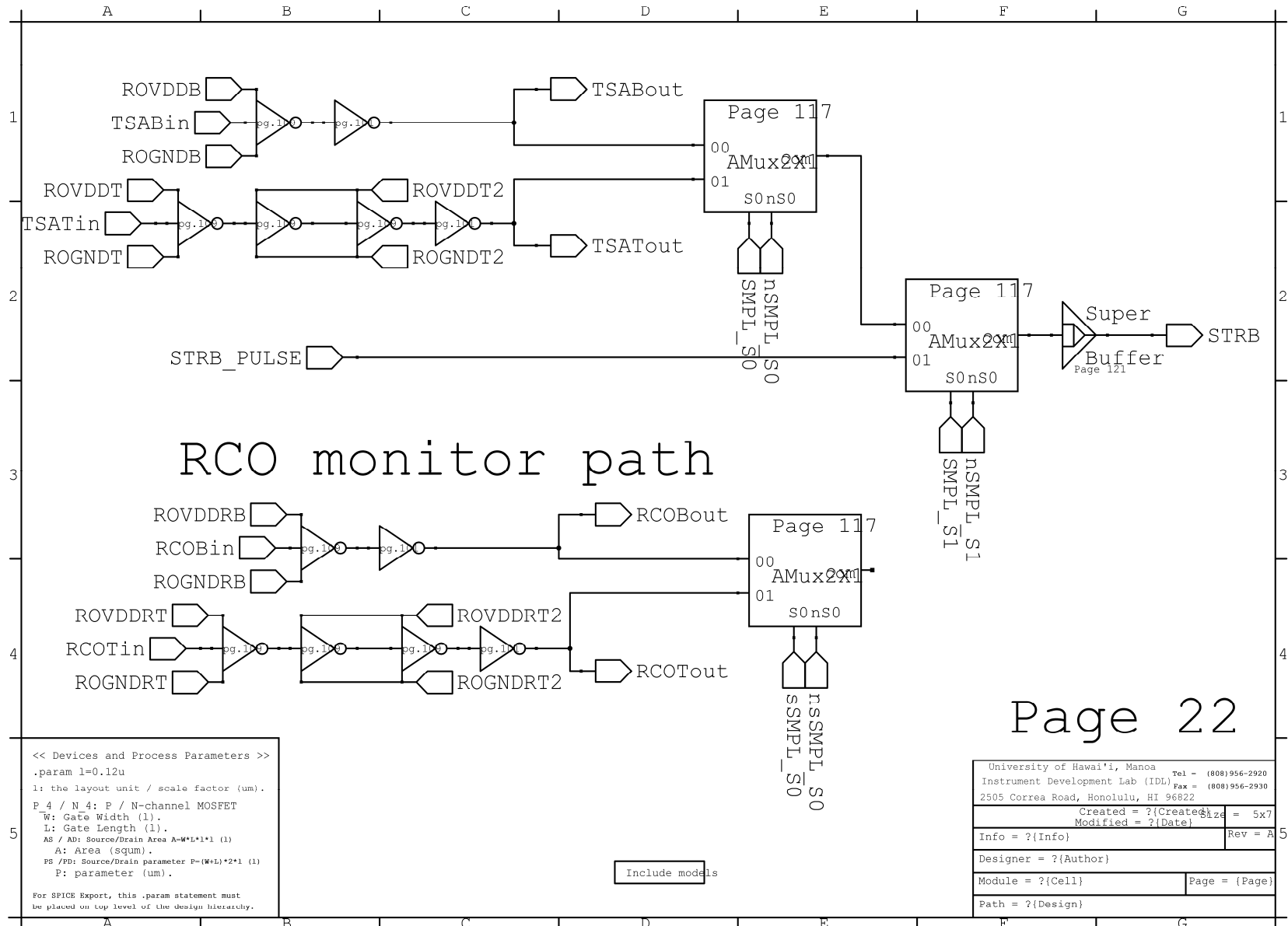
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.param l=0.12u
l: the layout unit / scale factor (um).
P 4 / N 4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).
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For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

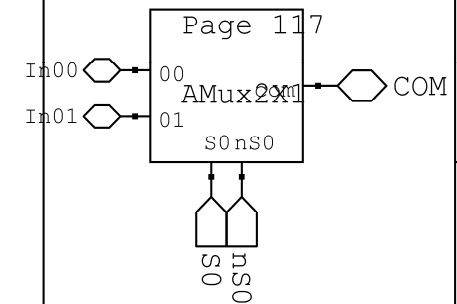
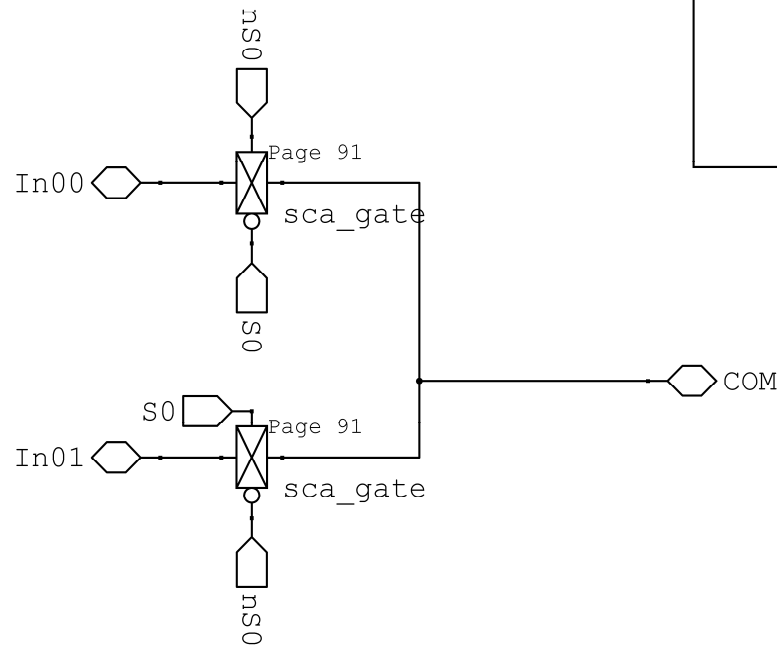
Include models

University of Hawai'i, Manoa		Tel = (808) 956-2920	
Instrument Development Lab (IDL)		Fax = (808) 956-2930	
2505 Correa Road, Honolulu, HI 96822			
Created = ?{Created}		Size =	5x7
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LARC Column [timing] Bot (LARC_col_bot)



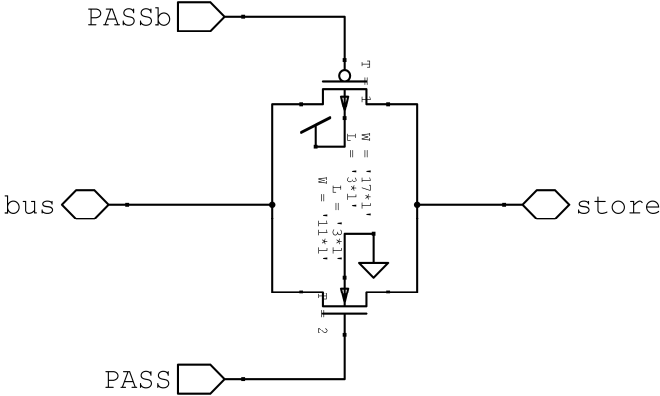
Analog 2x1 Mux (AMux2X1)



Page 117

University of Hawai'i, Manoa		Tel = (808) 956-2920
Instrument Development Lab (IDL)		Fax = (808) 956-2930
2505 Correa Road, Honolulu, HI 96822		
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SCA Pass Transistor (sca_gate)



Include models

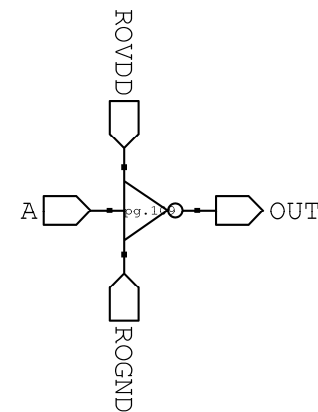
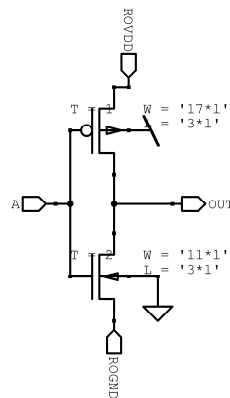
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l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.

SCA Page 91

University of Hawai'i, Manoa		Tel = (808) 956-2920
Instrument Development Lab (IDL)		Fax = (808) 956-2930
2505 Correa Road, Honolulu, HI 96822		
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Ring Oscillator Inverter (ring_osc_inv)



SCA Page 109

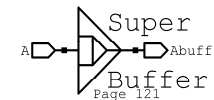
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 .param l=0.12u
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 P 4 / N 4: P / N-channel MOSFET
 W: Gate Width (l).
 L: Gate Length (l).
 AS / AD: Source/Drain Area A-W*L*1*1 (l)
 A: Area (squm).
 PS / PD: Source/Drain parameter P-(W*L)*2*1 (l)
 P: parameter (um).

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

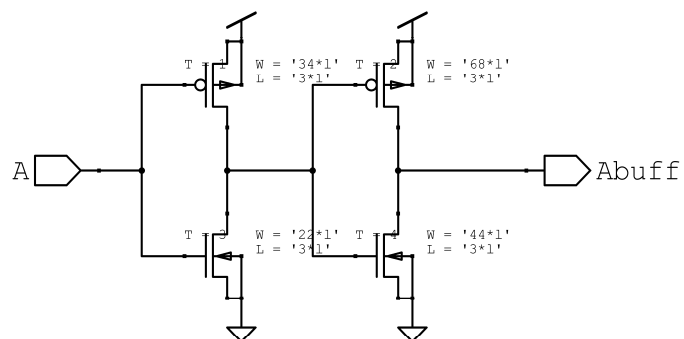
Include models

University of Hawai'i, Manoa		Tel = (808)956-2920	
Instrument Development Lab (IDL)		Fax = (808)956-2930	
2505 Correa Road, Honolulu, HI 96822			
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Designer = ?{Author}			
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Super Buffer (super_buff)



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<< Devices and Process Parameters >>
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 l: the layout unit / scale factor (um).
 P 4 / N 4: P / N-channel MOSFET
 W: Gate Width (l).
 L: Gate Length (l).
 AS / AD: Source/Drain Area A=W*L*1*1 (l)
 A: Area (squm).
 PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
 P: parameter (um).

For DTCB Export, this .param statement must be placed on top level of the design hierarchy.

Include models

Page 121

University of Hawai'i, Manoa		Tel = (808) 956-2920
Instrument Development Lab (IDL)		Fax = (808) 956-2930
2505 Correa Road, Honolulu, HI 96822		
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Info = ?(Info)		Rev = A
Designer = ?(Author)		
Module = ?(Cell)		Page = (Page)
Path = ?(Design)		

Simulation page is LARC_TIA_4

1pF Cap:

$6.134\text{fF}/\mu\text{m}^2$

$1\text{pF} = 163\mu\text{m}^2$

T2 size:

$L=171\text{ (}20.58\mu\text{m)}$

$W=66\text{ (}7.92\mu\text{m)}$

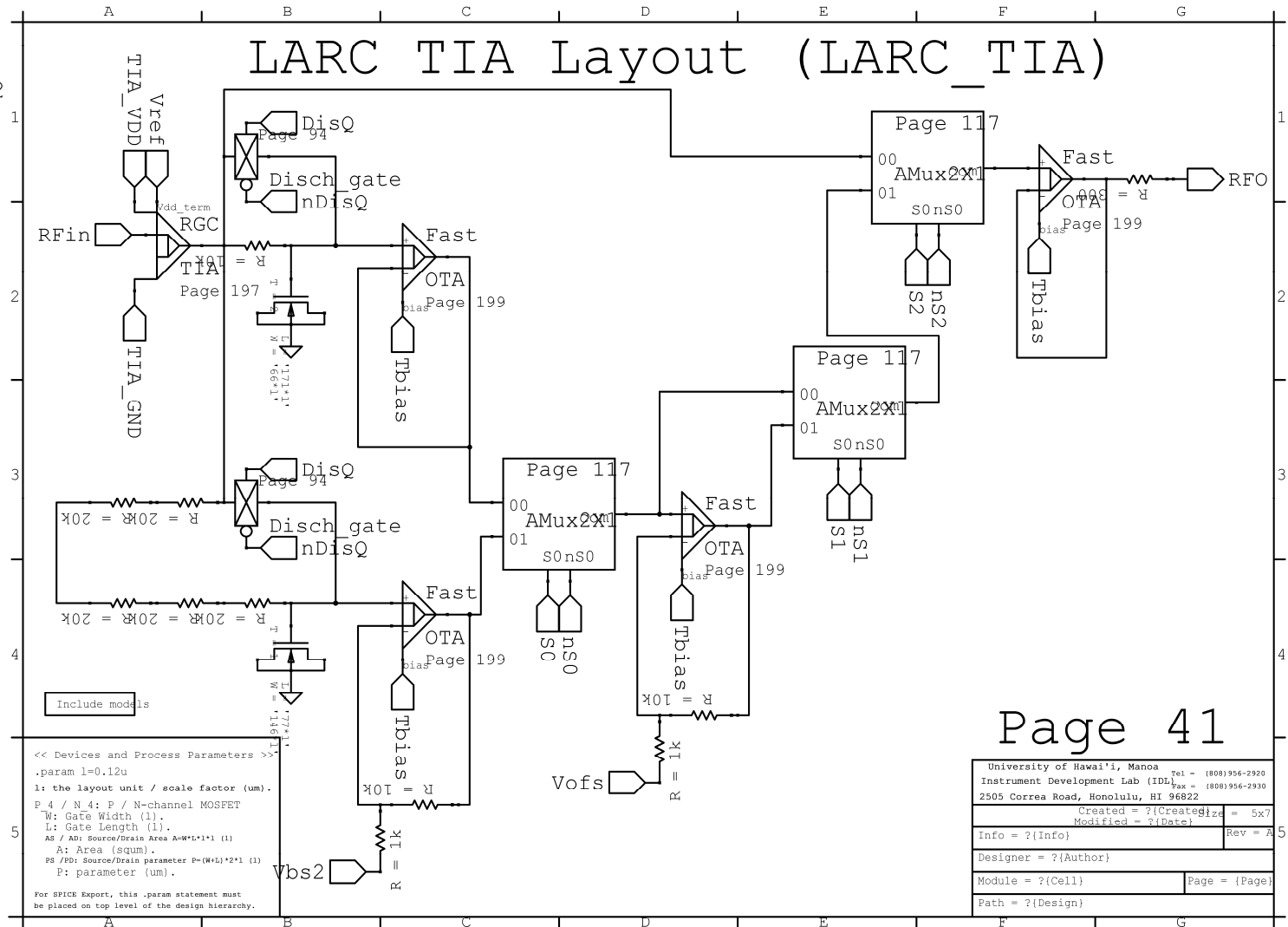
$163\mu\text{m}^2$

T1 size:

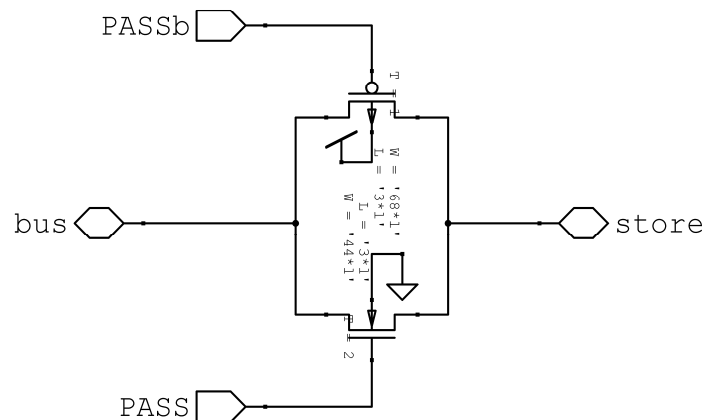
$L=77\text{ (}9.24\mu\text{m)}$

$W=146\text{ (}17.52\mu\text{m)}$

$161.9\mu\text{m}^2$



LARC Discharge Gate (Disch_gate)



Include models

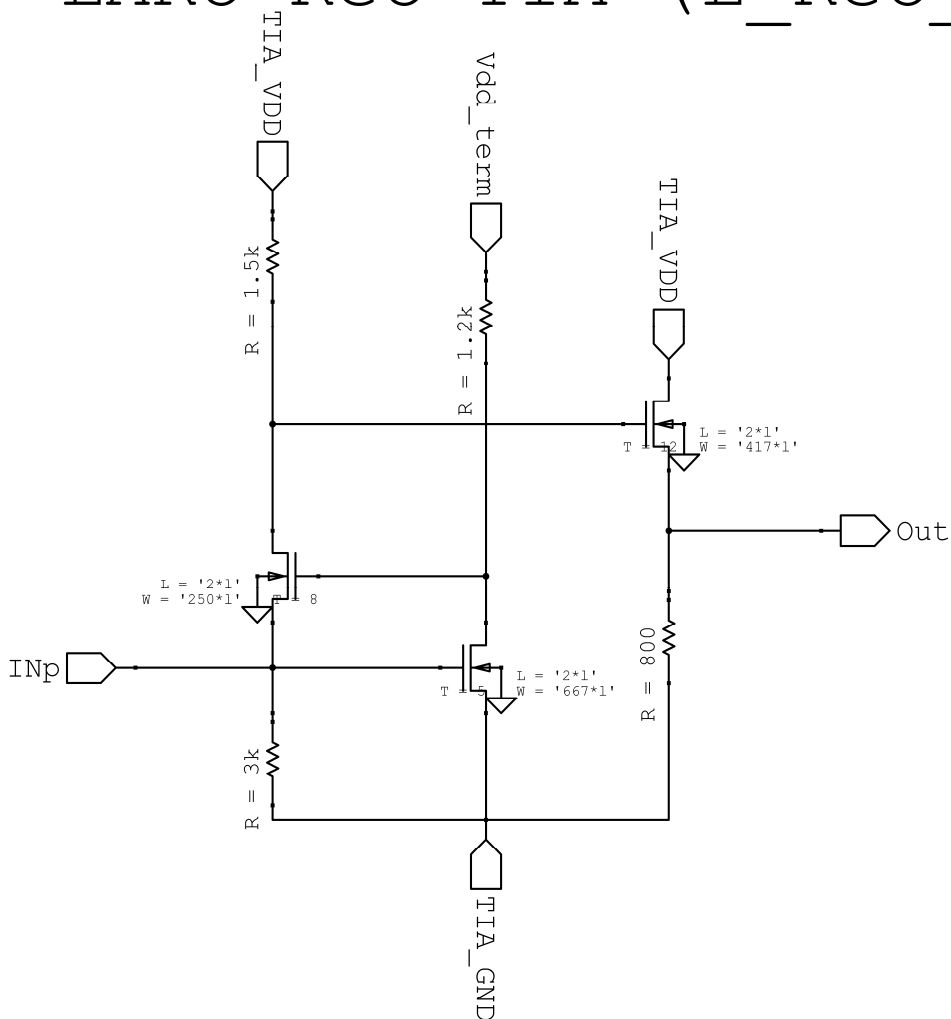
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<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P 4 / N 4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1 (l)
A: Area (squm).
PS / PD: Source/Drain parameter B=(W*L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
```

Page 94

University of Hawai'i, Manoa		Tel = (808)956-2920
Instrument Development Lab (IDL)		Fax = (808)956-2930
2505 Correa Road, Honolulu, HI 96822		
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Modified = ?(Date)		
Info = ?(Info)		Rev = A
Designer = ?(Author)		
Module = ?(Cell)		Page = {Page}
Path = ?(Design)		

LARC RGC TIA (L_RGC_TIA)



<< Devices and Process Parameters >>
 .param l=0.12u
 l: the layout unit / scale factor (um).
 P_4 / N_4: P / N-channel MOSFET
 W: Gate Width (l).
 L: Gate Length (l).
 AS / AD: Source/Drain Area A=W*L*1 (l)
 A: Area (squm).
 PS / PD: Source/Drain parameter P=(W*L)*2*1 (l)
 P: parameter (um).
 For SPICE Export, this .param statement must
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Include models

Page 197

University of Hawai'i, Manoa	
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2505 Correa Road, Honolulu, HI 96822	Fax = (808)956-2930
Created = ?(Created)	Size = 5x7
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