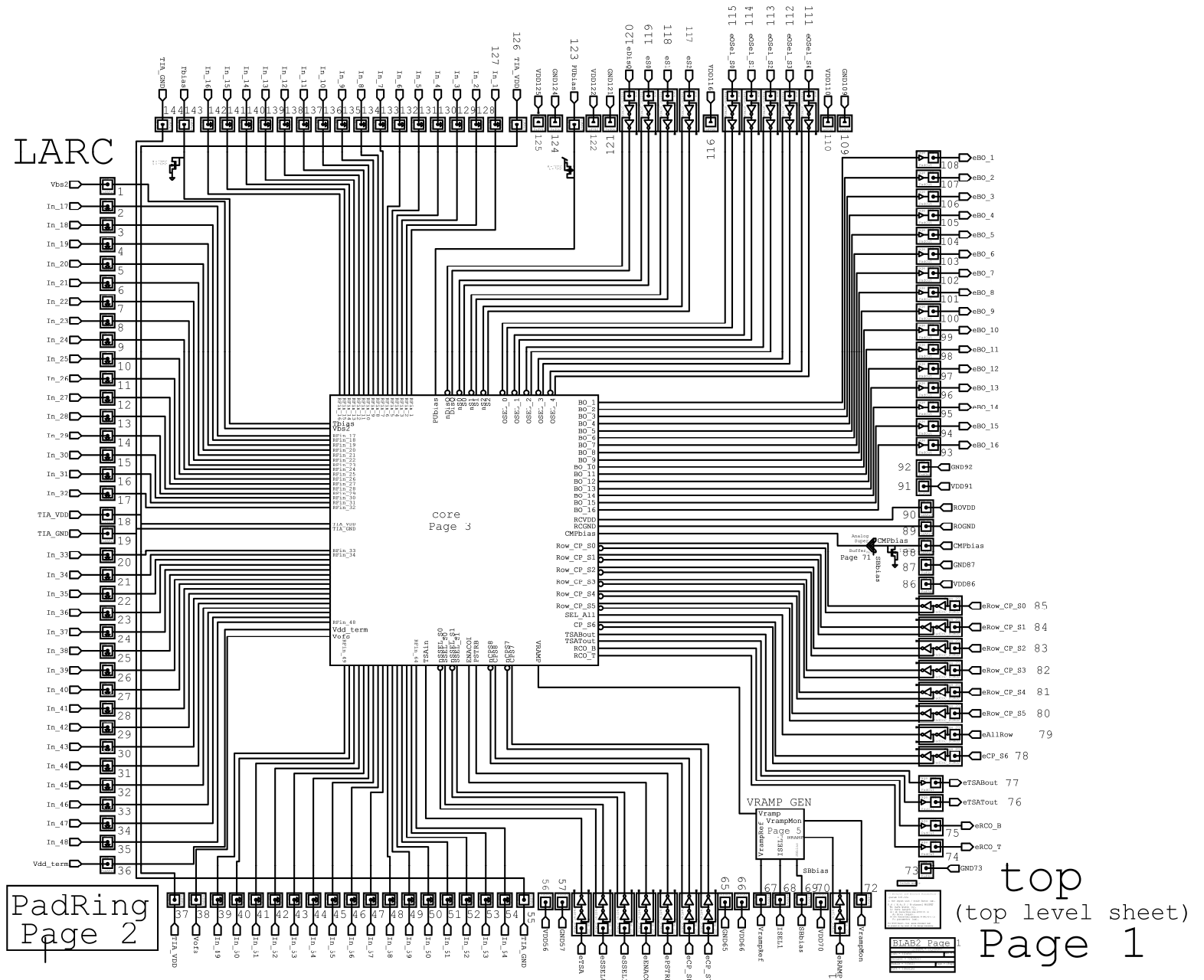
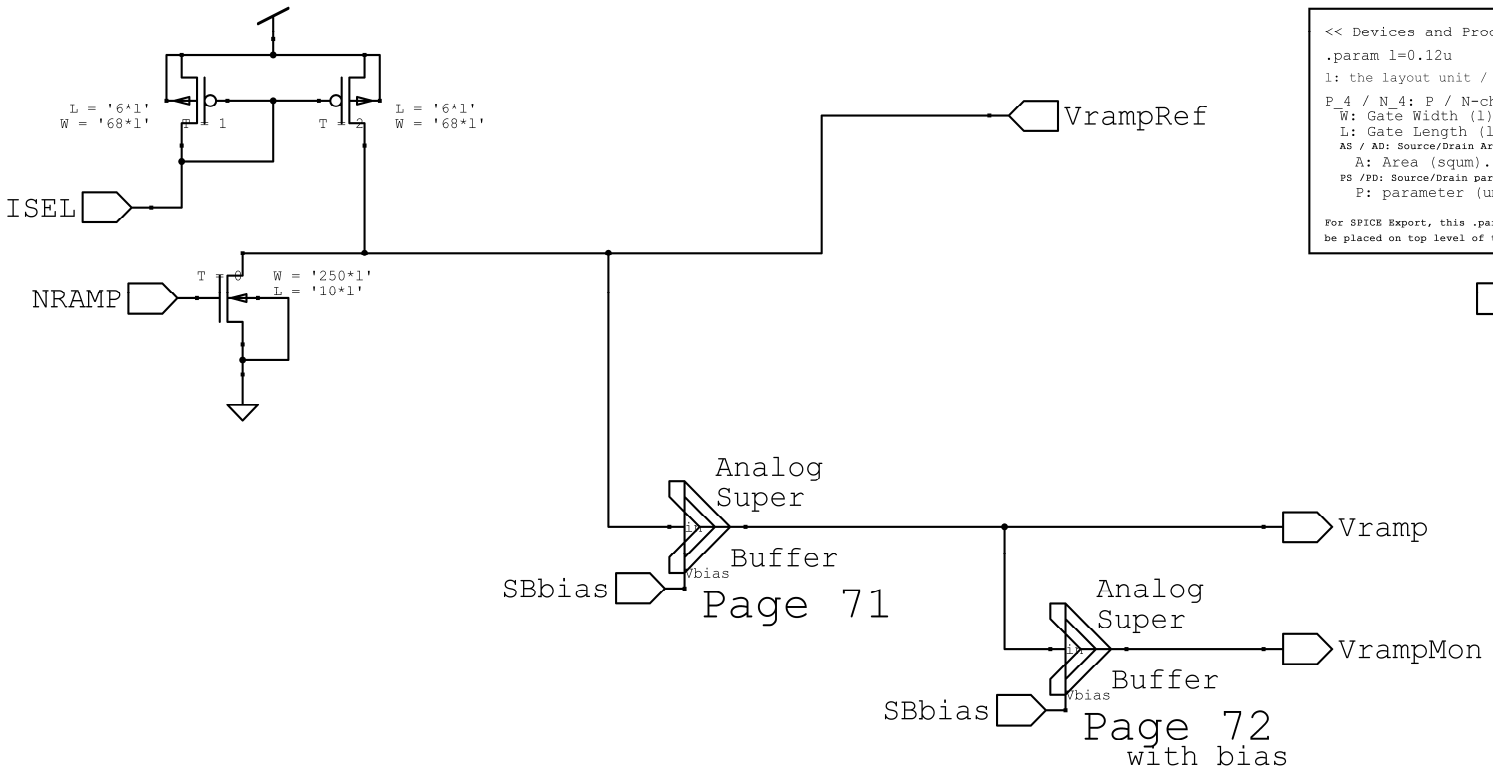

LARC
PadRing
Page 2
core
Page 3
VRAMP GEN
Vramp
VrampMon
Page 5
top
(top level sheet)
Page 1
BLAB2 Page 1

Voltage Ramp Generator (VRAMP_GEN)



<< Devices and Process Parameters >>

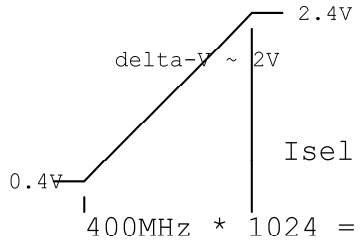
.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*l*l (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*l (l)
P: parameter (um).

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

Include models



~10pF for no load Cap, just input pad

Isel = (1/C)*(delta-Q/delta-T) ~ 10uA

Page 5

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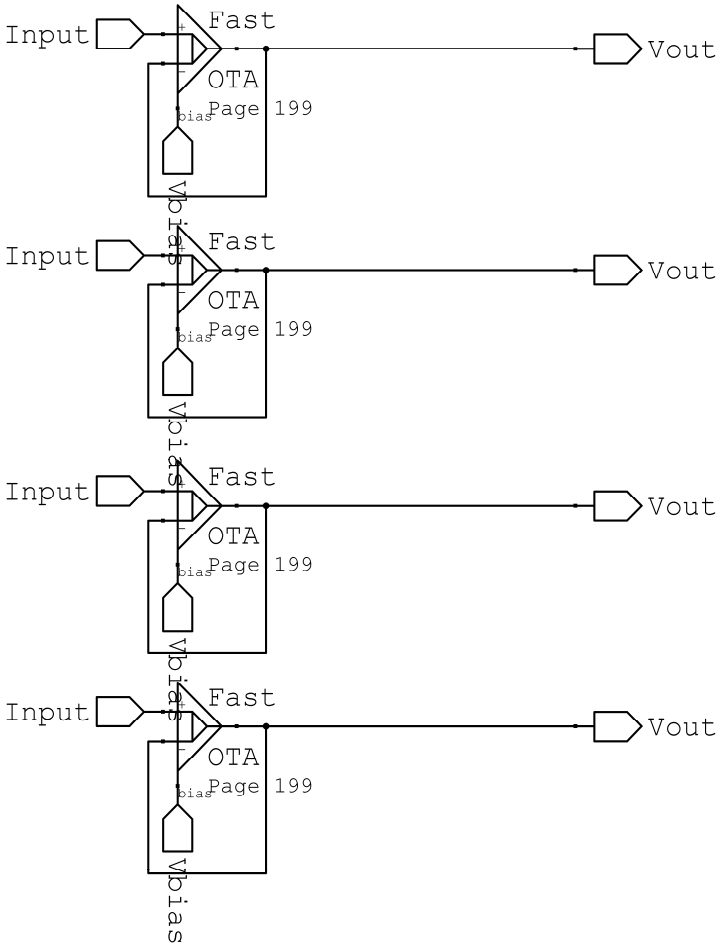
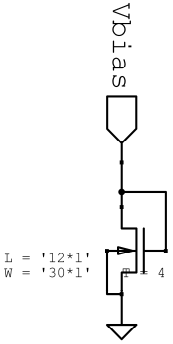
Analog Output Super Buffer (ao_superbuff_wbias)





<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*l*l (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*l (l)
P: parameter (um).

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

Include models

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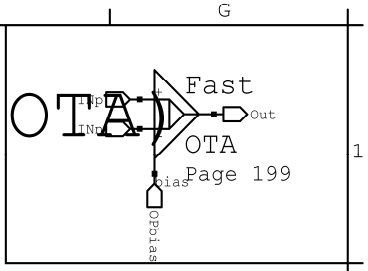
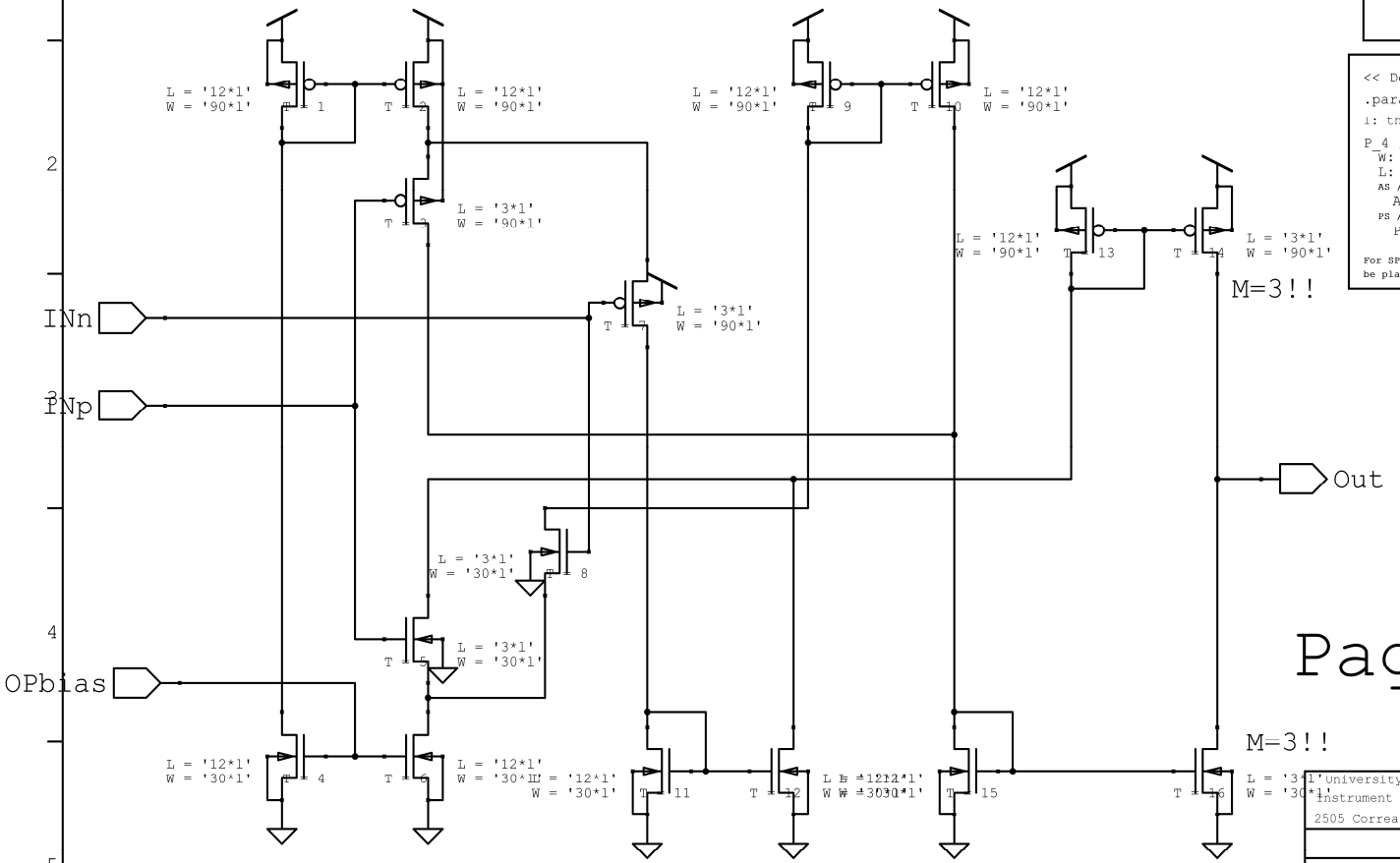
OTA for Fast performance (OTA)





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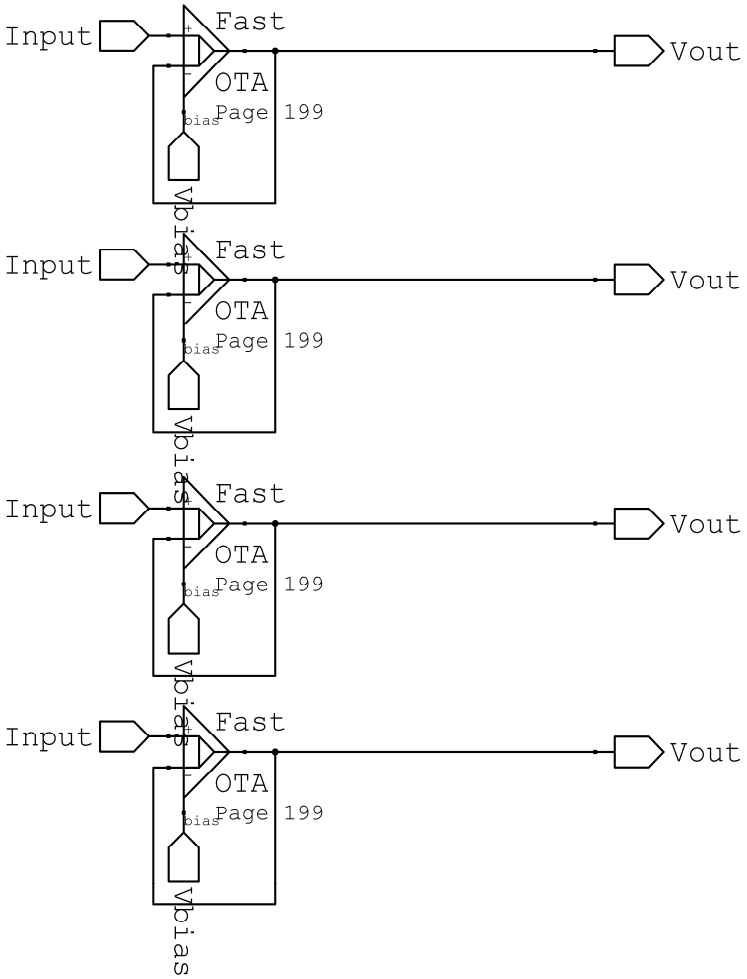
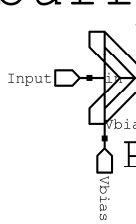
Analog Output Super Buffer (ao superbuff)





Page 71

<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET

W: Gate Width (l).

L: Gate Length (l).

AS / AD: Source/Drain Area A=W*L*l*l (l)

A: Area (squm).

PS /PD: Source/Drain parameter P=(W+L)*2*l (l)

P: parameter (um).

For SPICE Export. this .param statement must be placed on top level of the design hierarchy.

Include models

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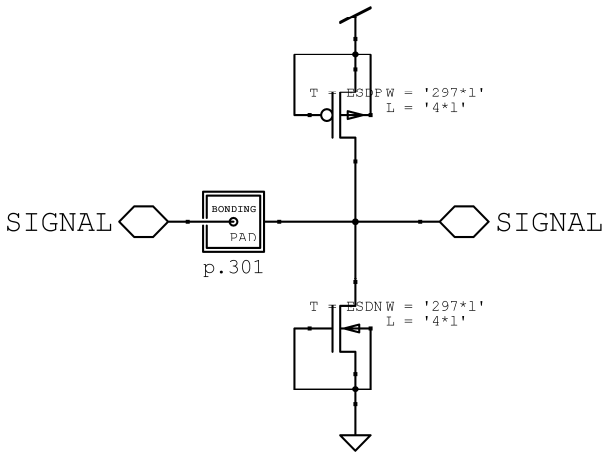
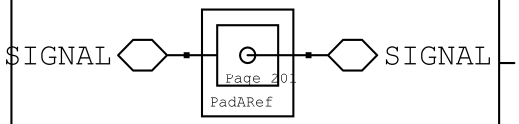


Include models



<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*1 (l)
P: parameter (um).

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

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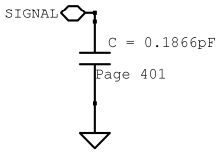
Pad_Bond

p.301



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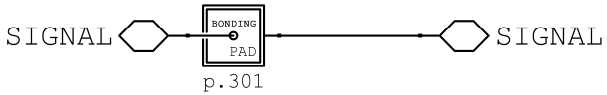
PadHFIn



p.301

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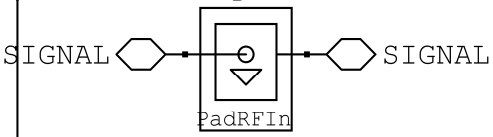

Include models

<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET
W: Gate Width (1).
L: Gate Length (1).
AS / AD: Source/Drain Area A=W*L*1*1 (1)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*1 (1)
P: parameter (um).

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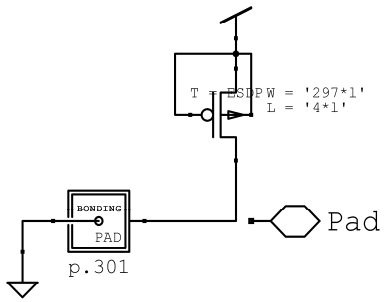
PadGnd



Include models

<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
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A: Area (squm).
PS /PD: Source/Drain paramoter P=(W+L)*2*l (l)
P: parameter (um).

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PadInC

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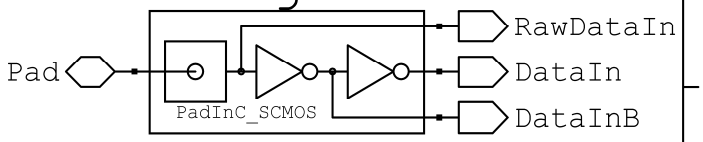
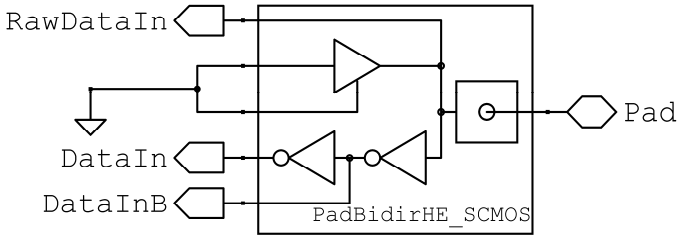


Page 210



Include models

<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*l*l (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*l (l)
P: parameter (um).

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

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Rev = A
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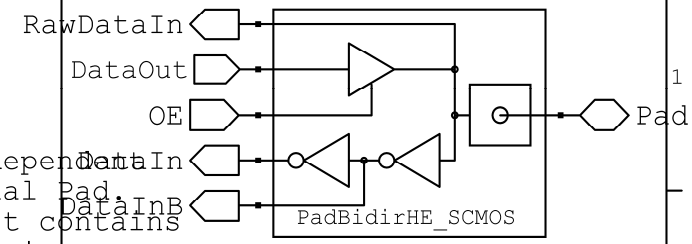
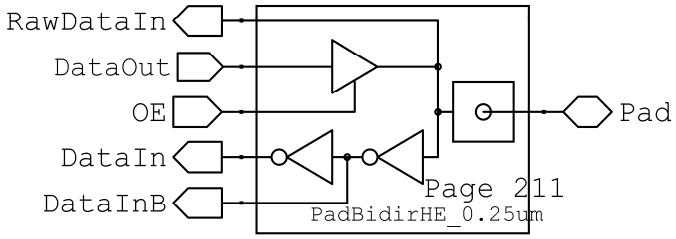
Bidirectional Pad

This module is the technology independent implementation of the Bidirectional Pad. It can be used for TPR, however it contains no information for exporting to Spice. In order to specify a technology for exporting to Spice, instance the appropriate PadBidirHE below.





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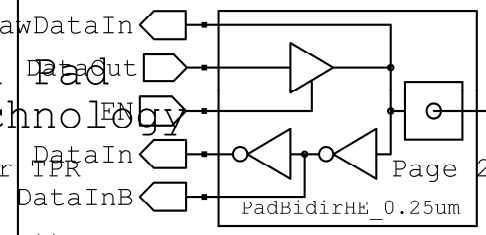
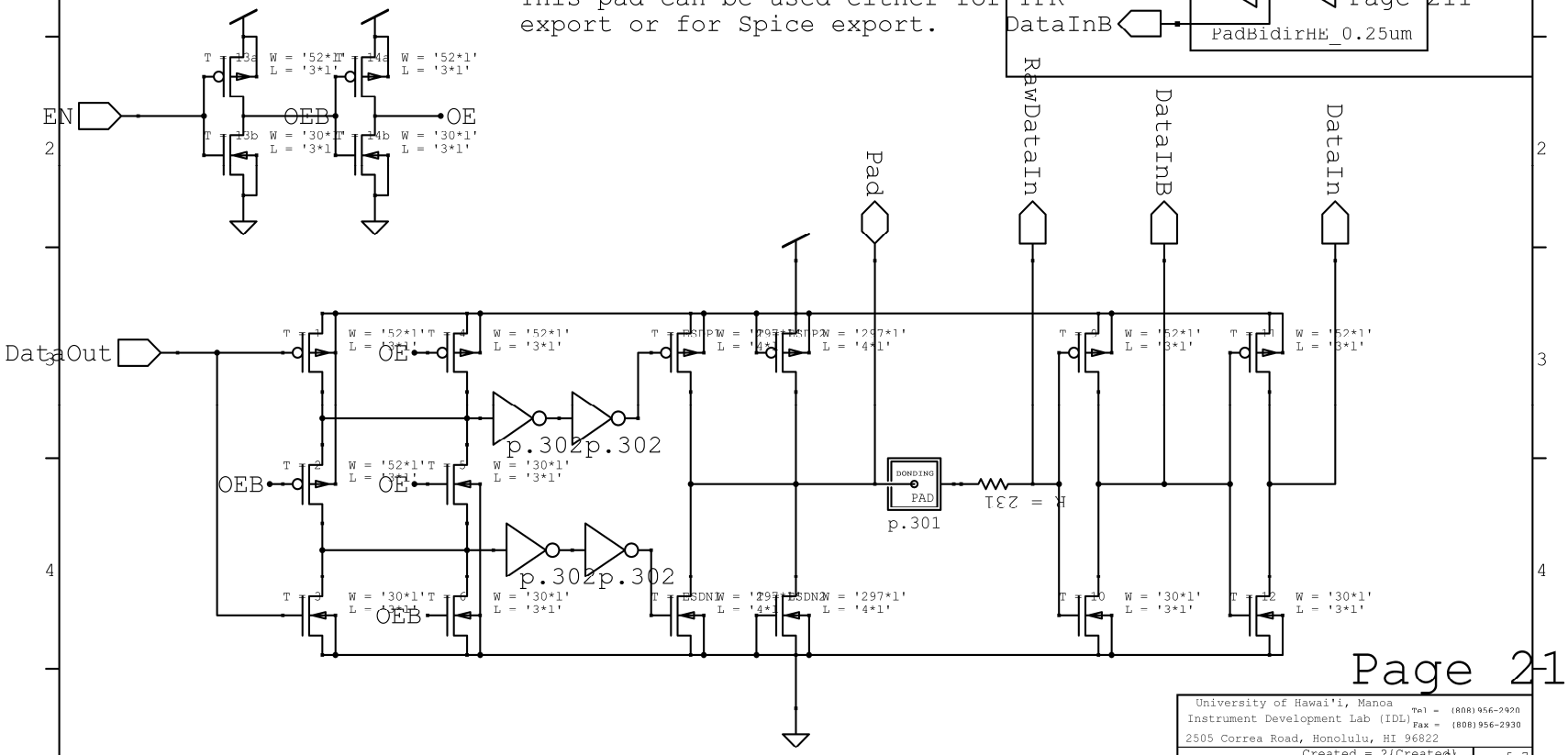
Designer = ?{Author}	
Module = ?{Cell}	Page = {Page}
Path = ?{Design}	

Hi-ESD Bidirectional Pad
TSMC 0.25u MOSIS Technology

This pad can be used either for TPR export or for Spice export.



Page 211



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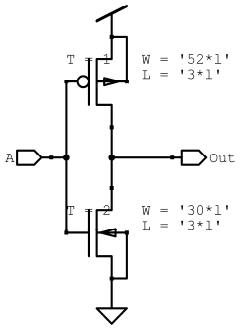
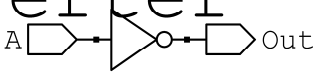
Generic digital IO Inverter

Inv





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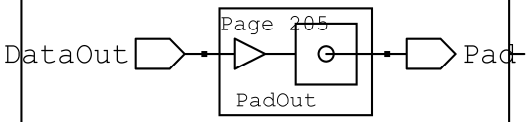
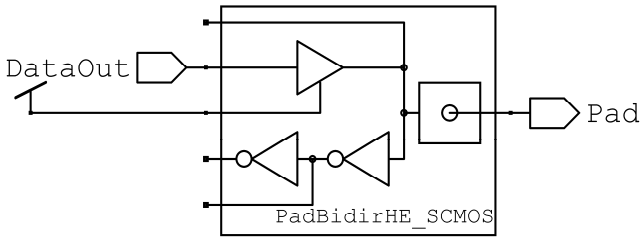


Page 210



Include models

<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*l (l)
A: Area (squm).
PS /PD: Source/Drain paramoter P=(W+L)*2*l (l)
P: parameter (um).

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

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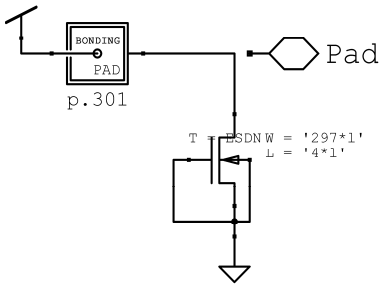
PadVdd



Include models

<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*1 (l)
A: Area (squm).
PS /PD: Source/Drain paramoter P=(W+L)*2*1 (l)
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PadVdd

Page 204

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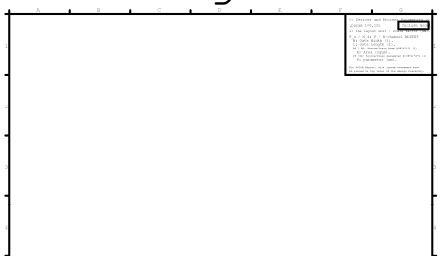
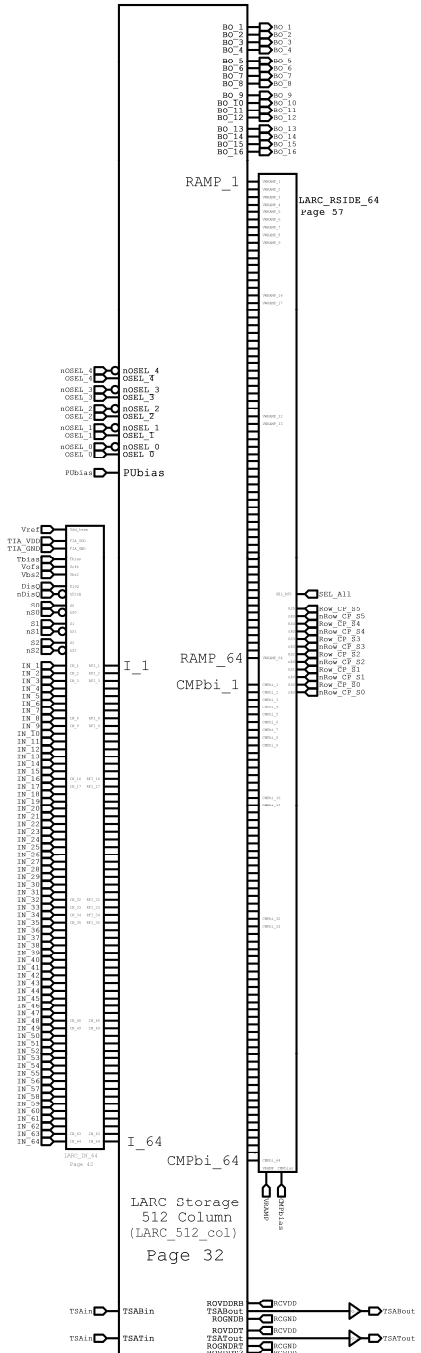
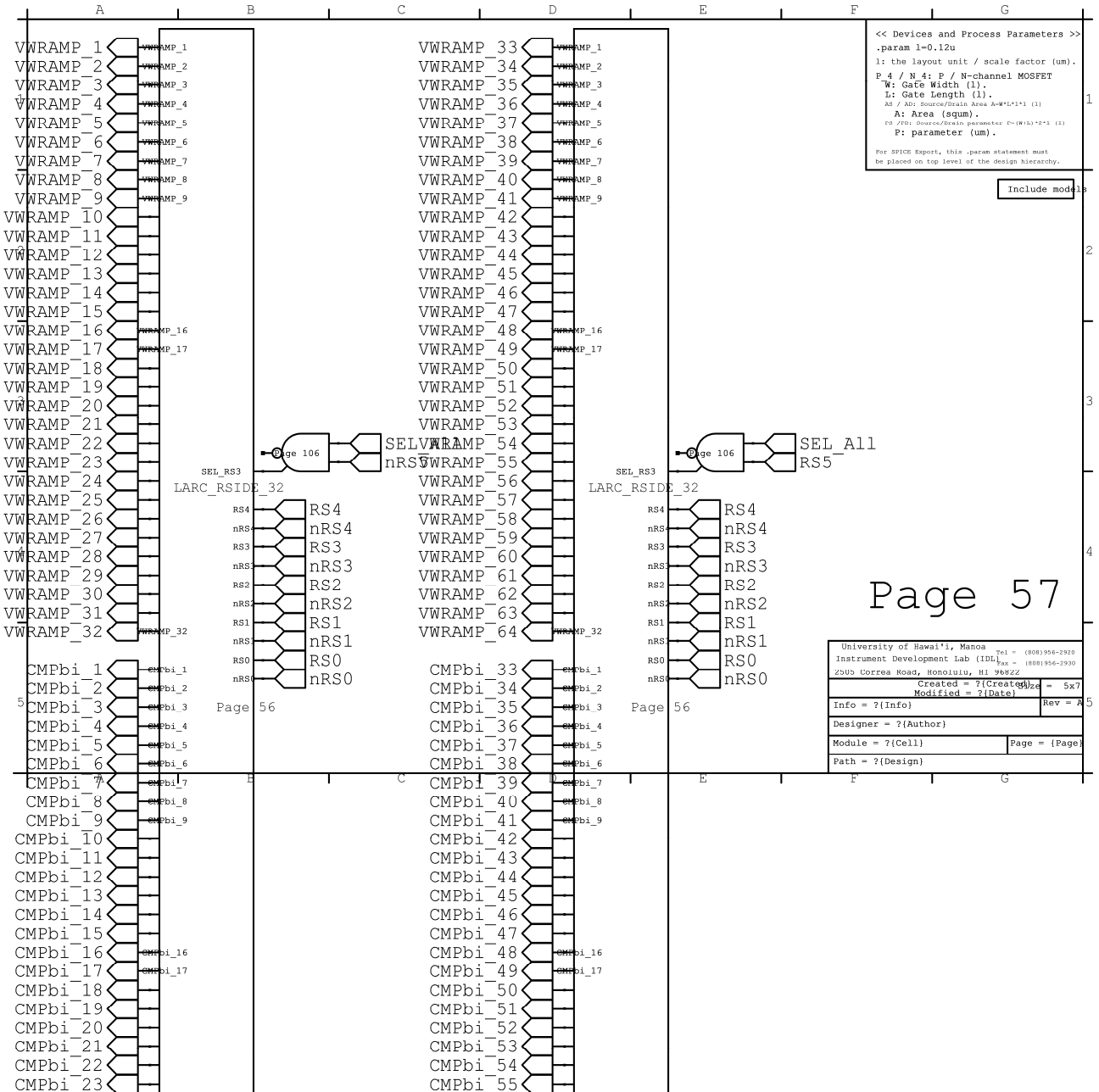
Monster Core (core)

Page 3

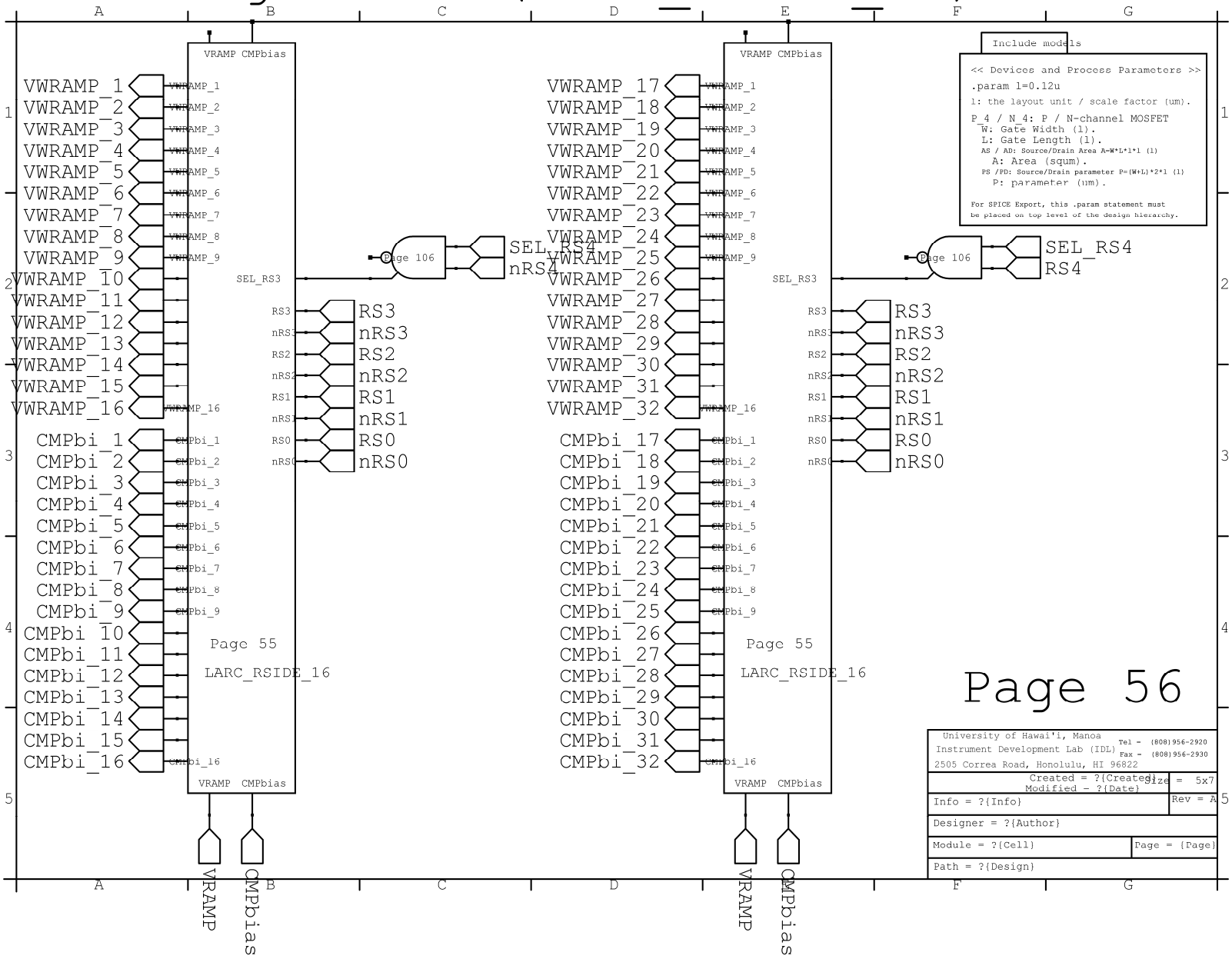




LARC RightSide (LARC RSIDE 64)



LARC RightSide (LARC_RSIDE_32)



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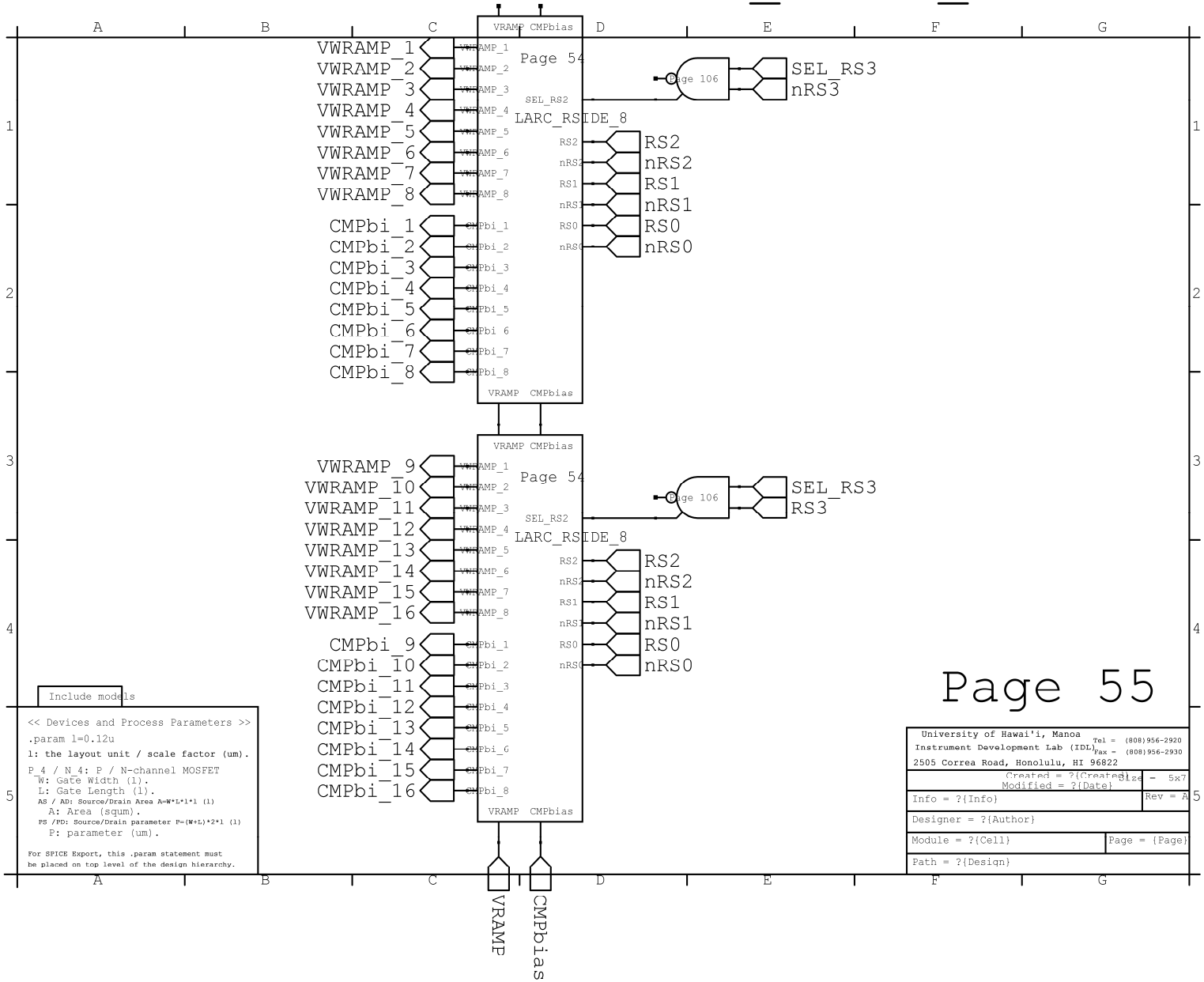
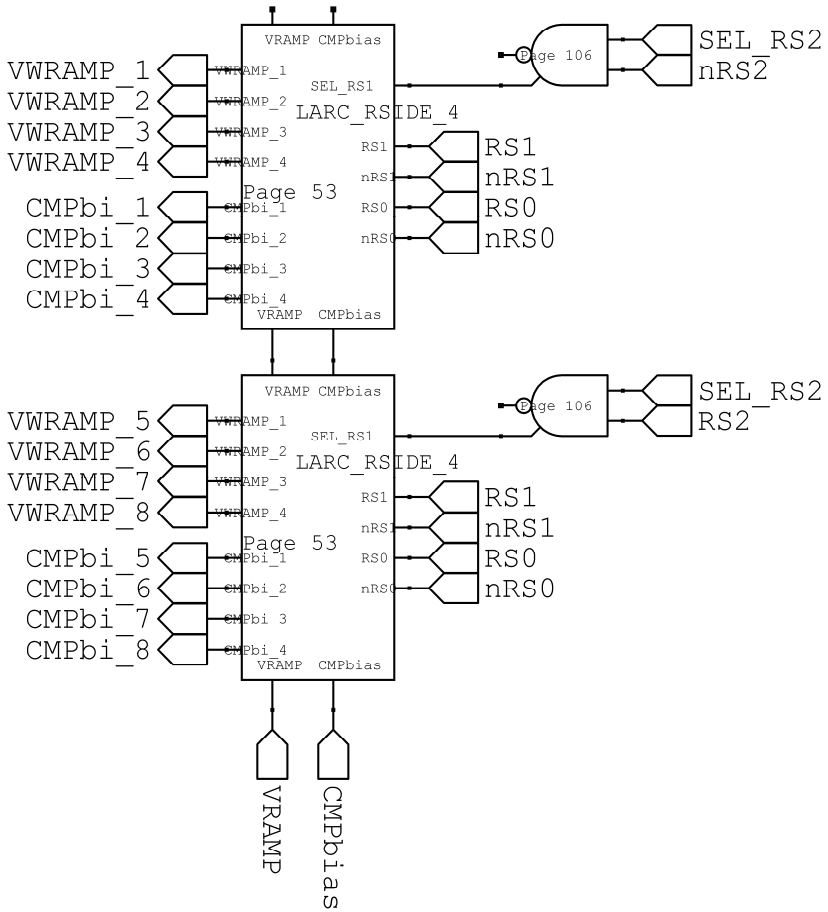
LARC RightSide (LARC_RSIDE_16)



LARC RightSide (LARC_RSIDE_8)



Include models

<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*l*l (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*l (l)
P: parameter (um).

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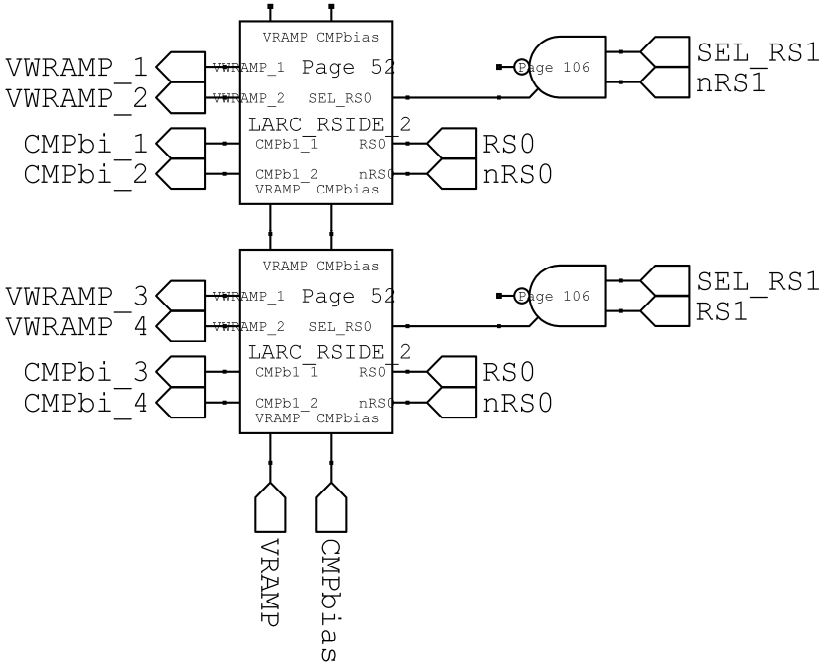
LARC RightSide (LARC_RSIDE_4)



Include models

<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET

W: Gate Width (l).

L: Gate Length (l).

AS / AD: Source/Drain Area A=W*L*l*l (l)

A: Area (squm).

PS /PD: Source/Drain parameter P=(W+L)*2*l (l)

P: parameter (um).

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

University of Hawai'i, Manoa
Instrument Development Lab (IDL)
2505 Correa Road, Honolulu, HI 96822
Tel = (808)956-2920
Fax = (808)956-2930

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Modified = ?{Date}
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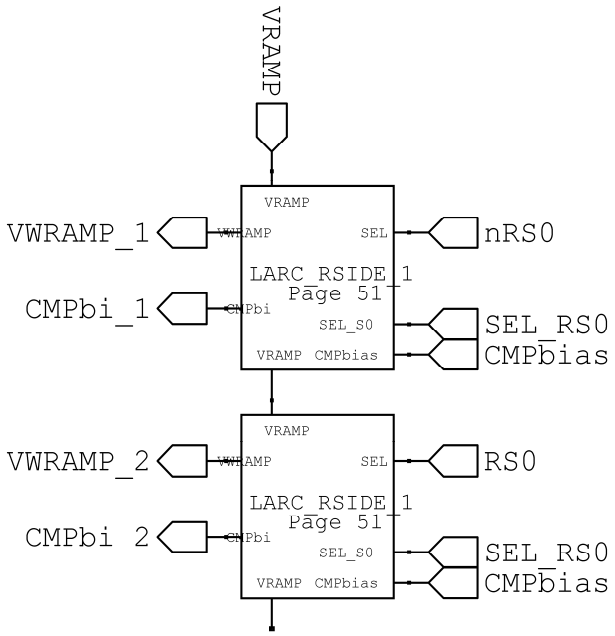
LARC Rightside (LARC_RSIDE_2)



<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*l*l (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*l (l)
P: parameter (um).

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

Include models

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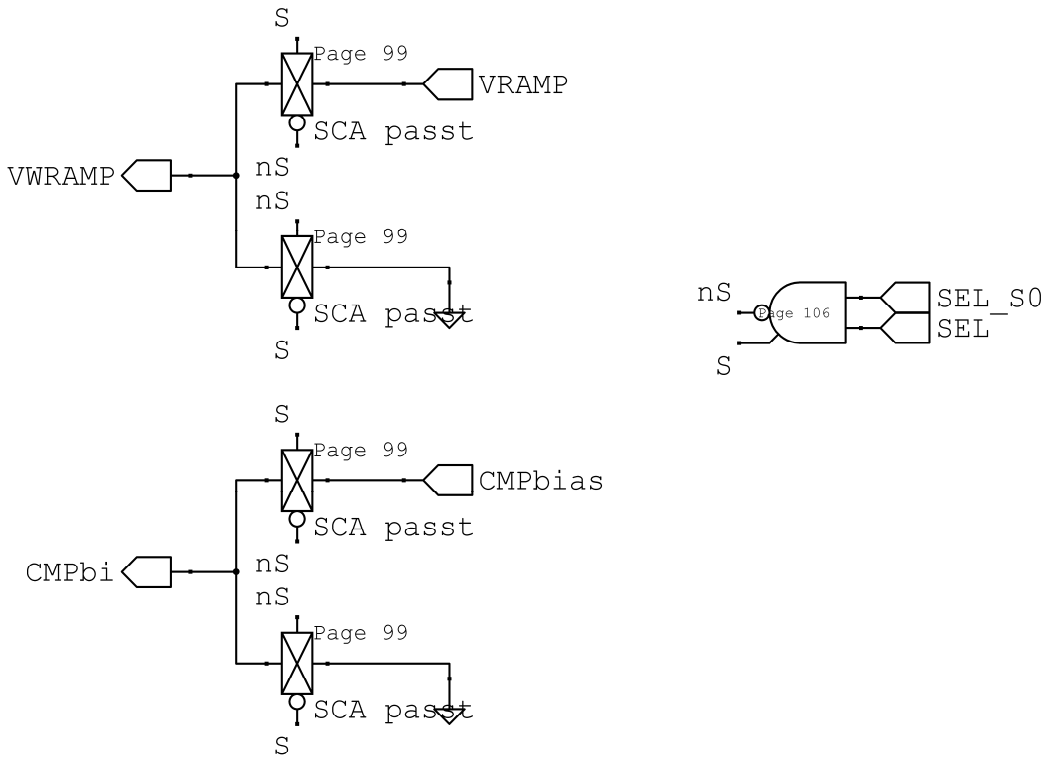
LARC RightSide Select (LARC_RSIDE_1)




```
<< Devices and Process Parameters >>
.param l=0.12u
l: the layout unit / scale factor (um).
P_4 / N_4: P / N-channel MOSFET
  W: Gate Width (l).
  L: Gate Length (l).
  AS / AD: Source/Drain Area A=W*L*l*l (l)
    A: Area (squm).
  PS /PD: Source/Drain parameter P=(W+L)*2*l (l)
    P: parameter (um).

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be placed on top level of the design hierarchy.
```

Include models

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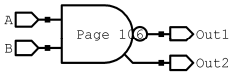

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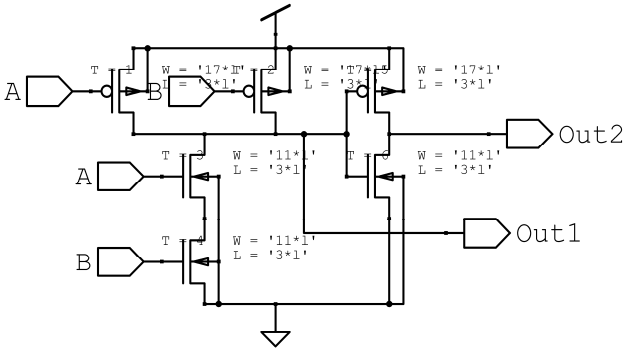
NAND2C



<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P 4 / N 4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*l*l (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*l (l)
P: parameter (um).

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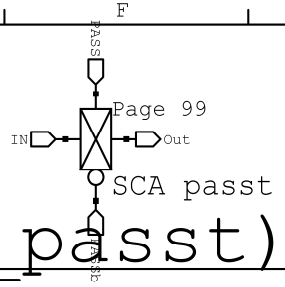
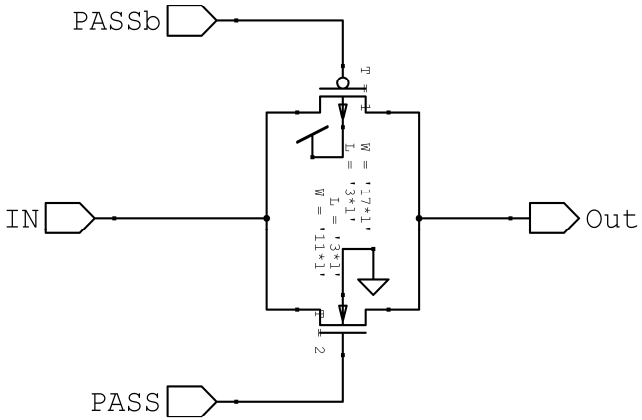
Module = ?{Cell}	Page = {Page}
Path = ?{Design}	

SCA Pass Transistor (big_passt)



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<< Devices and Process Parameters >>
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P_4 / N_4: P / N-channel MOSFET
  W: Gate Width (l).
  L: Gate Length (l).
  AS / AD: Source/Drain Area A=W*L*1*1 (l)
    A: Area (squm).
  PS /PD: Source/Drain parameter P=(W+L)*2*1 (l)
    P: parameter (um).

For SPICE Export, this .param statement must
be placed on top level of the design hierarchy.
```

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Instrument Development Lab (IDL)
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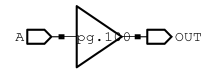

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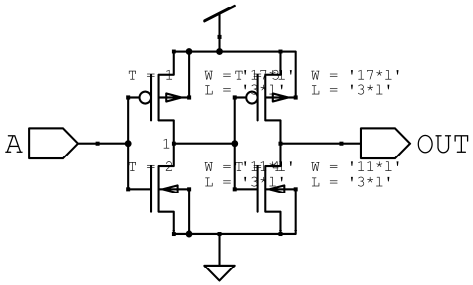

SCA Page 100

Include models

<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET

W: Gate Width (l).

L: Gate Length (l).

AS / AD: Source/Drain Area A=W*L*1*1 (l)

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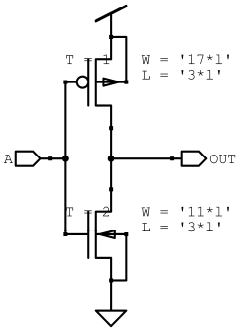

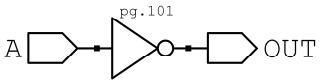

[NETTRAN OUTPUT=<# SCMOS_INV %{A} %{Out} VDD GND]

Inv

SCA Page 101

Include models

<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
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A: Area (squm).
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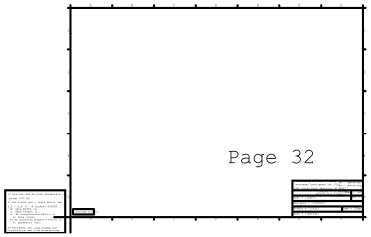
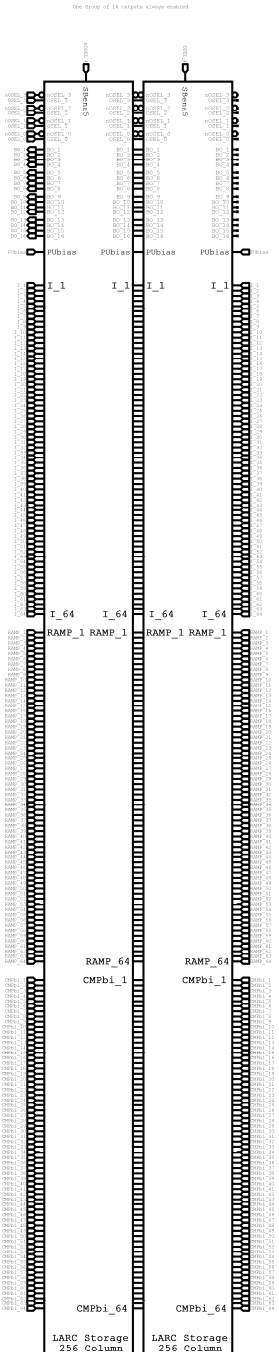
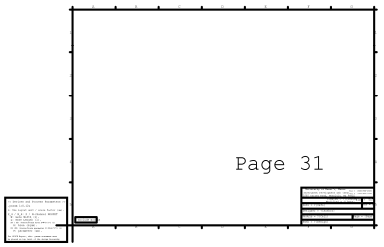
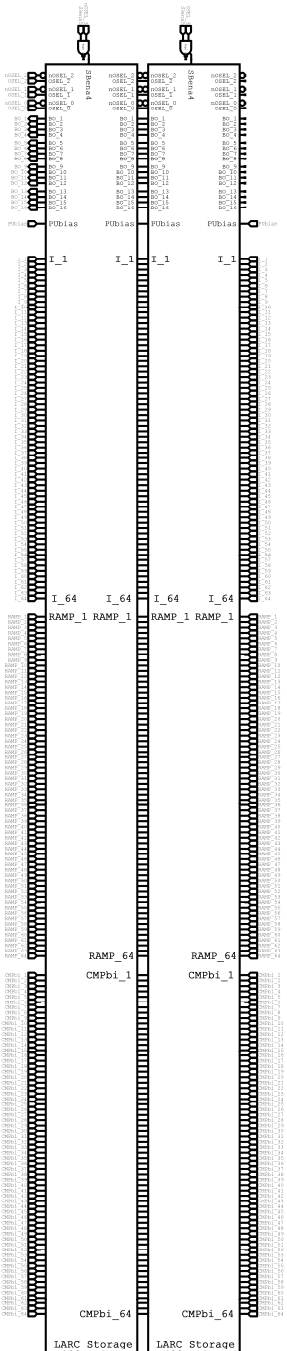
LARC Storage 512 Column (LARC_512_col)



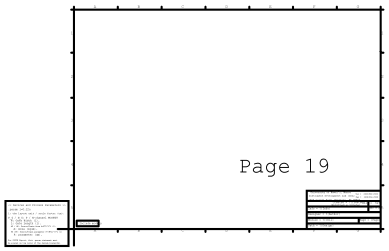


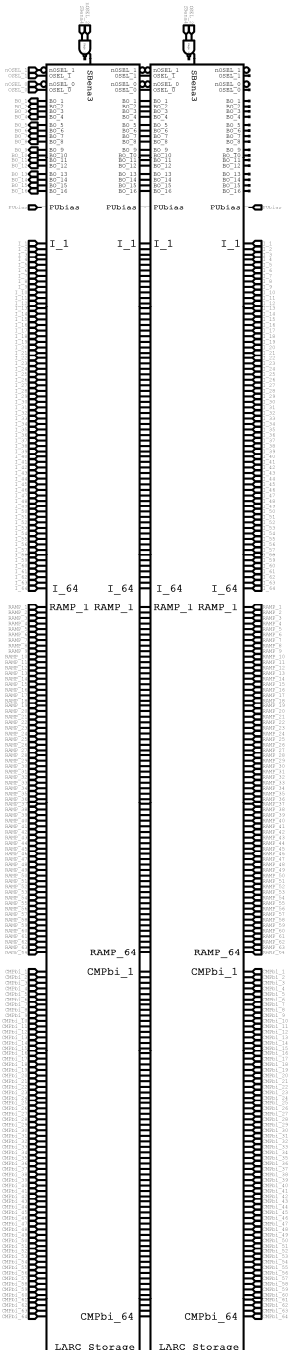
LARC Storage 256 Column (LARC_256_col)



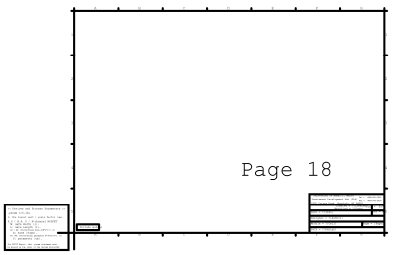


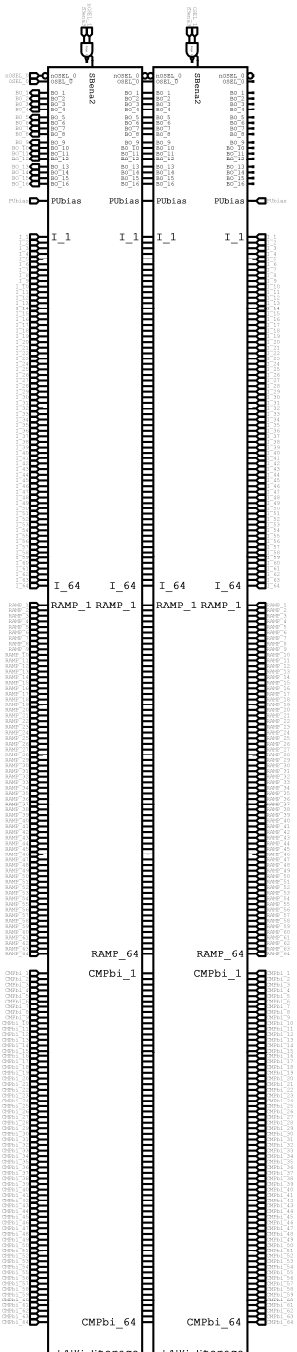
LARC Storage 128 Column (LARC_128_col)



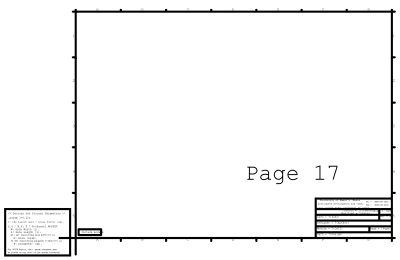


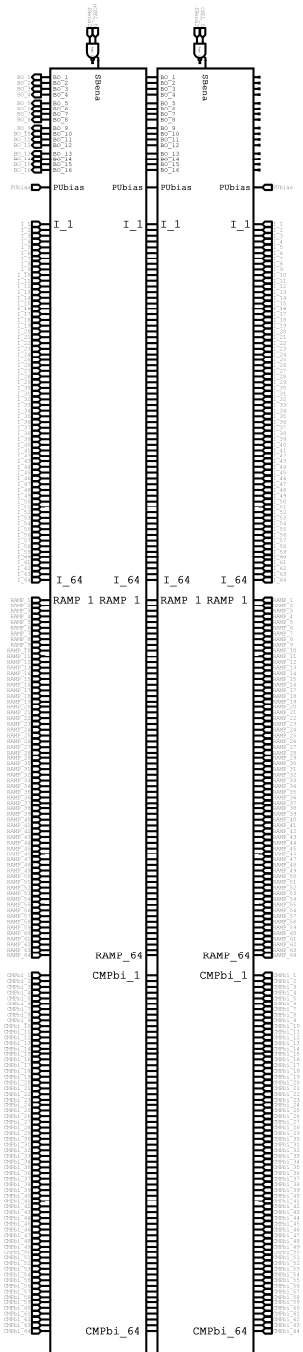
LARC Storage 64 Column (LARC_64_col)



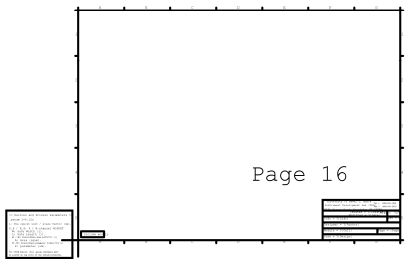


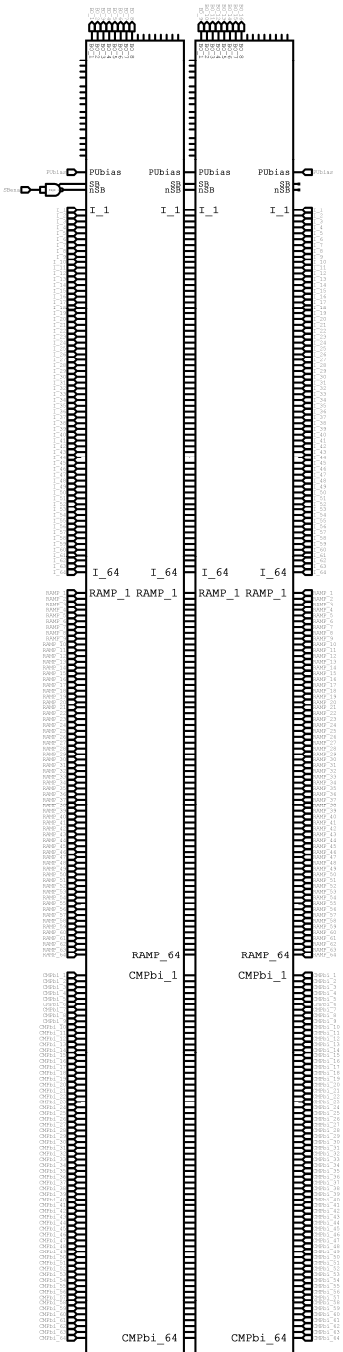
LARC Storage 32 Column (LARC_32_col)



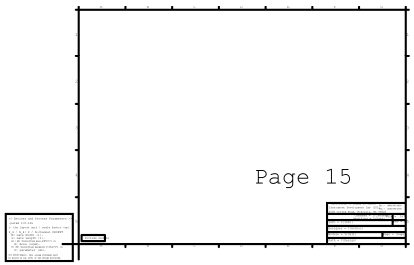


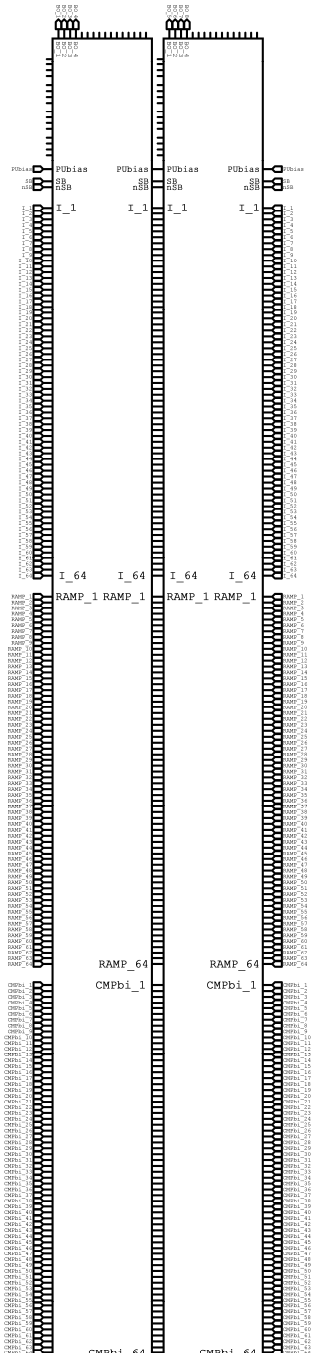
LARC Storage 16 Column (LARC_16_col)





LARC Storage 8 Column (LARC_8_col)





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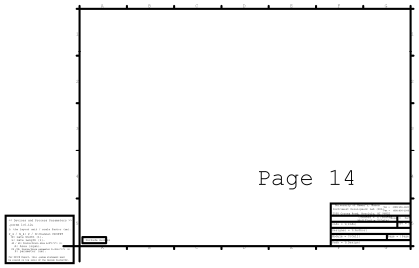
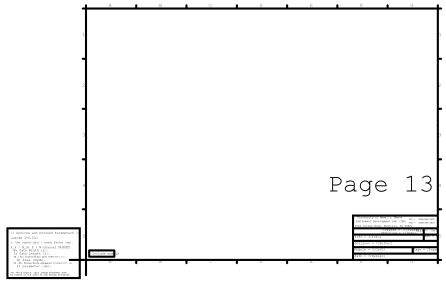
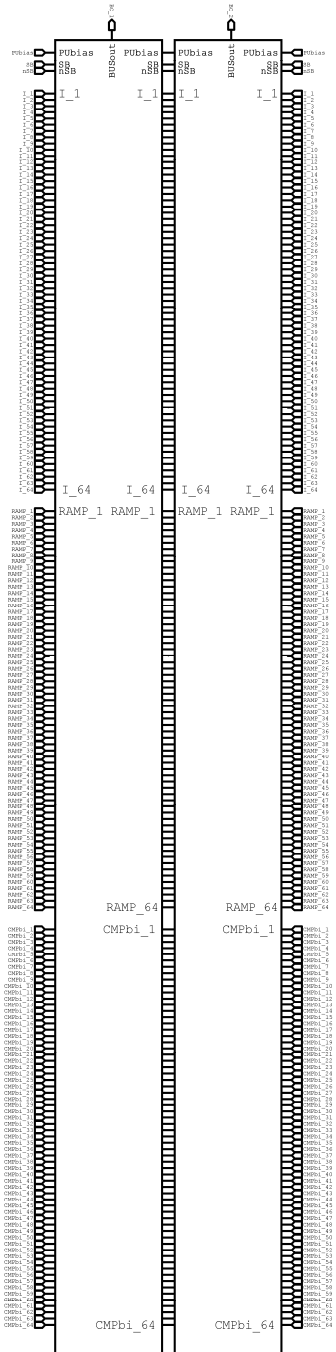
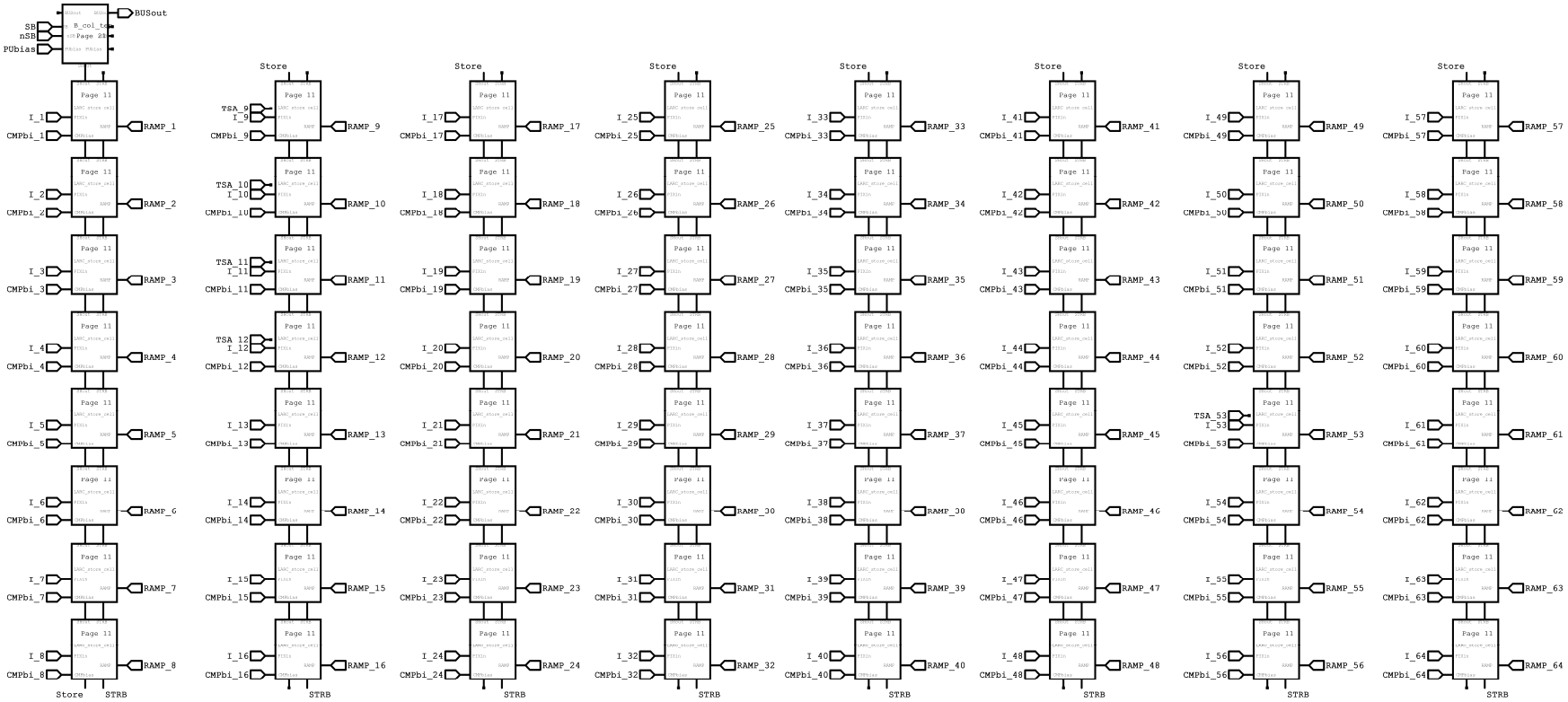


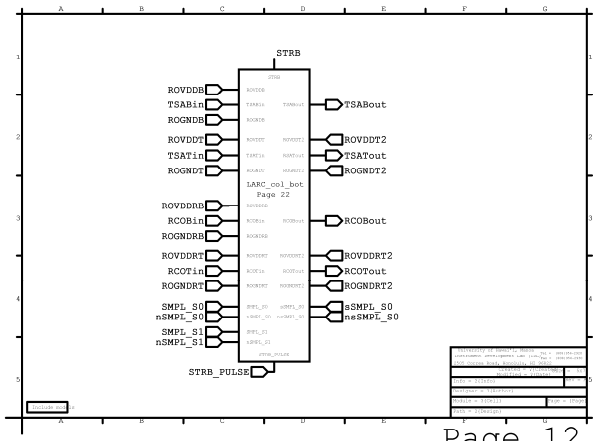
LARC Storage Double Column (LARC_2_col)



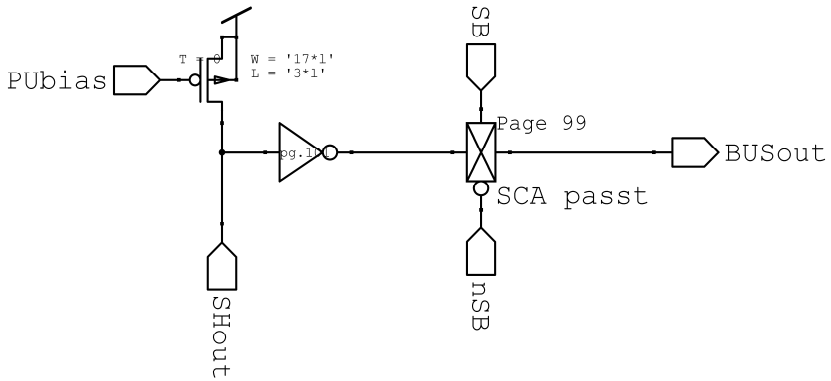




LARC Storage Single Column (LARC_single_col)



LARC Storage Column Top (LARC_col_top)



<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*1*l (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*l (l)
P: parameter (um).

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

Include models

Page 21

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Size = 5x7
Info = ?{Info}
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Designer = ?{Author}
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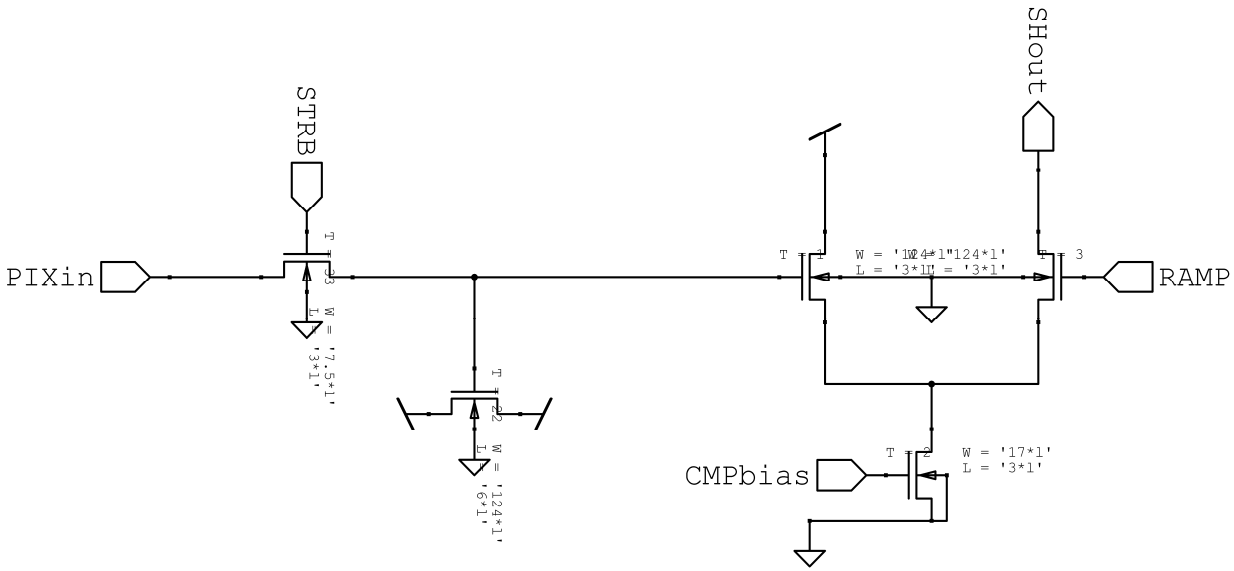
LARC Storage Cell (LARC_store_cell)



Capacitance =18.88um x (0.72um + 0.36um) = ~90fF

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<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*l*l (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*l (l)
P: parameter (um).

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Include models

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Created = ?{Created}
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Designer = ?{Author}
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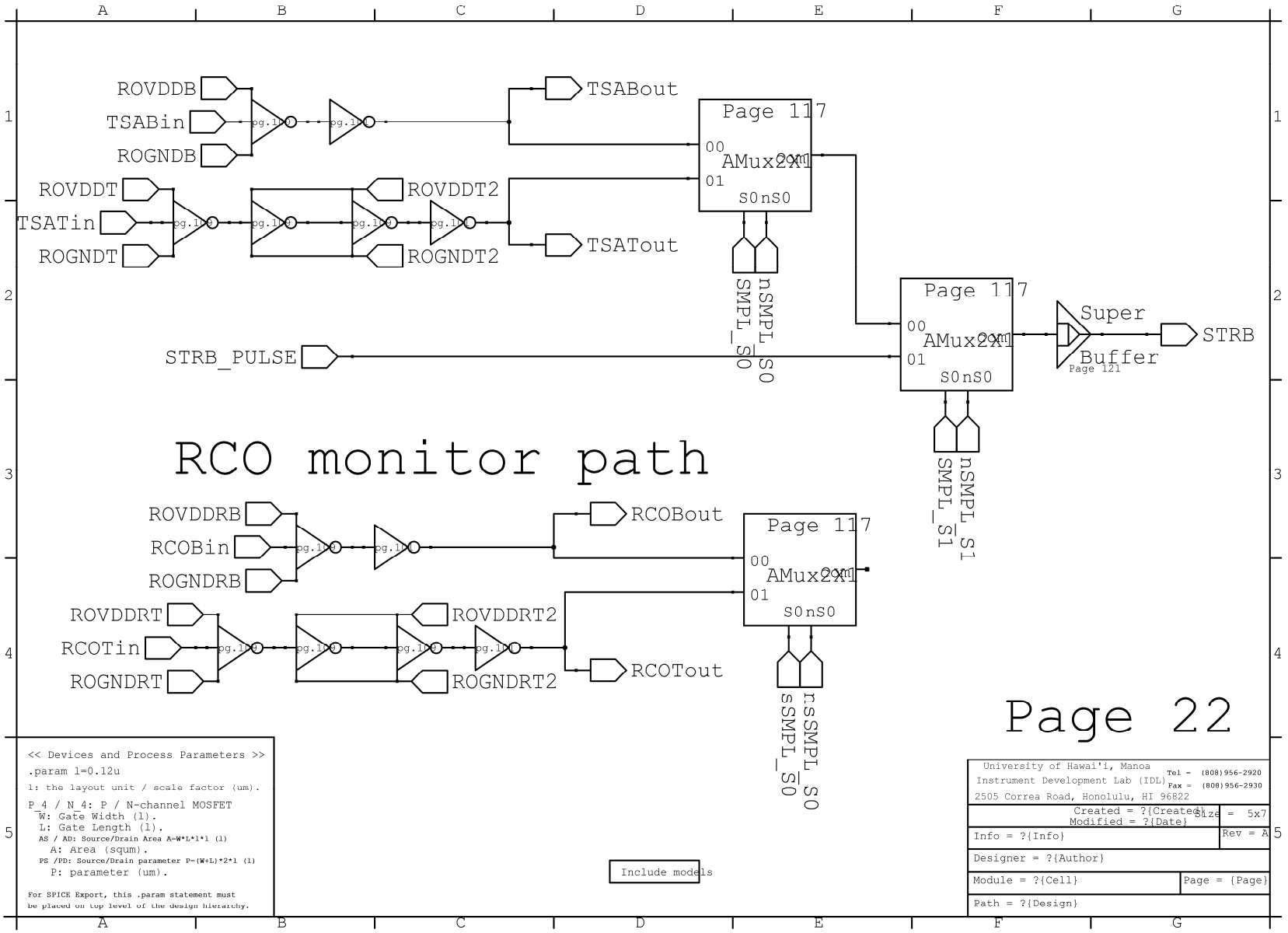
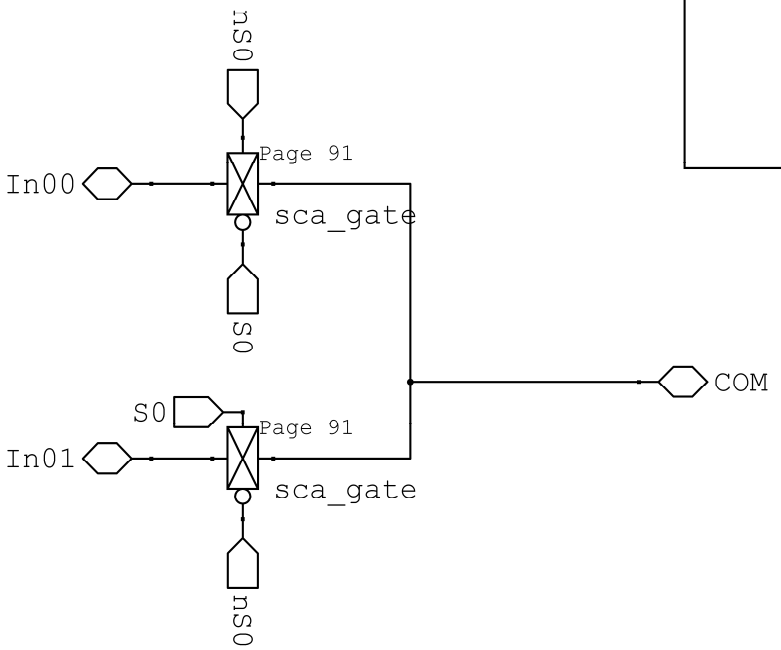
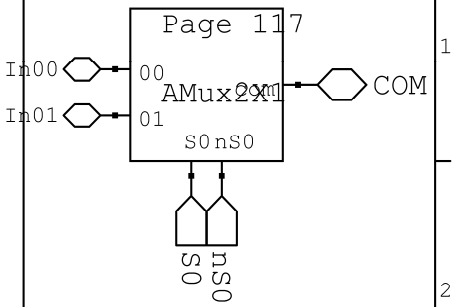
Path = ?{Design}

LARC Column [timing] Bot (LARC_col_bot)



Analog 2x1 Mux (AMux2X1)





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Instrument Development Lab (IDL)
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Tel = (808)956-2920
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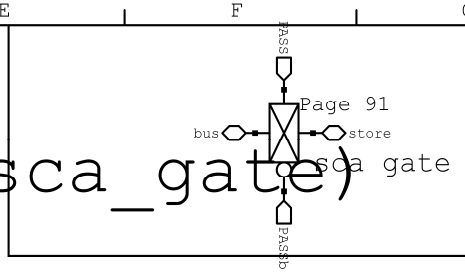
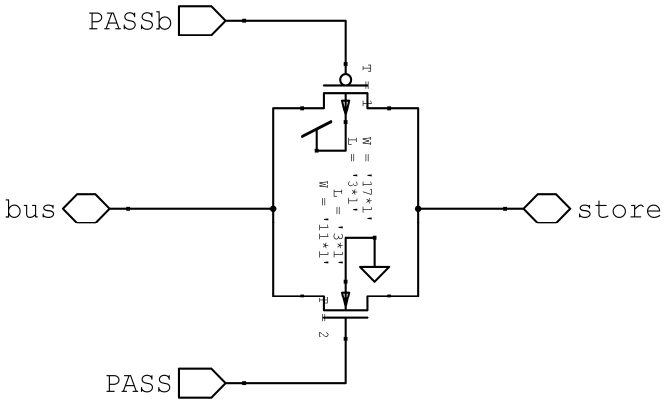
Module = ?{Cell}	Page = ?{Page}
Path = ?{Design}	

SCA Pass Transistor (sca_gate)





Include models

<< Devices and Process Parameters >>

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L: Gate Length (l).
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A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*l (l)
P: parameter (um).

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SCA Page 91

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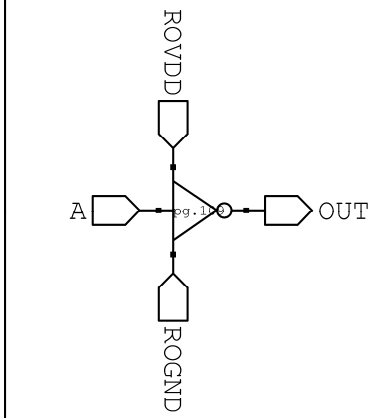
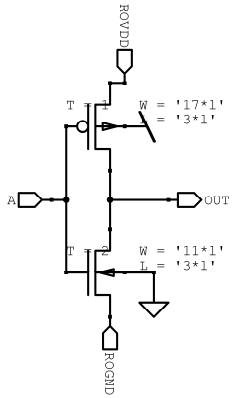
Path = ?{Design}	

Ring Oscillator Inverter (ring_osc_inv)





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Include models

<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET

W: Gate Width (l).

L: Gate Length (l).

AS / AD: Source/Drain Area A=W*L*l*l (l)

A: Area (squm).

PS /PD: Source/Drain parameter P=(W+L)*2*l (l)

P: parameter (um).

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

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Tel = (808)956-2920
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Modified = ?{Date}
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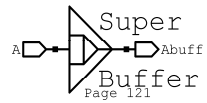
Page = {Page}
Path = ?{Design}

Super Buffer (super_buff)



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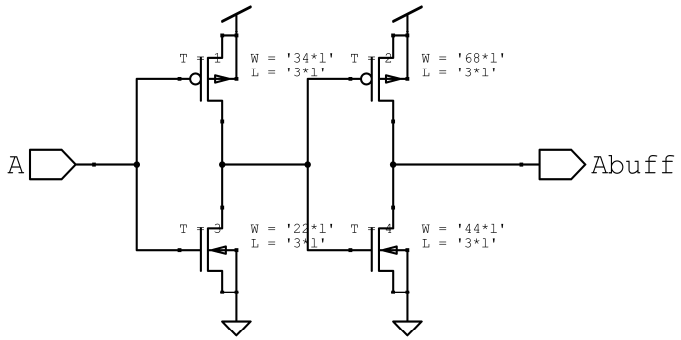

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<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET
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L: Gate Length (l).
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Include models

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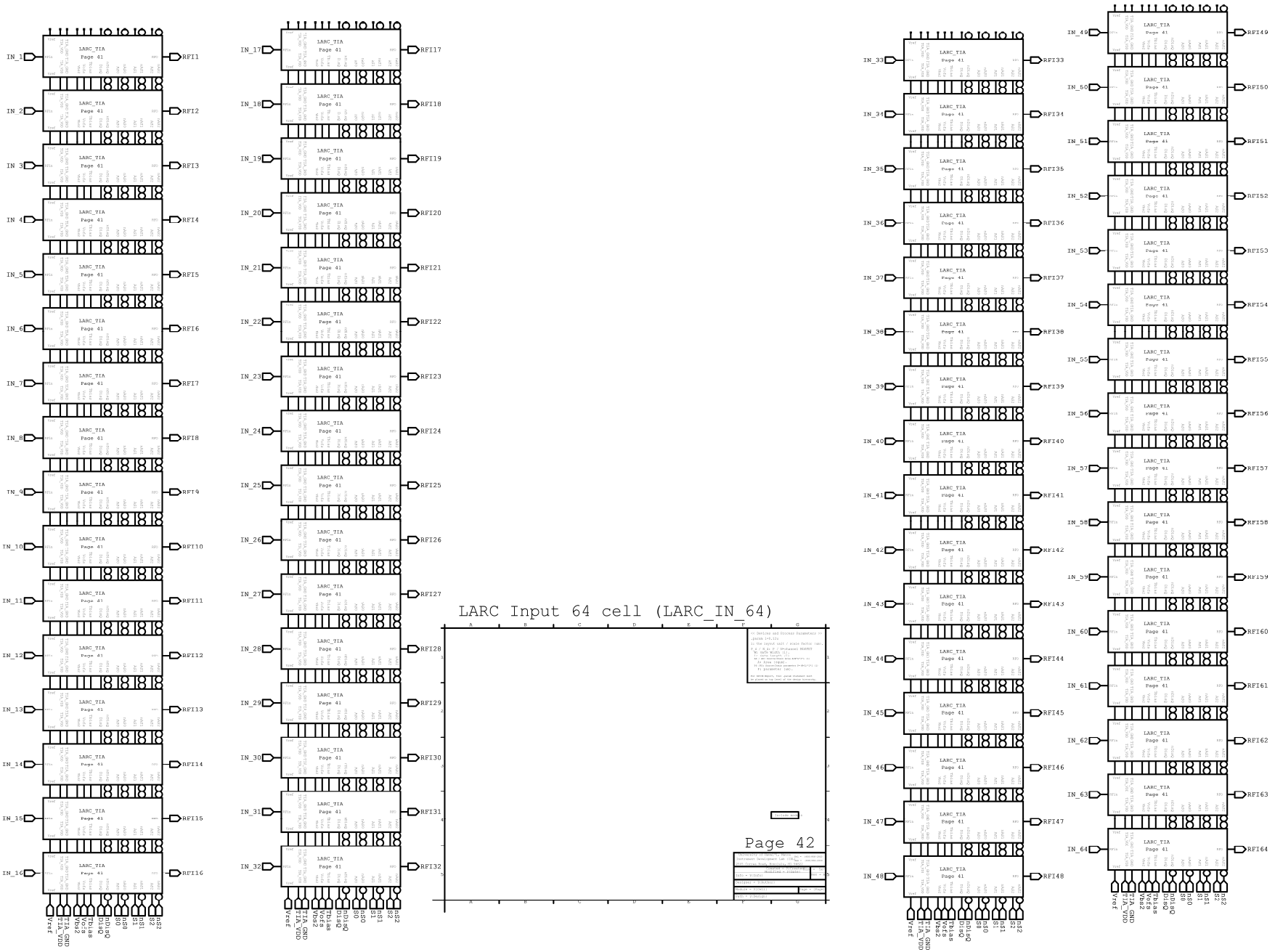

LARC Input 64 cell (LARC_IN_64)
Page 42

Simulation page is LARC_TIA_4

1pF Cap:

6.134fF/um^2

1pF = 163um^2

T2 size:

L=171 (20.58um)

W=66 (7.92um)

163um^2

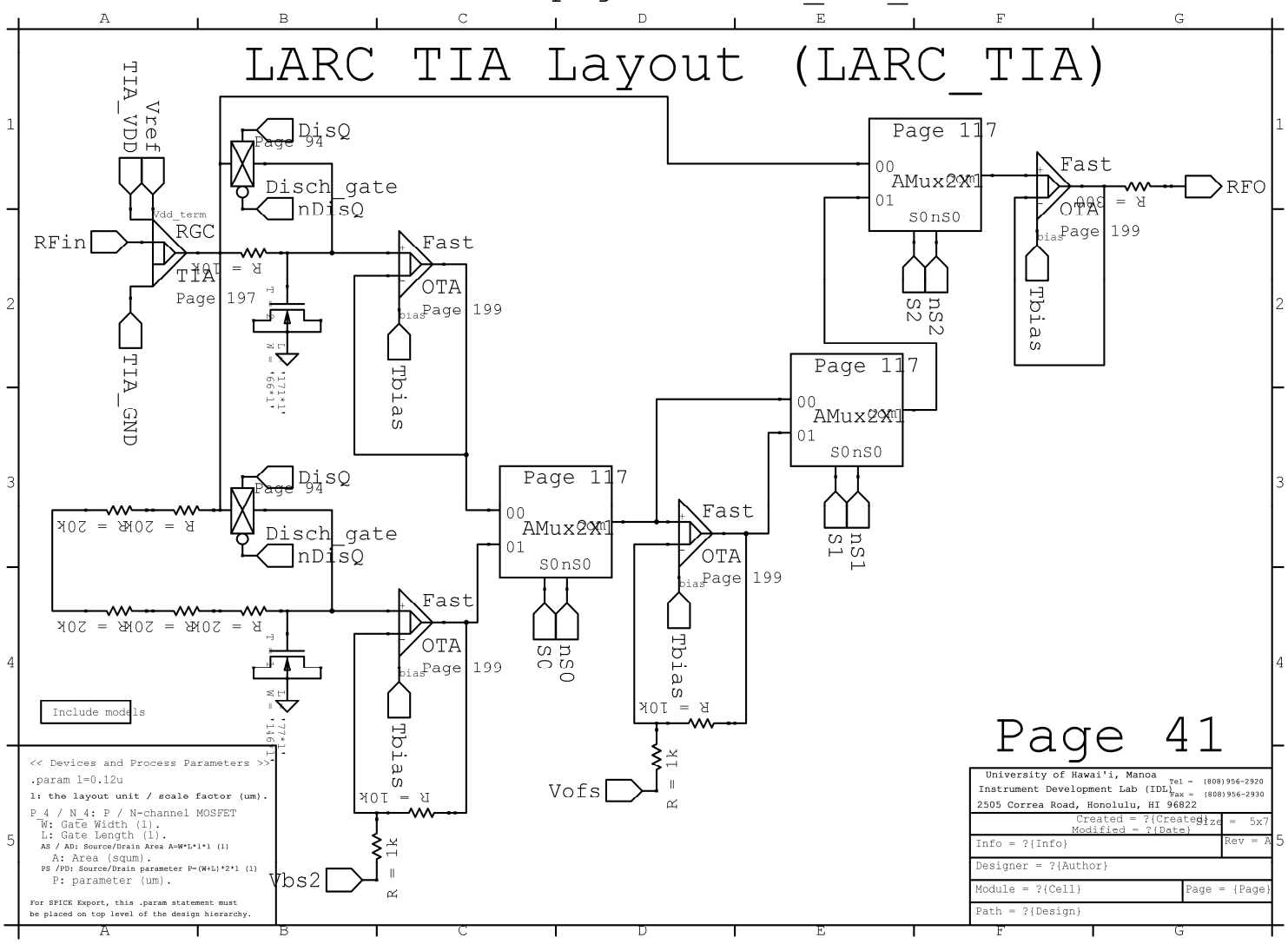
T1 size:

L=77 (9.24um)

W=146 (17.52um)

161.9um^2

LARC TIA Layout (LARC_TIA)



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Page = {Page}
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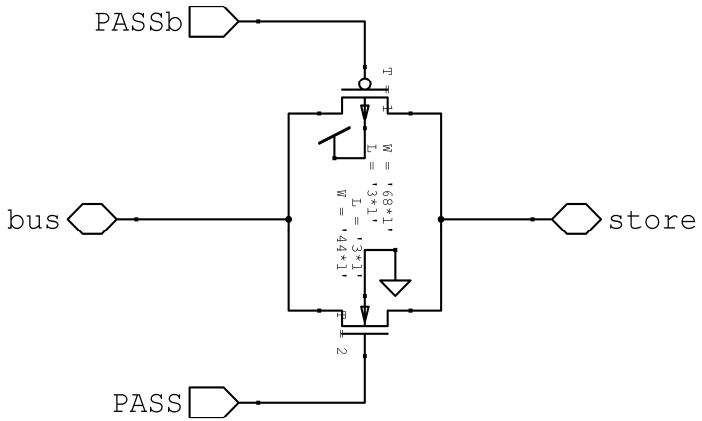
LARC Discharge Gate (Disch_gate)



Include models

<< Devices and Process Parameters >>

.param l=0.12u

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A: Area (squm).
PS /PD: Source/Drain paramoter P=(W+L)*2*1 (l)
P: parameter (um).

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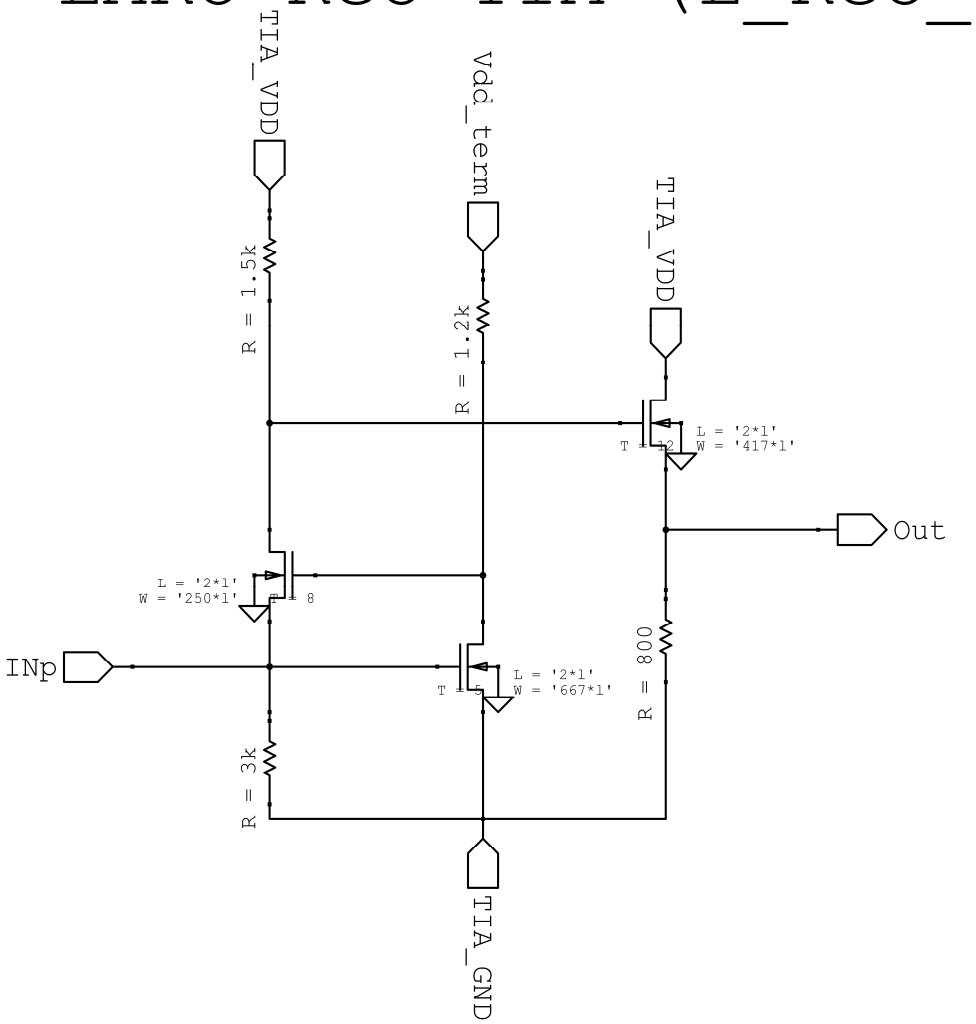
Designer = ?{Author}	
Module = ?{Cell}	Page = {Page}
Path = ?{Design}	

LARC RGC TIA (L_RGC_TIA)



<< Devices and Process Parameters >>

.param l=0.12u

l: the layout unit / scale factor (um).

P_4 / N_4: P / N-channel MOSFET
W: Gate Width (l).
L: Gate Length (l).
AS / AD: Source/Drain Area A=W*L*l*l (l)
A: Area (squm).
PS /PD: Source/Drain parameter P=(W+L)*2*l (l)
P: parameter (um).

For SPICE Export, this .param statement must be placed on top level of the design hierarchy.

Include models

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