

# Status of CDC Trigger Merger – Aurora on Altera



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# Outline



- Introduction
- Data Transmission between Xilinx and Altera
- Functional test of Altera transceiver
- Implement Aurora protocol in Altera
- Appropriate Altera chip

# Introduction



- Our FPGA design firmware is based on Altera both hardware and software. Our colleague is not willing to switch to Xilinx.
- To make this work possible, we have to investigate first the possibility of links between Altera and Xilinx through their transceivers (HSSIO , ROCKET IO).
- Also, it takes time for our EE colleague to familiar with our requirement ...

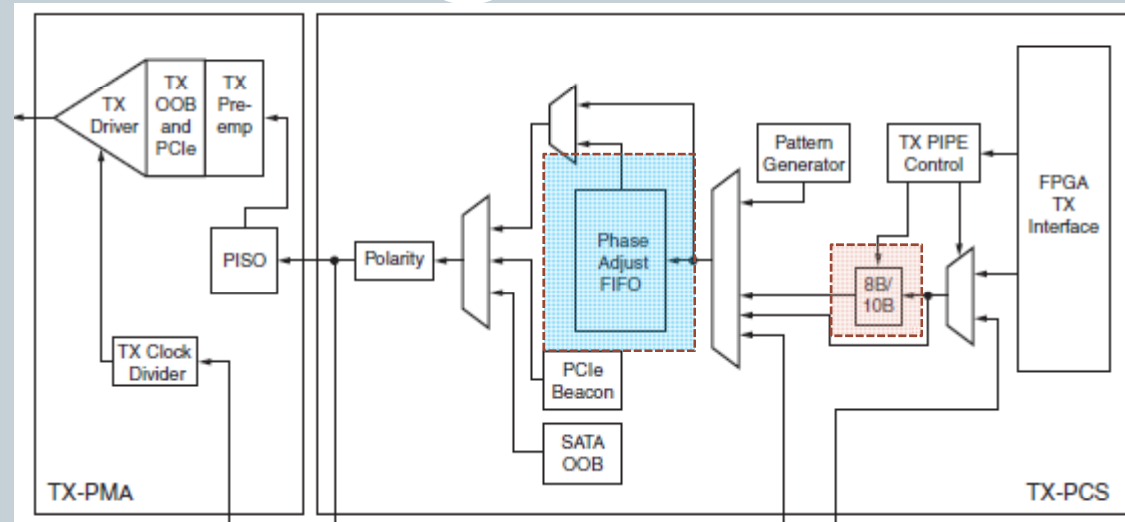
## What have been studied so far..



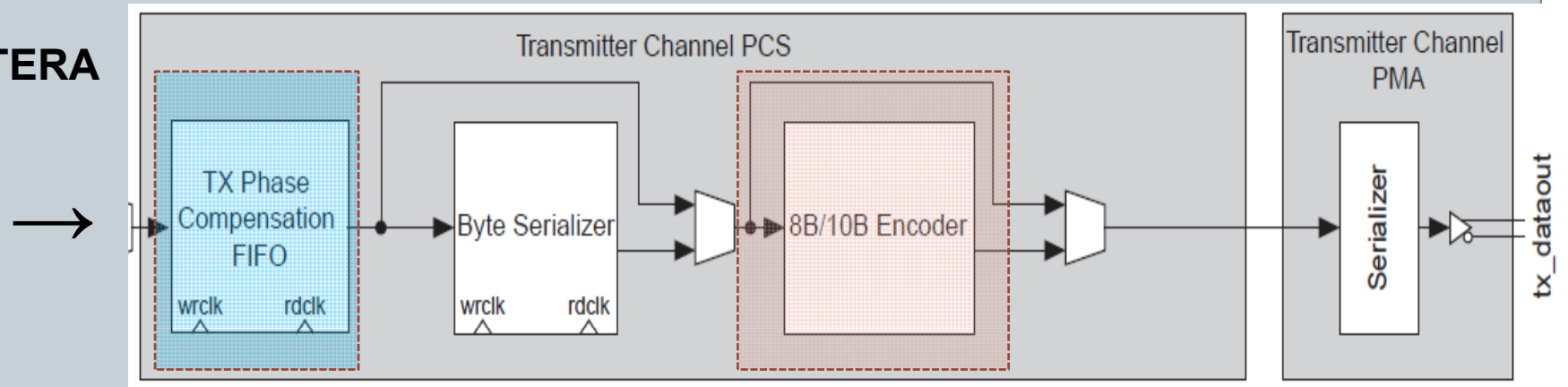
- Study the Xilinx Multi-Gigabit Transceiver(MGT) hardware structures and Altera's also.
- Study the Aurora Protocol parameters setting in Xilinx and find the corresponding setting in Altera
- Implement Aurora Protocol in Altera
- Find the appropriate chips (Arria II EP2AGX serial)

# Xilinx and Altera transceiver structure: **transmitter**

## XILINX

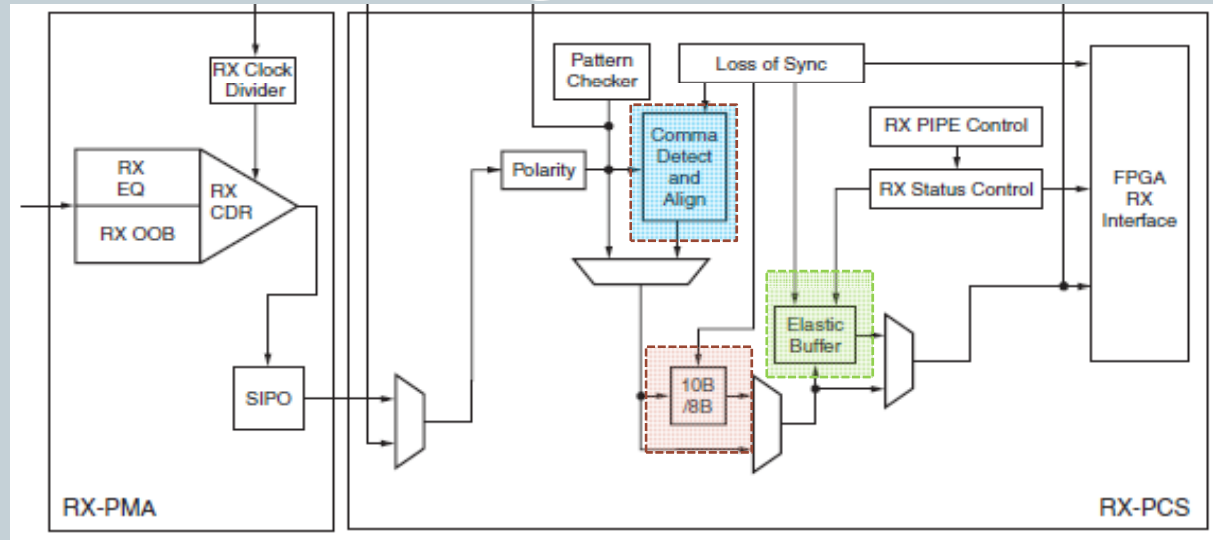


## ALTERA

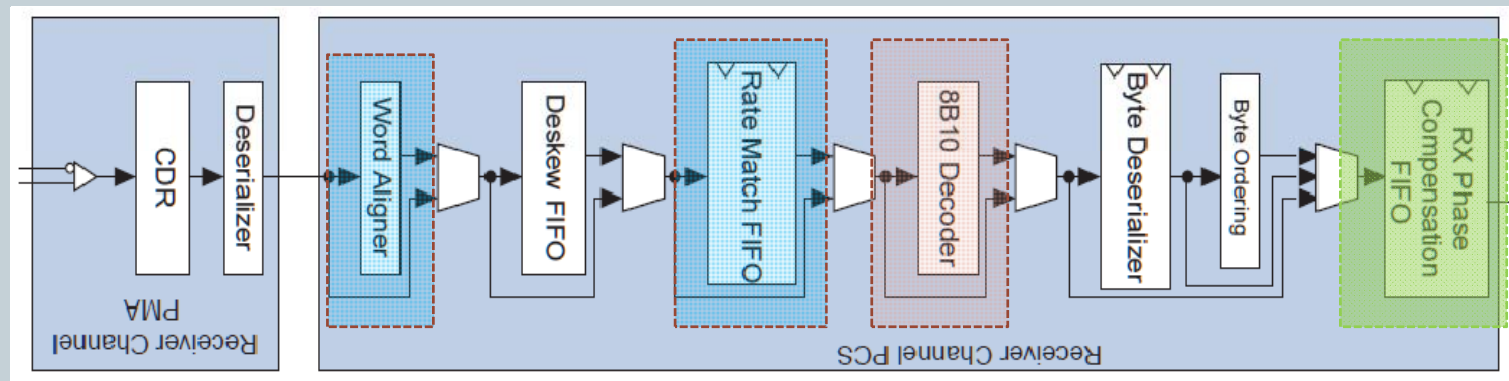


# Xilinx and Altera transceiver structure: **receiver**

**XILINX**



**ALTERA**



## Xilinx and Altera transceiver structure



- Apparently, the transceiver structures differ quite a lot, but there are still some corresponding functions can be located.
- If the functions Aurora used can be found in Altera, then we might be able to make data link through transceivers.

## Data transmission between Xilinx and Altera



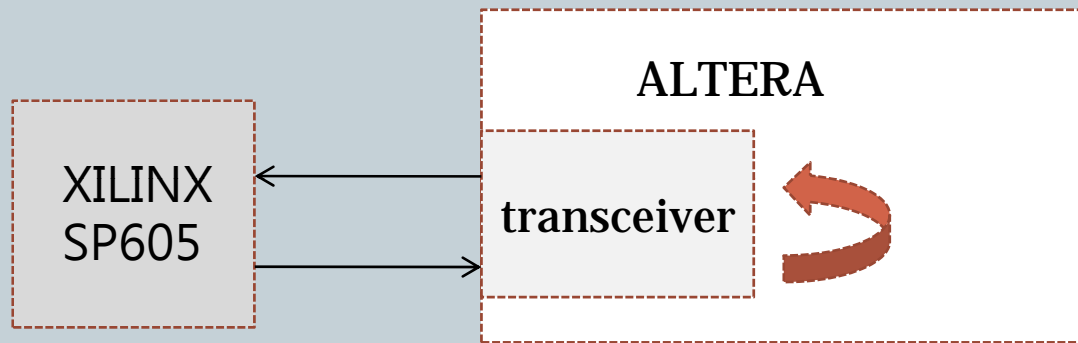
- Line rate: non-encoded data transmission rate
- Effective data rate: encoded data transmission rate
- Line rate: 3.125 Gbps, use 8b/10b encoding → effective data rate:  $3.125\text{G} * 0.8 = 2.5\text{ Gbps}$  .
  - Confirmed by Xilinx vs Altera data link
- Aurora uses 8b/10b encoding.



# Xilinx and Altera data link tests (No Aurora)



Test 1:

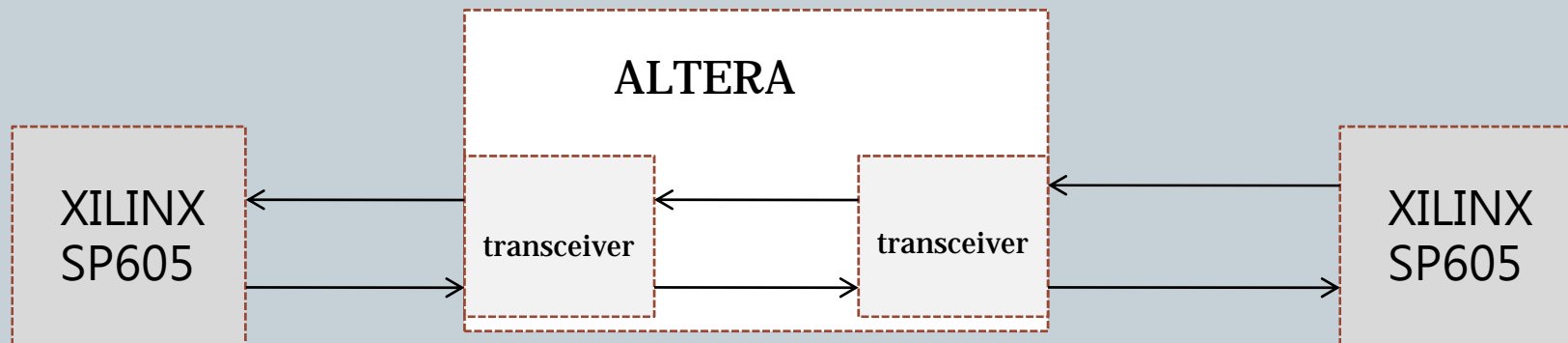


**Steps for connection:**

LANE\_UP ->  
CHANNEL\_UP ->  
send data

Use 16 bit data, Aurora  
not used

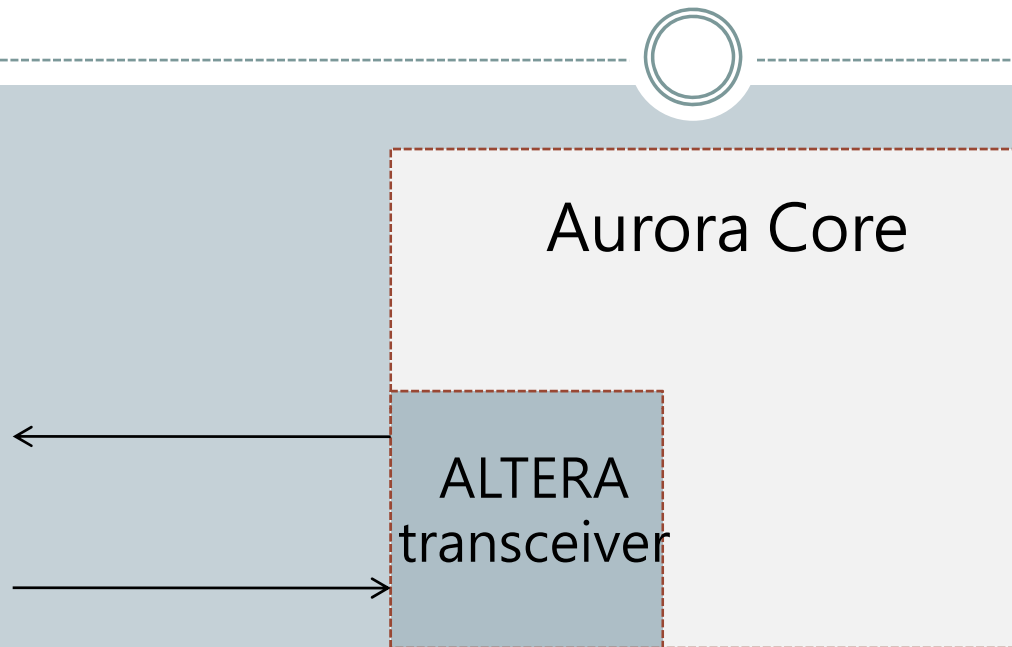
Test 2:



**WORKS!**



# Implement Aurora protocol in Altera



Core implementation:

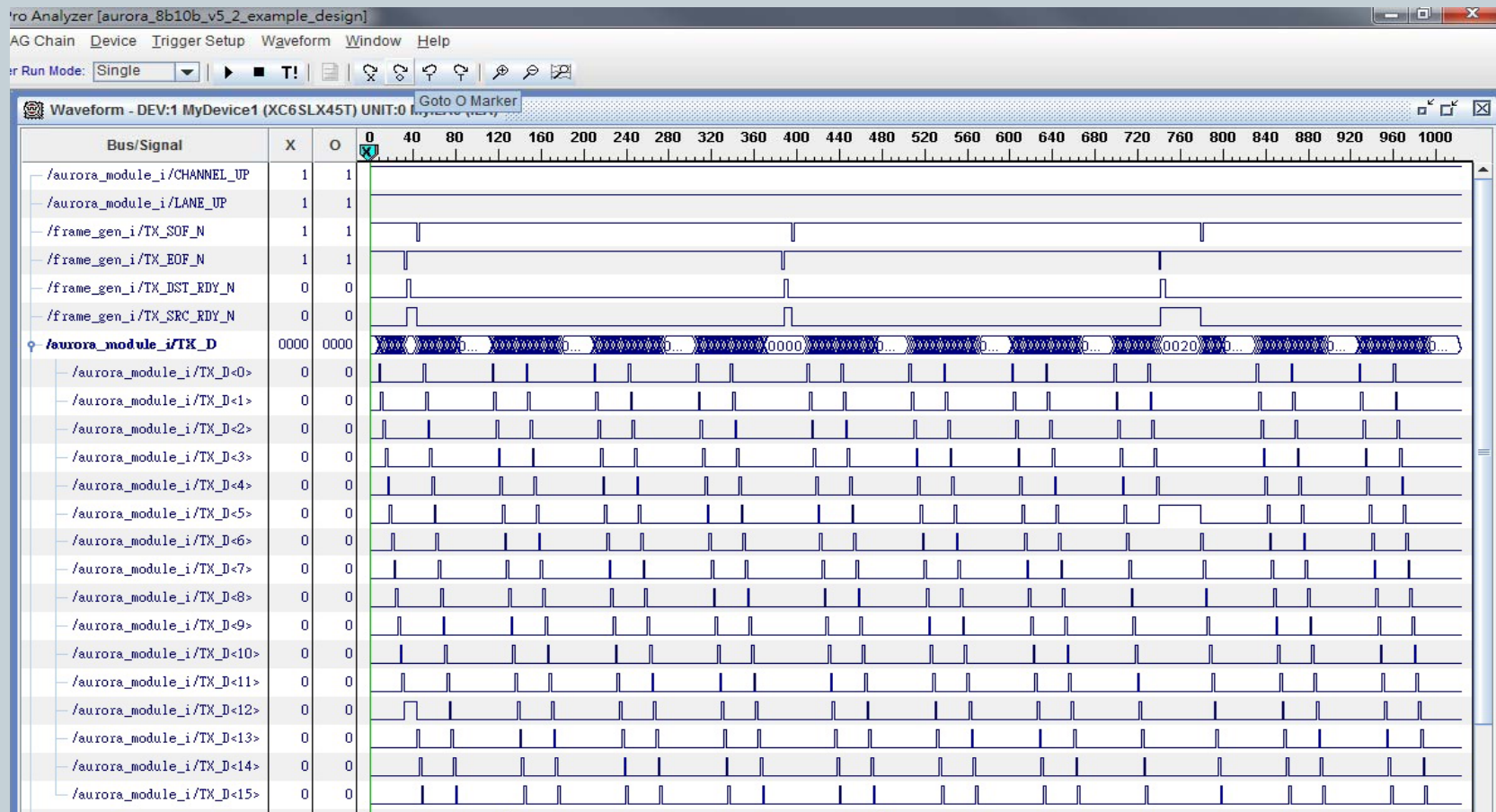
1. In Altera, construct the transceiver module with corresponding Aurora functions.
2. Replace the Aurora components used in XILINX transceiver( FDR, MGT...).

**It works at the first!** Need to test various requirements for Iwasaki san ...

- 1 : The user data rate from CDC front end for each channel.
- 2 : The algorithm to reduced the data in MERGER, rules,...

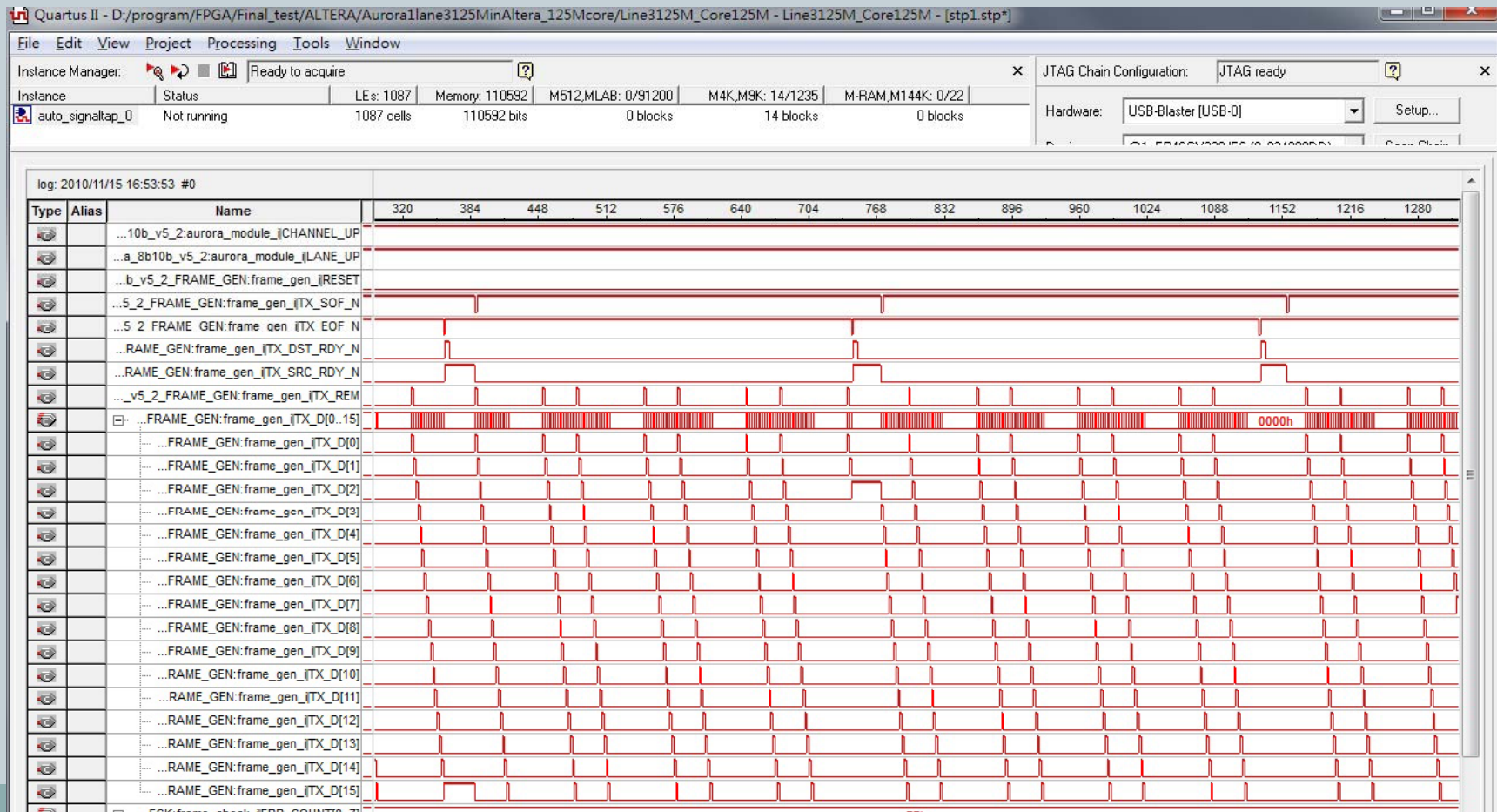
# Diagrams for Altera & Xilinx data link (Aurora)

- SP605 transmit and ALTERA receive

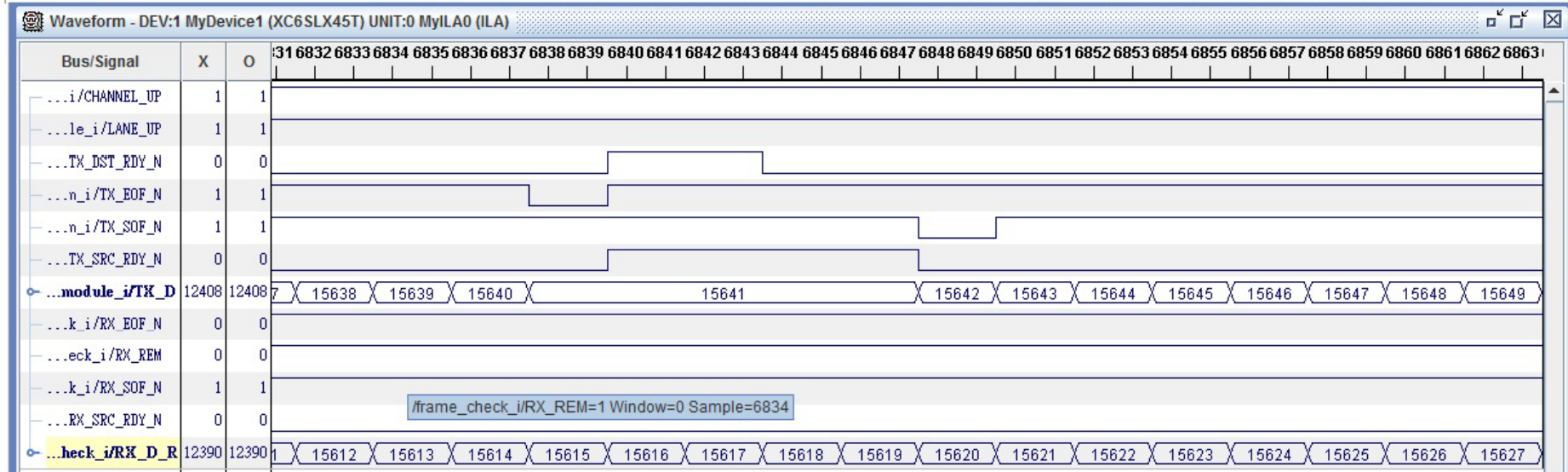
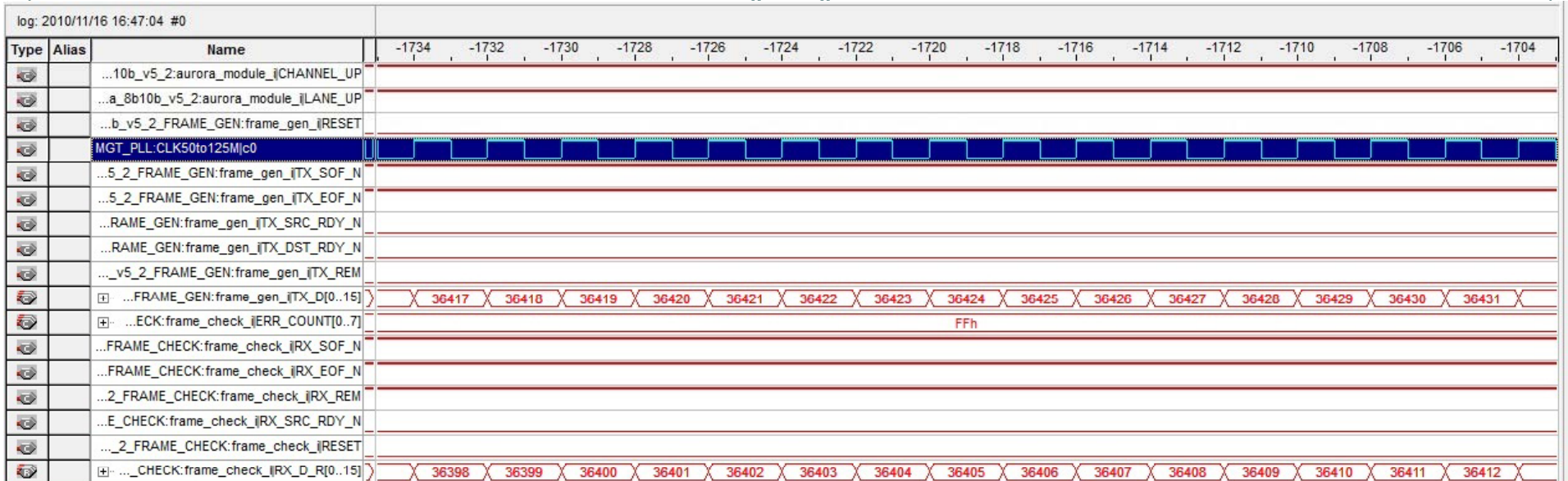


# Diagrams for Altera & Xilinx data link (Aurora)

- ALTERA transmit and SP605 receive



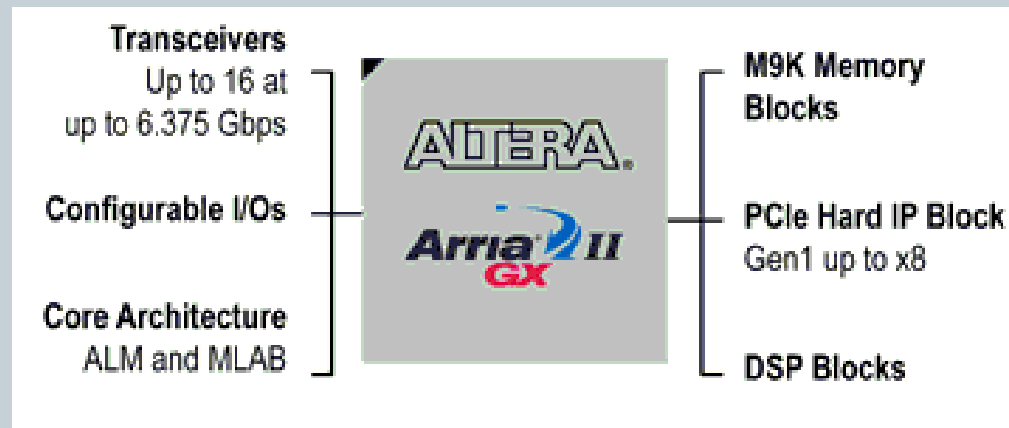
# Sending continuous data using Aurora



# Chips survey



- At present Altera chips: EP2AGX95EF29I3N
- transceiver: 12 pairs (6.375Gbps)
- price: 1120(USD)



# Summary



- Data link between Xilinx and Altera transceiver is tested.
- Aurora has been implemented in Altera.
- We has purchased a new virtex 6 development boards and will test more functions with that board.
- Board design and lay out will start after that...