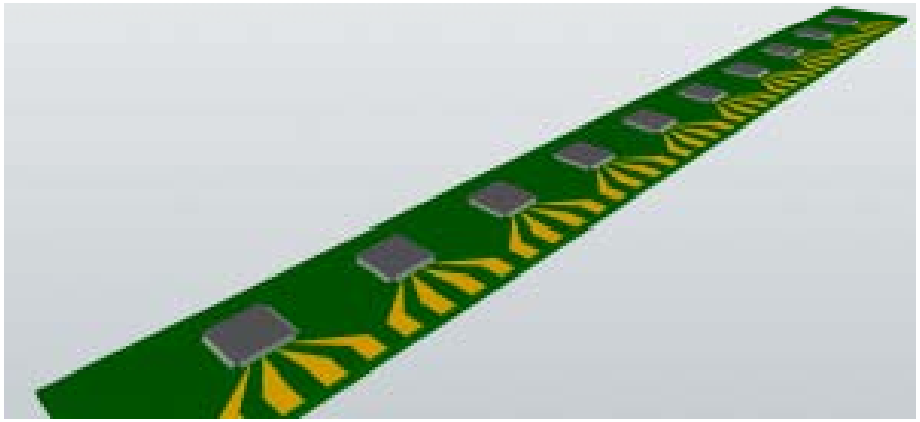
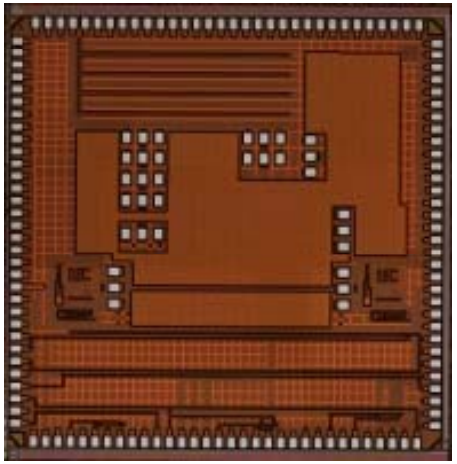
Electronics Overview

Gary Varner for the LAPPD Electronics Group

Year 2 Progress and Plans for Year 3

20-MAY-2011 Electronics GPC Review





Review of items raised last time (1)

1. It was not clear from the presentations how well the electronics development effort is integrated with other parts of the project. In particular, there may be interdependencies or requirements from other aspects of the project that could impact the electronics design, and it was not clear how this feedback and interaction are incorporated into the electronics design. The committee recommends that formal discussions with the various groups in the project be incorporated into electronics design process to ensure that there are no surprises during this second critical year, where the projects milestones show the development of an integrated device.

There has been much dialog and directly working together on items such as anode strip tests (Herve) and using prototype readout as part of characterization (Eric)

Review of items raised last time (2)

2. As a particular concern related to the above, it was not clear from the presentations how certain aspects of the electronics development meshes with the mechanical design. In particular, there were questions about the high voltage distribution inside of the photo-detector, signal flow and return paths, and the overall grounding scheme. Also, there were concerns about the sensitivity of the electronics to electrostatic discharge, such as sparks induced by high voltage. The committee recommends that the Electronics group and the Mechanical Group begin to develop a plan for how these two aspects of the project would be integrated to understand these issues, and to address any problems that might exist.

The high voltage distribution has been largely decoupled from the readout electronics effort. With first tiles, the degree to which noise and pick-up are issues will be an issue shall manifest themselves. Signal and current return being actively studied. ESD protection on chip input will be augmented with additional, external protection.

Review of items raised last time (3)

3. There were no presentations on system aspects, such as global clock distribution in a large detector array, system synchronization, and error detection/error correction. In particular, there are concerns as to how the front-end chip would recover from either data transmission errors or synchronization problems. The committee recommends that these be considered soon, as there may be aspects that will concern the design of the front-end chip.

Mircea will present the current plan for the first (beam test) readout system configuration. Worrying about some of these issues may be a bit premature, as we are still at an early prototype stage. Nothing in the design of the front-end ASIC precludes such synchronization and error detection, though that is envisioned to be largely the domain of the companion state-machine/event processing programmable logic.

Review of items raised last time (4)

4. There were no presentations on how the electronics would be calibrated, nor what aspects of the electronics will need to be calibrated. Some of the issues include identification of the corrections that might be needed, and how and where in the system they would be implemented. Several aspects discussed include time dependence corrections, amplitude dependence corrections, capacitor variations, clock phase corrections, etc. The committee recommends that the group begin to identify what kind of calibration techniques will be needed to address these, and how they might be incorporated into different levels of the data acquisition system. This plan should be a starting point, which evolves to include system issues, including the calibration of the physical detector, calibration of the front-end chips, and what role the back-end processing plays in the calibration process.

Kurtis has performed a number of calibration studies and will present a short synopsis of what constants and measurements are needed and the methodology to determine them. We have been exploring two paths for calibration/real-time correction and will present them today. Both use the same methodology.

Review of items raised last time (5)

5. Perhaps the most serious issue identified by the committee is the reversed stripline anode design. The signal attenuation at the end of the stripline is regarded as a serious concern. We are also concerned that impedance mismatch at the tile boundaries will cause reflection and/or attenuation of the signal. The group, along with Project Management, needs to resolve this issue soon, in case alternate strategies must be employed. In particular, a "conventional" stripline design might be needed, where the signal pick-off is on the inside of the plate, and signal pins would have to be inserted into the glass. This is a significant mechanical issue, which could impact the development schedule. We recommend that this be resolved soon.

The committee is right to be concerned and the problem is highly non-trivial. Fermilab RF expert Dave McGinnis has been brought on-board to provide guidance in the studies that will be presented today.

Review of items raised last time (6)

6. While the testing of the front-end chip is progressing well, the proponents did not present plans for testing the electronics with an integrated photo-detector. The committee recommends that the Electronics Group, along with Project Management, begin to develop a plan for such testing. It is not too early to do so, given the Year 2 milestones that are looming. In particular, some of the relevant tests include measurement of quantum efficiency, overall gain, gain and readout uniformities transit time uniformity, rate dependencies, etc. It was not clear how the new electronics would be used to test these aspects of the integrated device, nor what resources would be needed to do so. In a related aspect, the committee recommends that the group develops a contingency plan for testing both the electronics and an integrated device. In the event that there are delays in the development of the MCP or the photocathode of the large-area device. This may require planning with the MCP and Photocathode groups.

Performance limitations of the PSEC3 limited the usefulness of the initial tests with Matt and others. As will be presented today, we have taken this suggestion seriously and have made such contacts. Both test (eval) and full anode strip readout boards have been developed and will use multiple ASICs (PSEC4, IRS2, BLAB3A)

Review of items raised last time (7)

7. The committee is concerned that the electronics development does not have sufficient manpower resources to meet the Year 2 milestones and going forward. In particular, the areas identified that could benefit from additional resources include firmware development, software development, back-end design (DAQ), and overall system design. We recommend that additional resources be brought into the group, including students, postdocs, and engineers. The LAPPD project should also consider the addition of a system engineer to oversee the interfaces between different groups in the project.

While the group size has not increased, we have been very efficient with available manpower resources. A system engineer would be helpful, to coordinate the efforts.

Review of items raised last time (8)

8. The committee was very impressed with progress made with the design and development of the PSEC chip. While the development appears to be proceeding well, the proponents presented contingency scenarios for using other sampling chips in the event that the PSEC development has problems or would not be ready in time to meet Year 2 milestones. The committee recommends that the Electronics Group work with Project Management to identify a point in time when a decision will be made regarding which chip to go forward with to meet project milestones. That point would have to be within the next 3-6 months in order to be ready for test beam tests by the end of Year 2.

PSEC4 is our baseline ASIC. Given that it is a very conservative set of corrections to PSEC3, we have confidence it will be useable for the next round of testing. The alternate ASICs continue as fall-back options, should this not be true, and also for applications where a longer sampling depth, longer trigger latency, electronics gain, or some other project-specific requirement is needed. The electronics is modular and can accommodate different ASIC options with little additional effort.

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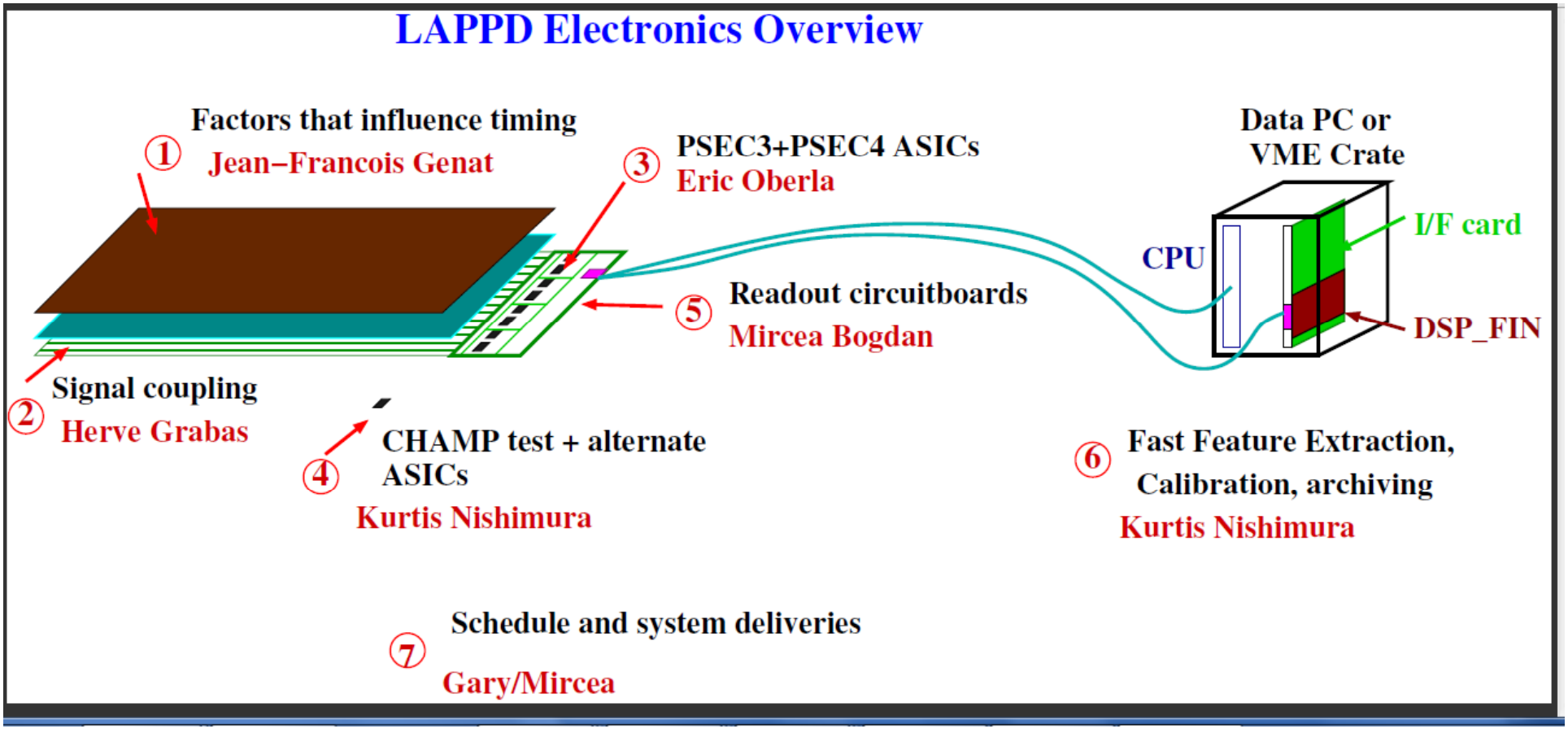

Initial systems all based on USB readout

Giga-bit fiber Tx/Rx for high rate/throughput

LAPPD Electronics and Integration Godparent Review

Friday 20 May 2011
from **08:00** to **18:00**UTC
at **Argonne National Laboratory (** ***Bldg 360, Rm A224*** **)**

Friday 20 May 2011 |

Suggest dropping 10:50 talk, making rest 30'

Friday 20 May 2011

top

08:00	Morning Refreshment	
08:30	Welcome (05')	Zikri Yusof
08:35	Overview (20')	Gary Varner
08:55	Review/update on physical parameters that influence timing (20')	Jean-Francois Genat
09:15	Signal development and coupling to Readout Electronics (20')	Herve Grabas
09:35	~~The PSEC3 ASIC (20')~~ → The PSEC3 and PSEC4 ASICs	Eric Oberla
09:55	Break	
10:10	~~Future ASIC Options (20')~~ → CHAMP lessons and alternative ASIC options	Matt/Kurtis
10:30	Readout System Overview (20')	Mircea Bogdan
~~10:50~~	~~Fast Feature Extraction/Data Reduction (20')~~ ← →	~~Matt/Gary~~
11:10	~~Data processing, Calibration and archiving (20')~~ → Fast feature extraction, Calibration, archiving	Kurtis Nishimura
11:30	Schedule, Plans and System deliveries (20')	Gary/Mircea ← ~~Jean-Francois/Gary~~
11:50	Open questions (20')	
12:10	Lunch	
13:10	Open discussion (if necessary) (30')	
13:40	Godparent Committee Discussion/Draft of Report (30')	

Schedule and System Deliveries

1. Matt's test system
2. Beam test stand
3. Chicago test stand
4. Hawaii x-ray FEL/ps laser
5. Others
6. Timescale??