A highly integrated photodetector module should include the requisite high-performance, compact and low-power signal recording electronics. The challenges and development strategy for fielding such a system are addressed in the following subsections.

0.1 The Electrical Circuit: from DC to GigaHertz

The ability to cover large areas and yet retain good time resolution, two attributes that are by nature exclusive to each other, depends on the introduction of transmission-line anodes with a time measurement (here implemented by waveform sampling) on each end [?]. Since the Micro-Channel Plates provide fast signals with rise-times on the order of a few hundreds picoseconds together with signal-to-noise ratios on the order of ten for single photo-electrons events, the propagation of these signals along anodes patterned as transmission-line can provide both picosecond timing and a fair position resolution below one millimeter in the two dimensions, using centroids. Moreover, as these transmission lines show almost no attenuation, it is possible to daisy-chain detectors and propagate signals on long distances keeping this position resolution. Figure 1

![Figure 1: 3 x 2 MCP tiles array and associated control and readout electronics](image)

Each strip line is composed of a pair of vertically spaced metal traces with dielectric in between the top and bottom strips. The impedance of the line depends only on the ratio of the width of the strip to the vertical spacing and the dielectric constant. We have chosen a 50-Ohm impedance for the strips and the input to the front-end waveform sampling chips. These ASICs are implemented in deep-submicron CMOS technology, allowing to record and digitize the pulse waveform for further signal processing extracting accurately charge and time upon a system or a channel trigger. The clock distribution relies on a central system clock distributed through an optical fiber system and local jitter
cleaner units close to the sampling ASICs. At each end of the detectors, FPGA devices manage the front-end ASICs in terms of distribution of control and calibration, trigger and readout, signal processing of the digital data, and interface to the data acquisition system. Time and amplitude calibration are performed switching to the anodes known charges stored in local precision capacitors. The pulses propagated through the transmission lines are recorded at each end and recorded in the same way as actual Micro-Channel Plate signals, providing accurate amplitude and time response allowing calibrating the Front-end ASICs gain, bandwidth, and the transmission lines propagation velocity.

0.2 The Signal Path and the 'Inside-Out' Anode

The anode shown in Figure 2 consists of a top layer and bottom layer of transmission-line strips, with glass in-between. The width of the traces, thickness of the glass, and glass dielectric constant are all such that the lines are 50 ohms at a few GHz.

In the ‘inside-out’ design we have shorted all the lines together on the top of the glass (i.e. the vacuum side) as shown in Figure 3 so that the sidewall frame can be bonded to a homogeneous silver surface, rather than having to cross the strips. The strips on the bottom layer are thus the ‘signal’ and those on top are the ‘ground’ for the signals on the lines, which are looked at differentially by the front-end chips at the ends of the lines ¹. The bottom trace then can be on the top surface of the ‘Tray’ rather than on the bottom surface of the tile, so that there are no signals that need to brought out of the vacuum volume of

¹This is analogous to grounding the center conductor of a long cable and floating the braid—one still sees the differential signal at the end of the cable, although inverted.
the tile. One only has to connect the grounds tile-to-tile or tile-to-tray, and this can be done with a resistive layer (and/or even inductive, see below) connexion along the tile edges.

Figure 3: The ‘ground’ anode traces in the ‘inside-out’ design, showing the interconnection between the traces under the sidewall (see Detail A). The interconnection has a mechanical function, preventing a direct path for vacuum leaks through the bottom seal along the strips. Electrically it provides a dead short DC connection for the ‘ground’ side of the signals, while at RF frequencies the lines function independently as the top traces of their transmission strip lines pairs.

The bottom line here (no pun intended) is that no signals need to be brought out through the sidewalls or back plate- the tile needs only to be stuck down on the tray. The signal path is thus very simple to construct.

0.3 The ‘No-Hands’ High Voltage Current String

This note is to suggest a similar solution for the HV current path, with the HV transmitted to the photocathode and the four MCP electrode surfaces by metalization on the bottom side of the window (i.e. the vacuum side). The ground is the same ground as the signal, which is differential with respect to it to ameliorate power-supply common mode noise.

Figure 4 shows a side-view of the stack-up of the MCP layers. Gap 1 is at the top (Photocathode to MCP1-In), and Gap 3 is at the bottom (MCP2-Out to Anode).
0.3.1 The Proposed Integral Resistor/Capacitor Chain

Figure 5 shows the circuit diagram for the HV. The design requires that resistors and capacitors in each gap be integral to the spacers; we do not know if this is possible, but are hopeful that this can be done using ALD \[2\]. Note that C3 stiffens the HV string at the point of highest current, after MCP2 where the gain is largest by a factor of 1000 \[2\]

0.3.2 Sample Calculation of Resistor Values for the Current Supply Chain

Suppose we desire the capability of a 1 MHz rate in an 8"-square tile, i.e. 16kHz/in-sq, with a 100 mv output pulse of width 1 nsec, driving 50 ohms (this is very conservative, as the output pulses will be smaller). The average current is then:

\[
I = (Rate)(I_{pulse})(\Delta t)
\]

\[
I = (1MHz)(0.1V/50ohms)(1nsec)
\]

\[
I = 10^6(2 \times 10^{-3}) \times (10^{-9}) = 2 \times 10^{-6}Amps
\]

We would like the string to carry 10 times this peak average current of 1 μA, i.e. we need a supply string capable of supplying at least 20 μA.

Taking Ossy’s recommendation for 10 MΩ for the MCP resistance (8" by 8") as a starting point, and a nominal operating voltage for a single MCP plate of

\[2\] We note that in a conventional PMT the voltage divider is stiffened for the last dynodes; in a two-MCP PMT as described here MCP2 has a gain of about 1000, comparable to the last 6-10 dynodes in a PMT.
1 KV for convenience of calculation, we find the current through the MCP to be

\[ I = \frac{V}{R} = 10^3 / 10^7 = 10^{-4} = 100 \mu A \] (4)

which satisfies the current requirement by a factor of 5.

We can then calculate the resistance of each element in the string. There are a number of considerations on the gaps and voltages that can be determined by simulation and confirmed by measurements:

1. The simplest solution for the spacers is to have the spacers in each of the 3 gaps to have the same resistance per length. This allows doing all the spacers in the same batch, presumably our best chance to have them all have the same resistance and the most uniform behavior versus other factors such as temperature, aging, contaminants;
2. A higher voltage and shorter path in Gap 1 should result in a lower TTS [?];
3. A higher voltage in Gap 2 results in fewer pores being illuminated in MCP2, and hence a lower gain (fewer saturated pores) but narrower distribution (all pores saturated) [?];
4. A larger Gap3 and lower voltage spreads the charge out over more strips, possibly allowing better uniformity.

The HV chain starts with an external connection (outside the vacuum) to the metalization on the bottom side (inside the vacuum) of the top window (see Figure 4). Table 0.3.2 gives the height, voltage, and resistance in each element.
For simplicity now we will take the spacers to have the same resistance per unit length.

<table>
<thead>
<tr>
<th>Name</th>
<th>Height</th>
<th>V</th>
<th>I</th>
<th>( R_{\text{Tot}} )</th>
<th>( N_{\text{spacer}} )</th>
<th>( R_{\text{spacer}} )</th>
<th>( \kappa )</th>
</tr>
</thead>
<tbody>
<tr>
<td>G1</td>
<td>1.0 mm</td>
<td>200 V</td>
<td>100 ( \mu )A</td>
<td>2 M( \Omega )</td>
<td>25</td>
<td>50 M( \Omega )</td>
<td>5000 ( \Omega )-cm</td>
</tr>
<tr>
<td>MCP1</td>
<td>1.2 mm</td>
<td>1200 V</td>
<td>100 ( \mu )A</td>
<td>12 M( \Omega )</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>G2</td>
<td>0.5 mm</td>
<td>100 V</td>
<td>100 ( \mu )A</td>
<td>1 M( \Omega )</td>
<td>25</td>
<td>25 M( \Omega )</td>
<td>5000 ( \Omega )-cm</td>
</tr>
<tr>
<td>MCP2</td>
<td>1.2 mm</td>
<td>1200 V</td>
<td>100 ( \mu )A</td>
<td>12 M( \Omega )</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>G3</td>
<td>2.5 mm</td>
<td>500 V</td>
<td>100 ( \mu )A</td>
<td>5 M( \Omega )</td>
<td>25</td>
<td>125 M( \Omega )</td>
<td>5000 ( \Omega )-cm</td>
</tr>
<tr>
<td>Total</td>
<td>6.4 mm</td>
<td>3.4 KV</td>
<td>100 ( \mu )A</td>
<td>32 M( \Omega )</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>

Table 1: The dimensions of the elements in the current string, shown in Figure 4. Gap 1 (G1) is the photocathode-MCP1\(_{IN}\) gap, Gap 2 is between the 2 MCP plates, and Gap 3 is the MCP2\(_{OUT}\)-Anode spacing. Each gap has 25 spacers made of 3-mm diameter glass rods, coated with ALD to achieve the resistance \( R_{\text{spacer}} \) per spacer and hence a parallel resistance of \( R_{\text{Tot}} \). The last column, \( \kappa \), is the ALD sheet resistance in \( \Omega \)-cm.

Figure 6: The dimensions of the two kinds of spacers- Gaps 1&2 and Gap 3.

Figure 6 shows the dimensions of the two kinds of spacers- Gaps 1 and 2, and Gap 3. Both are made from glass rod cut into precise lengths; the rod should be (more-or-less) CTE matched to the glass window and anode.

A quick approximate calculation of the ALD sheet resistance on the sides of the cylindrical spacer follows. The resistance of the spacer is given by:

\[
R = \kappa L/A = \kappa L/(\pi td)
\]  

where \( L \) is the length, \( A \) is the area of the resistive layer, \( d \) is the diameter of the spacer, and \( t \) is the thickness of the resistive layer. Putting in typical spacer values of \( L = 0.1 \text{ cm} \), \( d = 0.3 \text{ cm} \), \( t = 100 \text{ nm} = 10^{-5} \text{ cm} \), and \( R = 50 \text{ M}\( \Omega \) (see Table 1), we find the sheet resistance is

\[
\kappa = RA/L = R(\pi td)/L = 5000 \text{ \( \Omega \)-cm}.
\]  

6
0.3.3 Capacitor Values for the Current Supply Chain

In a photomultiplier one typically stiffens the last several stages with increasingly large capacitors, and also has a cap across the HV-to-ground total string. In this MCP design we have effectively only two stages, and so it is only the second MCP that needs the stiffening. Each spacer adds local capacitance, with the total being the sum of the parallel caps.

There are two functions of these caps:

1. stiffening the string so that the DC voltage doesn’t dip after a pulse, and
2. providing an AC high-frequency return path for the fast pulse to diminish ringing (bypassing) [?].

**Stiffening- Storing locally distributed charge** The charge in a single pulse is

\[ I\Delta t = 2 \mu A \times 10^{-9} = 2 \times 10^{-15} \text{Coulombs} \]  

(7)

If we want to have charge for 1000 pulses stored locally, i.e. \(2 \times 10^{-12} \text{Coulombs}\), we need a capacitance of

\[ C = \frac{Q}{V} = \frac{2 \times 10^{-12}}{1000} \text{Coulombs} = 2 \times 10^{-15} \text{Farads} = 2 fF \]  

(8)

which is tiny, and at the macroscopic level of the spacers is already supplied by the MCP plates.

**Bypassing** We have had good success with bypassing the perimeter of the 2” Planacon with 3 capacitors per side, connecting the anode to MCP2-OUT. Each capacitor is 100 pf [?], and as they are small they are very low inductance. If we can make each spacer a capacitor we will have distributed bypassing capacitance.

0.4 Tolerances

0.4.1 Tolerances on the Resistance Values of the MCP’s and Spacers

The relative resistances in the HV divider string shown in Figure 5 determine the voltages across the MCP’s and gaps. As the sheet resistance between the spacers and the MCP’s is different, the ALD process breaks up into two separate runs, one for the spacers and one for the MCP plates. There is no gain in the gaps, and we believe the dependence on the voltage is mild (simulation and measurements will eventually tell us if this is so). The MCP’s, however, have a strong dependence of gain vs voltage, typically a factor of 1.7 per 100V at 1.6KV [?]. Consequently the resistances of the two MCP’s should be matched. For a 10% difference in gain from MCP1 to MCP2, the two should have an overall resistance difference less than 1% (18V out of 1.6KV gives a 10% gain change). Tests will show whether or not the resistances of the two plates track with temperature and use.

In summary, the tolerance for the absolute resistance of the spacers is 10-20%, and is not critical. The relative resistances for the spacers should be the
same within 10%, and as they are made in the same batch, this should not be a problem. The tolerance on the average resistance for the MCP's is also not so critical, e.g. 10%. However in this scheme the two MCP’s should have the same resistance within 1-2%, which is tight.

0.4.2 Tolerances on the Capacitance Values
The tolerances on the capacitances are very loose- up to 50% even would be acceptable. Whatever is natural for the process we can accept; it would, however, be good if all the capacitors in a single batch come out the same within 10%, for example.

0.5 The Window and Anode HV Path Patterns
The pattern on the inside of the window, shown in Figure 7, serves three functions: 1) it provides a uniform metal surface for the top seal between the sidewall and the window; it distributes HV across the large photocathode so that there is no voltage drop in the PC itself; and 3) it distributes current to the resistive spacers that form the HV string to ground, providing current for the MCP amplification.

Figure 7: The electrode patterns on the window (left) and top of the anode (right).

0.6 Alternative Anode Patterns
The mechanical design of the tile is flexible, and allows alternative anode patterns with different cross-talk, analog-bandwidth, return path impedance, and risetimes, allowing optimization for different applications. Figure ?? shows a conceptual design for an anode designed to have less cross-talk and better bandwidth, as well as a lower-impedance return (although at some cost in amplitude), using coplanar strip lines.
0.6.1 Resistive/inductive anode grounding.

An optimized termination pattern such as shown Figure 7 could be implemented keeping a plane tile-to-tray interface. Figure 15 shows the Spice simulated amplitude distribution obtained along a strip when the anodes are tied to ground at the strip ends by a zero impedance. The signals disappears a moving the source close to the strips ends since propagation cannot (or partly) take place on a distance less than the product of the rise-time by the propagation velocity. Implement resistive/inductive terminations could overcome this issue. Figure ?? shows the amplitude distribution obtained with a 15 Ohms (strip to strip) and 20nH (strip to end) termination.

0.7 Electrical Characteristics of Transmission-Line Anodes

0.7.1 Tray-Tile Strip Lines

The strip lines are implemented in a scheme that enables simplification of the mechanical construction of the hermetic vacuum assembled, the ‘Inside-Out’ construction. In this scheme the top trace of each strip line is inside the 8”-square vacuum assembly (the ‘tile’) that contains the photocathode and the two MCP’s as well as the anode plane of top strips, as shown in Figure ?? in Section ???. The bottom plane of strips is on a separate printed circuit board that runs the length of three tiles, and onto which the tiles are laid. There are no electrical connections between the tiles and this circuit board.

The PC card that contains the lower traces terminates on each end in two 8”-long narrow cards, the ‘analog board’ that interface the lower strips and the ground connections to the front end chips, as shown in Figure ?? in Section ???. We refer to the system of the PC card, the analog cards, and the digital card that handles controls and clock, as well as the honeycomb support structure, as ‘the tray’. A SuperModule consists of six tiles mounted to the tray, and thus has an optically sensitive area of 16” by 24” (40 cm by 60 cm).

0.7.2 Anode Electrical Characteristics

The goal of precision timing requires a level of understanding of the formation and propagation of signals on the anode beyond the present literature. A major goal of the LAPPD project is to develop this understanding and capture it in a detailed simulation so that we can optimize for different applications. We describe the relevant attributes below.

Analog Bandwidth  Figure ?? shows the measured transmission transfer function, i.e. the ratio of the signal measured at the end of the line versus the input signal, as a function of frequency for an silk-screened 8”-tile anode. The 3db point is at 2.4 GHz, as expected from a simulation of the anode using the Ansoft HFSS package [?]. We note the good agreement (the fine structure in the measurements is related to the details of the signal injection and measurement probes, and will be better with the ASIC layout).
Figure 8 shows the time resolution versus analog bandwidth (ABW) of the anode and input to the waveform sampling ASIC at a sampling speed of 10 and 20 and 40 GS/sec. For very large area applications, such as LBNE, psec time resolution is neither possible nor necessary, and the lower analog bandwidth associated with long silk-screened anodes (e.g. 1.1 GHz) is more than adequate. For very precise timing such as would be desirable at a collider one can go to higher quality anodes and shorter strips, with a consequent higher ABW.

![Figure 8: The time resolution versus analog bandwidth at 10 and 20 GS/sec.](image)

**Impedance**  The impedance of the transmission lines is set by two parameters, the ratio of the strip width to the top-bottom line separation, $w/d$, and the dielectric constant of the glass. The top-bottom separation in the present (generic) design is set by the thickness of the glass tile bottom, which we have chosen to be 0.106”, the thickness of the readily-available and inexpensive 2.75mm Schott B33 glass. The quoted dielectric constant of B33 is 4.6 at 25C and 1MHz [?]

- Microstrip line
Figure 9: Characteristic impedance of a microstrip line

- Coplanar line

\[
Z_{\text{meas}} = \frac{2Z_0}{\sqrt{\beta (\beta + 1)}} \left( \frac{\beta + 1}{\beta + \frac{1}{\beta} \tan \phi} \right) \left( \frac{\tan \phi}{\beta + \frac{1}{\beta} \tan \phi} \right) \left( \frac{\tan \phi}{\beta + \frac{1}{\beta} \tan \phi} \right)
\]

where \( Z_0 \) is the impedance of lossy space (first cylindrical) and \( \tan \phi \)

\[
S_{\text{rad}} = \sqrt{\frac{1 + \frac{1}{\beta^2}}{1 - \frac{1}{\beta^2}}}
\]

Figure 10: Width of the strips of a coplanar line for a given characteristic impedance.

Figure 11 shows the measured impedance of a silk-screened anode plate (left panel) and the measured dielectric constant (right panel), versus frequency up to 5 GHz. The measured impedance is 50 Ohms, as intended, constant over a wide range of frequency; the structures at high frequency are due to the details of signal injection and extraction in the test setup, as can be seen in the right hand plot where the dielectric coefficient is constant over the full frequency range.

**Propagation Velocity** The measured phase delay and group delay on an 8” silk-screened glass anode are shown in Figure 12 versus frequency. Note that the value of the cut-off in group delay is higher than the 2.4 GHz measured in Fig. ??, a sign that pulse timing measurements may be better than one naively would expect from ABW alone. The velocity, 0.48c agrees well with the
Figure 11: The measured impedance of a silk-screened anode plate (left panel) and the measured dielectric constant (right panel).

calculated value for the 0.29m length in the test setup.

Figure 12: The measured phase delay and group delay on an 8” silk-screened glass anode versus frequency.

Cross-Talk  Figure 13 shows a simulation of the cross-talk between a strip and the three nearest neighbors. We note that the cross-talk is helpful, as long as there is not a rate problem, in finding the centroid of the pulse, as all the strips are digitized.

Figure 14 shows measurements of the cross-talk on a neighboring strip at the far end from the signal injection. The sign and magnitude agree with the simulation [?].

Attenuation and Uniformity  Figure 15 shows simulation results on uniformity (needs updating for JF’s new results xxx).
Figure 13: A simulation of the cross-talk between a strip and the three nearest neighbors.

Figure 14: Measurements of the cross-talk on a neighboring strip at the far end from the signal injection. The sign and magnitude agree with the simulation.

0.8 The Analog Boards

Figure 16 shows the Analog Board, the simple PC card that supports and interfaces to the waveform-sampling ASICs. These are soldered onto each end of long PC lower anode card.
0.8.1 Impedance Matching to the Front-End Chips

Figure 15: Simulation results on uniformity versus position across the anode.
(need JF update xxx)

Figure 16: The Analog Board, the simple PC card that supports and interfaces to the waveform-sampling ASICs.

Figure 17 shows the impedance matching of the transmission line strips into the pads of the wave-form sampling ASICs.
0.9 Front-End Chips (The PSEC ASICs)

We have chosen the IBM 130nm CMOS 8RF process as the basis for the front-end waveform sampling ASICs, a smaller (and hence faster) and more modern process than the 250nm and 350nm processes used in the pioneering waveform sampling chips [?].

The left-hand panel in Figure 18 presents the specification for the current round of waveform sampling ASIC (PSEC3). The right-hand panel gives a tabulation of the various operating and triggering modes for the chip.

A block diagram and floor plan of PSEC3 are given in Figure 20 and Figure ??.

The previous version ASIC, PSEC2, is shown mounted on an initial test card in Figure 21. This chip achieved a sampling rate of 11 GS/sec, but the ADC readout was compromised by leakage; detailed testing is underway while PSEC3, which has the fixes and other improvements, is being fabricated.

0.10 The Digital Board

Figure 22 shows a proto-type of the Digital PC card that receives the digitized data from the ASICs on the Analog Boards.

0.11 DAQ, Clock Distribution, and Slow Control

The digital board will connect to the DAQ system via a Giga-bit serial link that handles the data from the 80 strips per SuperModule. In addition, prototypes will have a USB connector for simple debugging. The digital boards are set up so that they can be daisy-chained for low-rate applications, allowing flexibility in the number of channels per data collector and in the system layout. Initially all tests will be done using USB directly to a PC; we will then move to a fast serial link using commercial receiving modules.
Figure 18: Left: The specification for the current round of waveform sampling ASIC (PSEC3). Right: A tabulation of the various operating and triggering modes for the chip.

<table>
<thead>
<tr>
<th>Channels</th>
<th>Input 1 + Input 2 + Timing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling rate</td>
<td>10-20 GHz</td>
</tr>
<tr>
<td>Analog Bandwidth</td>
<td>1-2 GHz</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>800 mV</td>
</tr>
<tr>
<td>Sampling window</td>
<td>40 ns - 500 ns (or 6 delay cells)</td>
</tr>
<tr>
<td>Sampling jitter</td>
<td>15 ps</td>
</tr>
<tr>
<td>Cost</td>
<td>1%</td>
</tr>
<tr>
<td>DLL Timing generator</td>
<td>Internal phase comparator and charge pump, external DLL filter</td>
</tr>
<tr>
<td>DC input impedance</td>
<td>50 ohm internal, 50 ohm external</td>
</tr>
<tr>
<td>Conversion clock</td>
<td>Adjustable 100 MHz to 200 MHz internal clock oscillator</td>
</tr>
<tr>
<td>Read clock</td>
<td>Maximum conversion time 8 ns</td>
</tr>
<tr>
<td>Power</td>
<td>480 W/channel</td>
</tr>
<tr>
<td>Power supply</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Process</td>
<td>IBM 0.8 μm CMOS</td>
</tr>
</tbody>
</table>

Figure 19: A block diagram of PSEC3.

The clock distribution system consists of a master 500 MHz clock, which is fanned out to the digital boards using the a TI multi-channel jitter cleaner and
Figure 20: the floor plan of PSEC3 showing the timing generator feeding six channels of sampling arrays (four regular, one for tests, and one for time calibration), and the two token passing readout controls.

clock distribution chip [?]. The clock will be ‘cleaned’ locally on each digital card. From tests and specs we expect to be able to hold a channel-to-channel jitter of 1-2 psec in one SuperModule, and a module-to-module jitter of 2-3 psec. We expect that calibration to better than this can be done locally; for
example, in a collider environment photons from pizero decays can be used as the local time base on an event-by-event basis, so that one is only measuring the difference in arrival times between photons \((v = c)\) and charged particles.

The one application we are presently working on that requires psec resolution, i.e. better than this, is TOF at high-energy colliders such as the Tevatron, LHC, and ILC. Rather than relying on achieve psec resolution on a big system over long periods of time, we propose to ‘self-calibrate’ by measuring the difference in arrival time on an event-by-event basis between photons, of which there are many, and the charged particles to be identified. The method can be checked with electrons and muons, which are identified by conventional collider means, and is under study by simulation now.

## 0.12 Analysis and Diagnostic Software

The SuperModule system design was chosen to put substantial analysis capability at the front-end, so that sparsified calibrated data are all that are regularly shipped ‘upstairs’ from the supermodules themselves. Calibration, local removal of ‘hot-spots’, book-keeping of hot-spots and dead-spots, and other data-intensive operations will be done locally in the FPGA.

The read-out will be by fiber, with USB available for local diagnostics and debugging. The digital cards are designed to be daisy-chained, with both input and output optical connectors, so that a single design can cover a wide-range of required DAQ band-widths for typical applications \([?]\). Systems using commercially available hardware are being worked on at both Chicago and Hawaii; Figure 23 shows a set of Hawaii optical fiber transmitter and receiver boards (both institutions have a lot of experience with large DAQ systems and fast readout; the specs in most near-term applications, even including PET, are
easily met by these systems.)

Figure 23: A set of Hawaii optical fiber transmitter and receiver boards as an example of available hardware that easily meets the specs for most applications, even including PET.

0.13 Expected Performance

Figure 24 shows the expected performance versus number of photo-electrons for a 20 GS/sec sampling rate and a 1.5 GHz analog bandwidth.

Figure 24: The expected performance versus number of photo-electrons for a 20 GS/sec sampling rate and a 1.5 GHz analog bandwidth. (note- wrong plot-new plot on way)