July 7, 2011

Dear Electronics Group Godparents,

The electronics group wishes to thank the Godparent Committee for their thoughtful comments and recommendations following the Electronics Godparent Review of May 20, 2011. We have below both their original recommendations and our responses in an effort to document our plans for moving forward both with regard to the specific suggestions and in general for the future.

Best Wishes,

Electronics and Integration Group

LAPPD Electronics and Integration Godparent Review - 05/20/2011

Attending Members: Igor Veryovkin, Bernhard Adams, Dave McGinnis, Steve Ross, Zikri Yusof (Chair).

A Godparent review of the Electronics and Integration effort within the LAPPD Collaboration was conducted on the 5/20/2011. The committee members once again congratulate those involved in this effort for the tremendous progress made and thank them for their presentations during the review. Issues raised based on the review are listed below:

[**Q:1**] Management issue : The committee urges the collaboration to make an attempt at listing some form or requirements and specifications that can be loosely denoted as goals, even if it is phased. This will allow for the demonstration of a "success".

[**A:1**] As a baseline goal, we adapt those of the orginal milestones as follows: demonstration of a sampling and digitizing ASIC with a sampling rate $\geq$ 10 gigasamples per second, $<$ 1 mV of noise, and $\geq$ 1 GHz of analog bandwidth. The existing PSEC3 ASIC meets the first two of these specifications, and the PSEC4 is expected to meet all three. As is implied by the committee's suggestion of phased goals, we also recognize that this field is much richer than any simple set of specifications can adequately represent. As such we also intend to explore the ultimate limits of timing precision, toward 1 picosecond and below.

[**Q:2**] A list of different applications and design trade-off can be useful. This list can be part of the collaboration's database and can be updated if necessary.

[**A:2**] We entirely agree, and as a starting point have prepared a table of various waveform sampling/digitizing ASICs and their properties. **(STILL NEED TABLE HERE... from Stefan Ritt's talk? Couldn't find the one Henry referred to...)**

[**Q:3**] Manpower concerns - Current funding is via Argonne subcontracting to UofC and

UofHawaii. Universities bring special advantages, but committee is concerned about long-term stability of the electronics effort.

[A:3] We also share the concerns of the committee. As the committee points out, university groups have advantages that make them particularly well suited to exploration and innovation. As we move toward larger production quantities and integrated assemblies, we hope to bring Argonne more closely and directly into the effort.

[Q:4] Review milestones and update whenever appropriate.

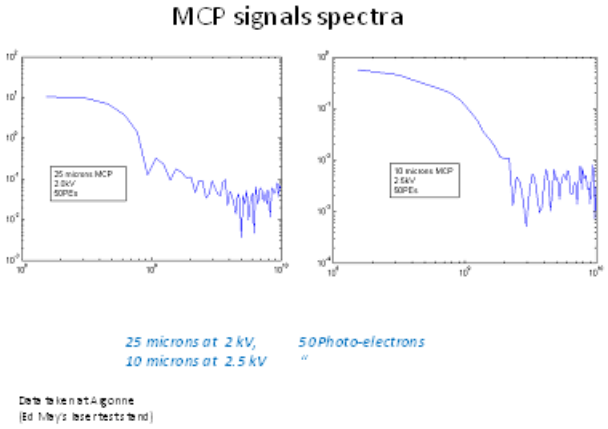
[A:4] We have prepared **(will prepare?)**, as part of the technical design report, a set of milestones for moving forth with the electronics effort. In addition to the ASIC-specific targets that have been previously mentioned above, these milestones are steps toward a full integrated readout system, and are briefly summarized here, organized into three main categories.

- Hardware
  - Design and fabricate hardware for small evaluation systems based on a single PSEC3 or PSEC4 ASIC.
  - Design and fabricate hardware to accommodate the readout of a single 8"x8" tile with PSEC3 or PSEC4 ASICs.
  - Design and fabricate hardware to accommodate the readout of a 2x3 panel of 8"x8" tiles with PSEC3 or PSEC4 ASICs.
- Firmware
  - Upgrade existing FPGA code to handle multiple/hierarchical control and data flow to support multiple PSEC3/PSEC4 based systems.
- Data Acquisition Software
  - Prepare DAQ software to control and readout PSEC3 4 channel evaluations boards. Support several small DAQ systems for testing 8"x8" MCP devices.
  - Prepare DAQ software to control and readout of 80 and 160 channel systems to support up to 2x3 panel of 8"x8" MCPs use in laser, cosmic ray and particle beam teststands.
  - Prepare Offline analysis software to analyze and archive data and results from above teststands.

[Q:5] Measure the bandwidth of the MCP pulse.

[A:5] We concur that is essential to get an accurate measurement of MCP pulse bandwidth. Previous measurements, shown below, have been performed using a laser 10 and 25 micron Planacon devices, and indicate a bandwidth of roughly 1.3 GHz. An immediate, concerted effort is now underway to measure the bandwidth of the MCPs intended for use in the 8"x8" devices.

[Q:6] Specify where they think the future bandwidth/rise time should be.



[**A:6**] We agree that this should be clearly specified. This specification will be carefully considered after the bandwidth of the MCP pulse is better known.

[**Q:7**] `Examine the trade off of anode bandwidth to spacing.`

[**A:7**] Studies are currently planned to investigate this issue specifically, as part of the larger set of anode studies being conducted by Hervé Grabas.

[**Q:8**] `Hervé Grabas has done a great job on the interconnects from the anode board to the waveform sampling chips. However, in transitions between different types of dielectric substrates and stripline types, it becomes very challenging to ensure good impedance match across a wide bandwidth. More engineering effort will be required here. In order to gauge the amount of effort required for this, we need to know the bandwidth of the pulses to be transmitted (see Item 6).`

[**A:8**] We recognize the committee's concern on this subject and agree that the design of high bandwidth anodes will be significant and challenging. We intend to continue to utilize the expertise of Dave McGinnis and make as much progress as possible on this front.

[**Q:9**] `Lower the input capacitance of the next generation ASIC chip by at least a factor of 2 from the PSEC-3 design. The committee would like to complement the ASIC design team for continued good work, and clear communications.`

[**A:9**] The PSEC4 ASIC has been designed with this goal in mind, and measurements will be conducted to verify the reduced capacitance and corresponding improvement in analog bandwidth when the chip returns from fabrication this fall.

[**Q:10**] `Evaluate work done so far for possible publication. Also continue to evaluate that all this work feeds into student dissertations.`

[**A:10**] We agree with the committee wholeheartedly. Papers are currently in preparation on both the PSEC3 ASIC as well as the anode studies conducted by Hervé Grabas. It is expected that the material on both the ASICs and the anode studies will appear in the dissertations of Eric Oberla and Hervé Grabas.