The CHAMP ASIC and ASIC Options

Kurtis Nishimura
University of Hawaii
LAPPD Electronics Godparent Review
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A bit of context…

- Hawaii (Gary) has a lot of ASIC experience with TSMC 0.25 μm.
  - As of beginning of last year, no direct experience with IBM 0.13 μm.
- Most waveform sampling/digitizing ASICs are in larger processes ($\geq$ 0.25 μm) …

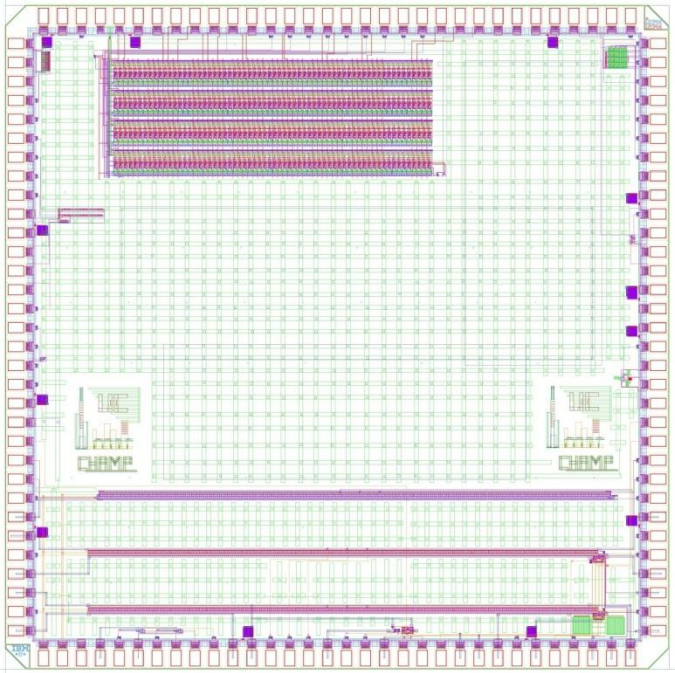
ASIC	Amplification?	# chan	Depth/chan	Sampling [GSa/s]	Time resolution	Analog BW	**Vendor**	**Size [nm]**	Ext ADC?	Cost
PSEC3	no.	4	256	1-16	TBD	TBD	**IBM**	**130**	no.	55k?
DRS4	no.	8	1024	1-5	10's of ps		**IBM**	**250**	yes.	? ? (ADC also)
SAM	no.	2	1024	1-3	10's of ps	350MHz?	**AMS**	**350**	yes.	? ? (ADC also)
IRS2	no.	8	32536	1-4	TBD	>= 1GHz	**TSMC**	**250**	no.	$ 47,500
BLAB3A	yes.	8	32536	1-4	TBD	350MHz	**TSMC**	**250**	no.	$ 47,500
TARGET	no.	16	4192	1-2.5	<40ps	150MHz	**TSMC**	**250**	no.	$ 41,500
TARGET2	yes.	16	16384	1-2.5	TBD	350MHz	**TSMC**	**250**	no.	$ 41,500
TARGET3	no.	16	16384	1-2.5	TBD	>= 1GHz	**TSMC**	**250**	no.	$ 41,500
PSEC4	TBD	8?	1K?	TBD	TBD	TBD	**IBM**	**130**	no.	55k?

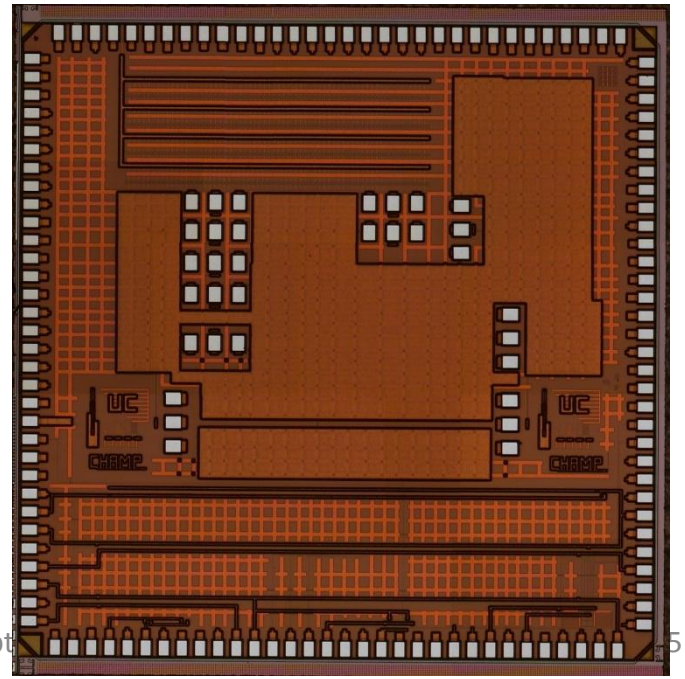
CHAMP

- Chicago-Hawaii ASIC, Multi-Purpose:
  - First experience for Hawaii…
    - …in the IBM 0.13 μm process for all of us.
    - …in ASIC design for a few of us.
    - Hawaii submission was primarily test structures to get a feel for the process, characterize some structures that may be useful on future ASICs.
  - On Chicago side:
    - Primarily independent versions of structures that were similar or identical to PSEC3 for planned characterization & independent debugging.

CHAMP

- Submitted as part of CERN MPW in May 2010.
- First die received from CERN Feb. 14th 2011.
  - ~9 month delay!
  - ~200 die: about same cost as 40 through MOSIS





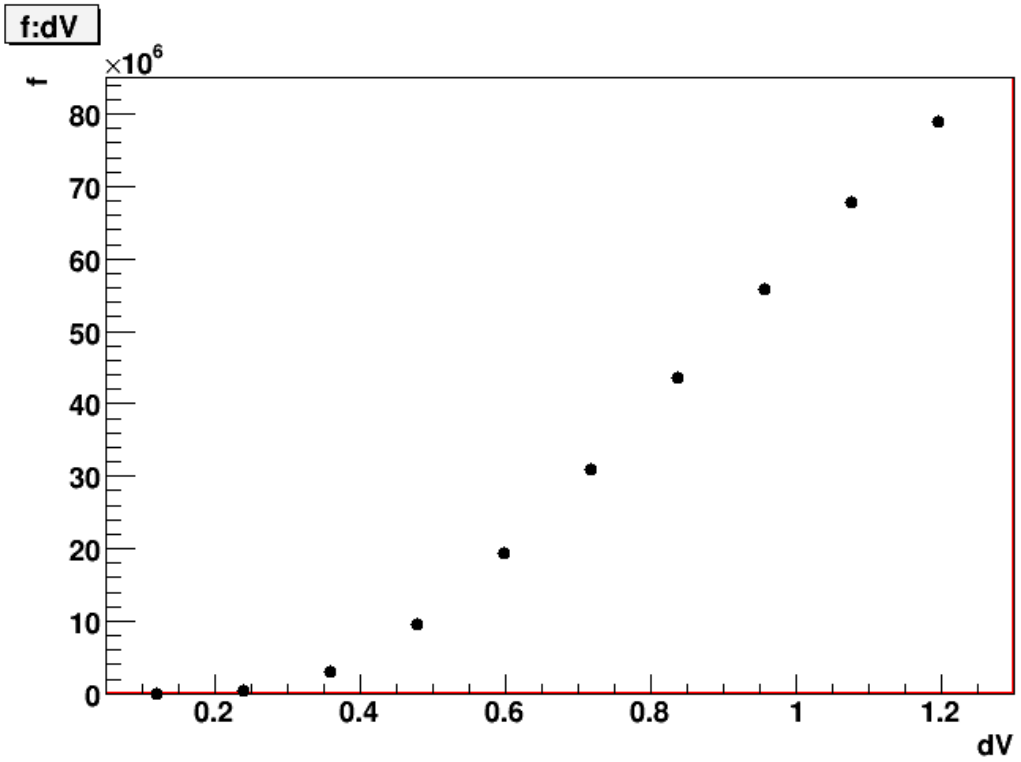
Hawaii Structures on CHAMP

- D flip-flops
- Voltage controlled delay line (VCDL) (x2)
- Voltage controlled ring oscillator (VCRO)
- Digital-to-analog converter (DAC)
- Waveform sampler arrays (WFS) (x4)
- Analog storage cells with built-in comparator
- LVDS receiver
- Charge sensitive amplifier (CSA)

Chicago Structures on CHAMP

- VCDLs w/ delay locked loops (DLLs)
  - "Slow" (18 GHz)
  - "Fast" (25 GHz)
- Independent DLL structure
- VCROs + counters
  - "Slow" (3 GHz)
  - "Fast" (4 GHz)

CHAMP Results (Hawaii) - VCRO



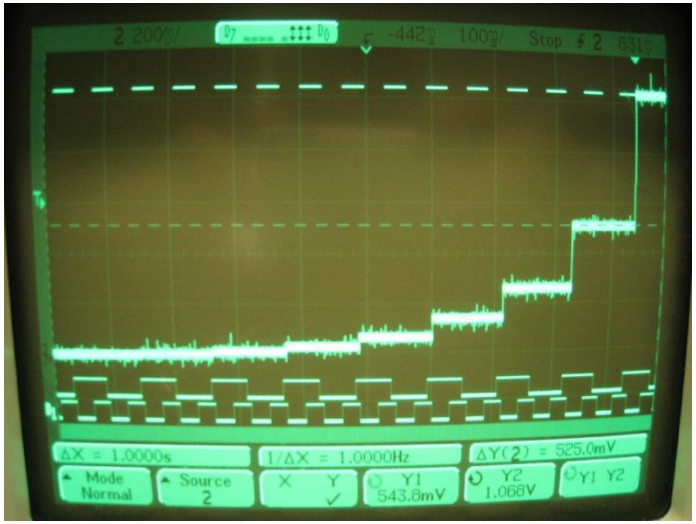
* Parasitic extractions were not working until very recently…

To add/change:
<Plot of VCRO sims w/ and w/o parasitics>

➔ Simulation without parasitics is almost useless for quantitative predicitons…

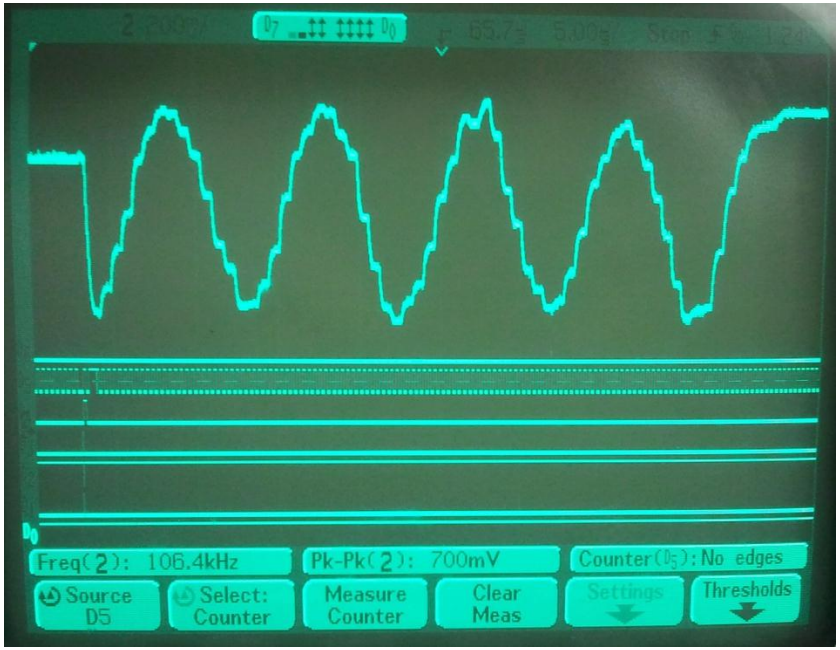
CHAMP Results (Hawaii) - DAC

<Some hopefully better DAC results here…>



CHAMP Results (Hawaii) - WFS

<Some WFS results here…>



CHAMP Results (Chicago)

- <Chicago CHAMP results?>

CHAMP Lessons Learned

- Submission through CERN MPW
  - Potential issues with long delays…
  - …but also may get more chips for same price.
- Hawaii:
  - Experience w/ ASIC design, IBM 0.13 μm.
  - Parasitics are vital! Now working well in Hawaii.
  - Many structures usable for future submissions:
    - DACs (w/ modified control), DFFs, lots of logic
- Chicago:
  - <TBD>

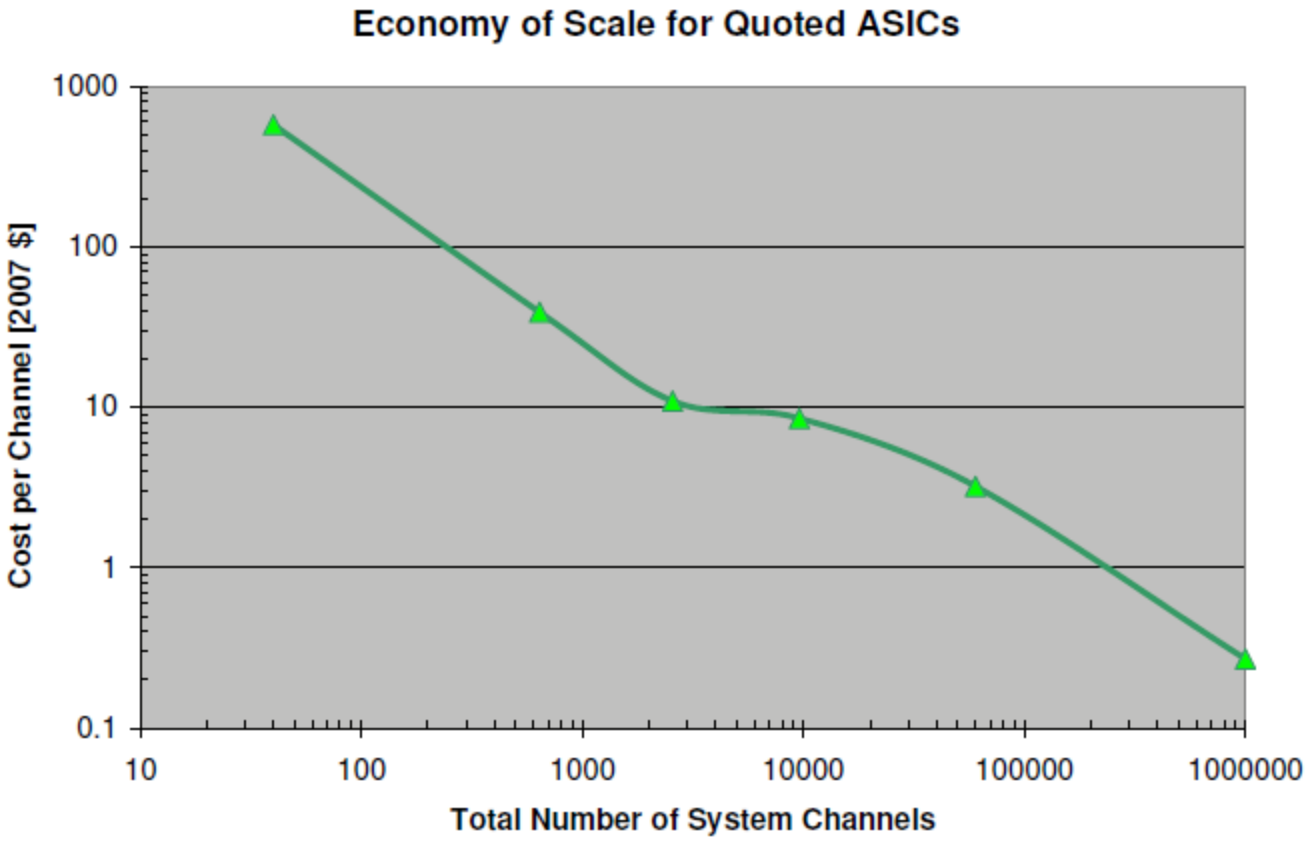
The “AS” in ASIC

- **<Still under construction…>**
- **Different possible ASIC options depending on application…**
- **Discussion/comparison of:**
  - **Sampling rates**
  - **Sampling depth**
  - **ADC linearity**
  - **Estimated costs**

Snapshot of fabricated ASICs (Hawaii)

ASIC	# Ch.	Sampling (GSa/s)	ABW (GHz)	# Samples	# Store cells/chan.	
LAB3	8+1	0.5-3.2	0.8	256+4	same	
BLAB1	1	0.5-6	0.2	64K	same	
BLAB2,3	8	0.5-4	0.3	2*64	32K	2stage x-fer
IRS, IRS2	8	0.5-3.3	1/?	2*64	32K	2stage x-fer
TARGET	16	0.5-2.5	0.2	4K	same	
TARGET2,3	16	0.5-2.0	0.4/1	2*32	16K	2stage x-fer
STURM	8	10-20	~2	4*8	same	
STURM2	8+1	1-200	~3	4*8	same	
LARC	64	0.5-3.5	0.5	1K	same	

All in TSMC 0.25um



<TSMC 0.25um… can we estimate something similar for IBM 0.13 μ m?>