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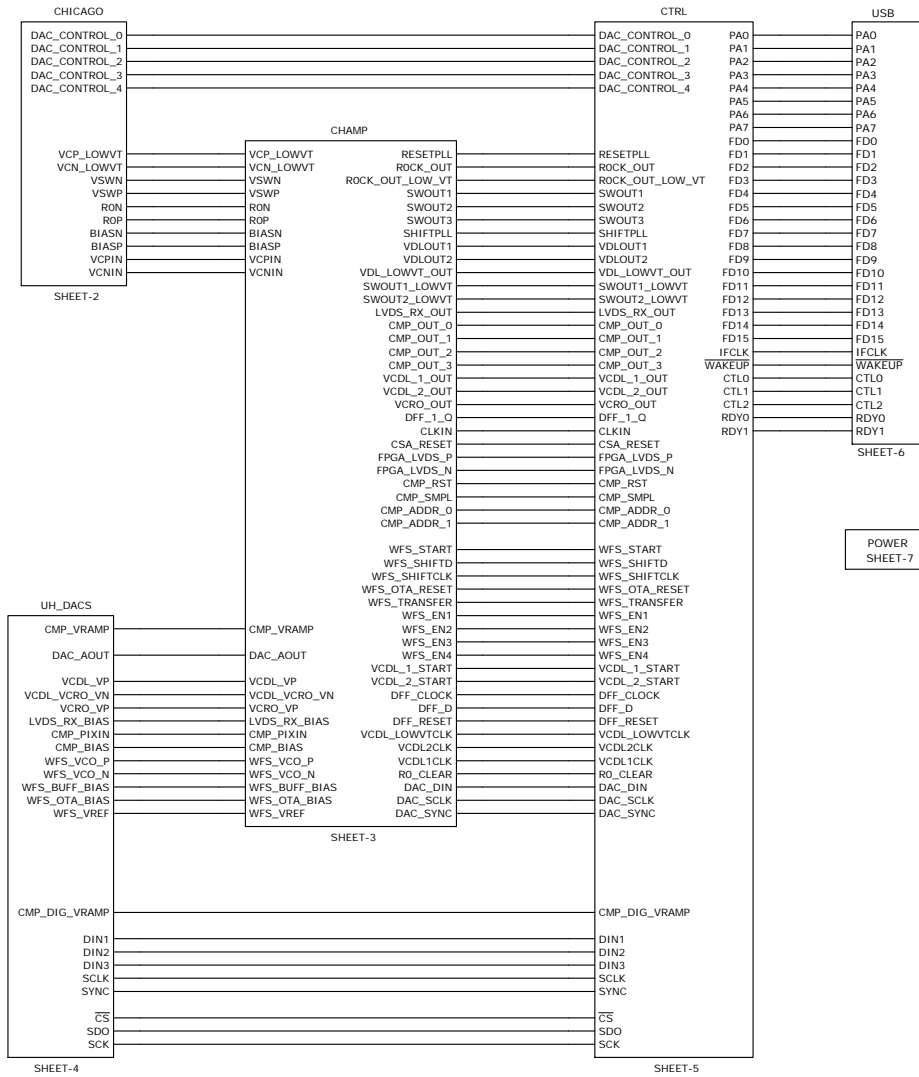
C

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### Layer Stack-up

Top Copper routing  
 Inner Layer 2 plane GND  
 Inner Layer 3 split plane: 1.2V A3.0V D3.3V  
 Inner Layer 4 split plane: A3.3V A1.2V D2.5V  
 Inner Layer 5 split plane: +5V A2.5V D1.2V  
 Bottom Copper routing

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TITLE: CHAMP\_Eval

IDL\_10\_001\_02



Design: GSV

Page Description:  
 TOP Block  
 BS\_LAPPD\_RevA

REV: A

DATED: 10-NOV-2010

[TOP]

SHEET: 1 OF 7

6 5 4 3 2 1

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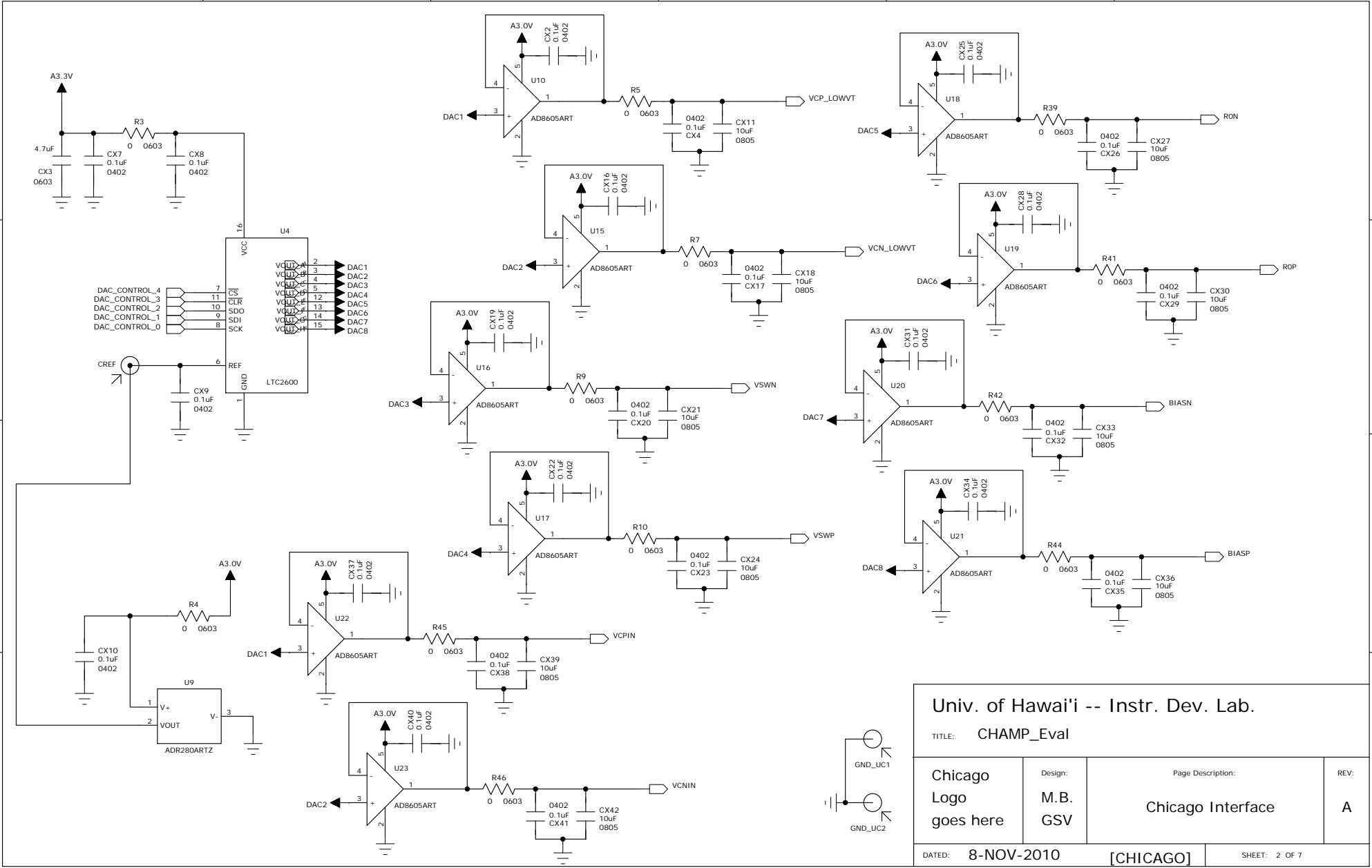
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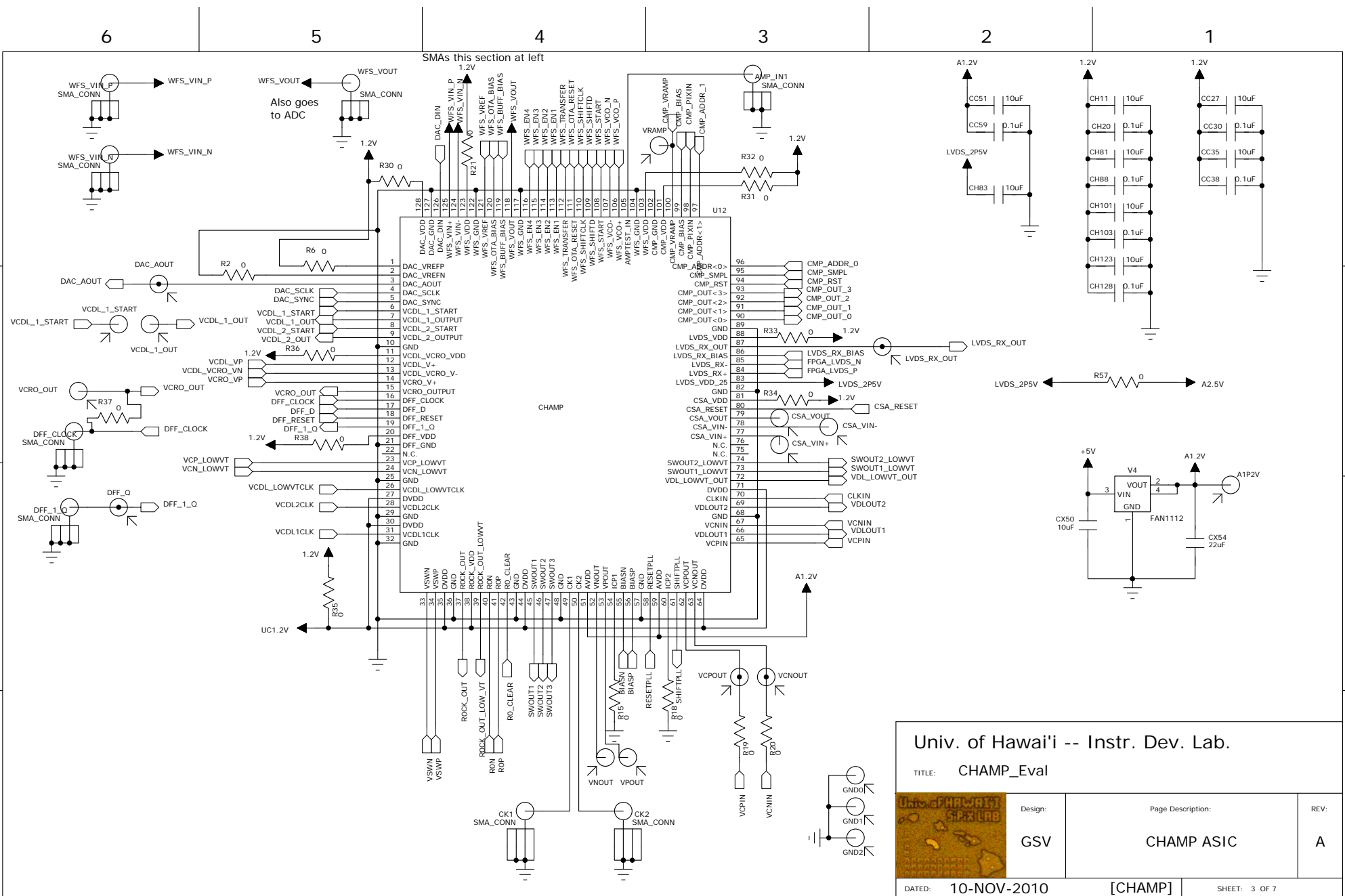
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DATED: 8-NOV-2010		[CHICAGO]	SHEET: 2 OF 7

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TITLE: CHAMP\_Eval

	Design:	Page Description:	REV:
	GSV	CHAMP ASIC	A

DATED: 10-NOV-2010 [CHAMP] SHEET: 3 OF 7

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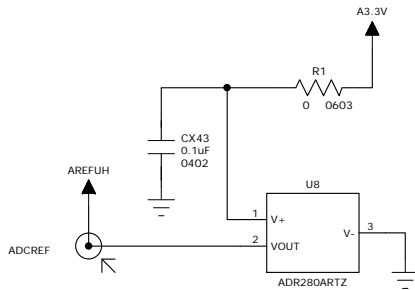
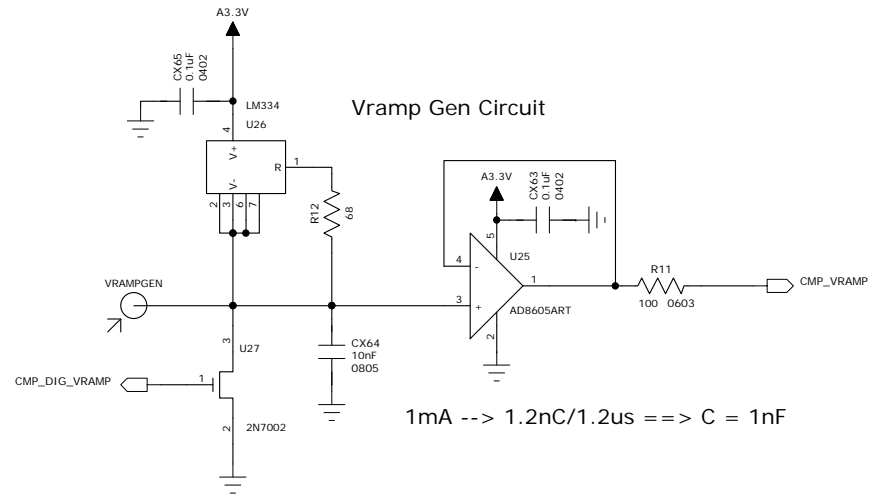
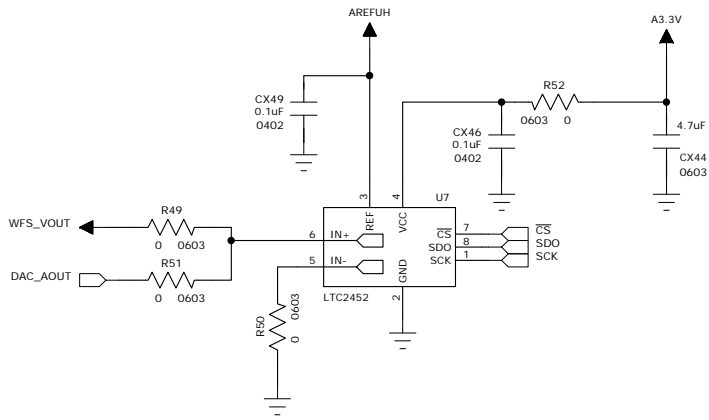
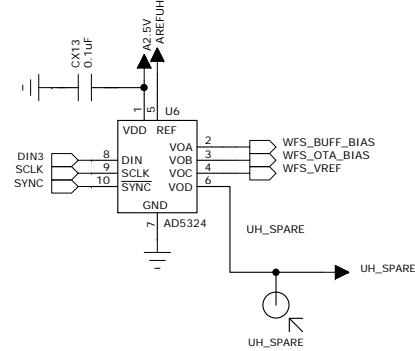
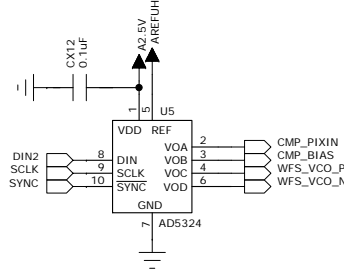
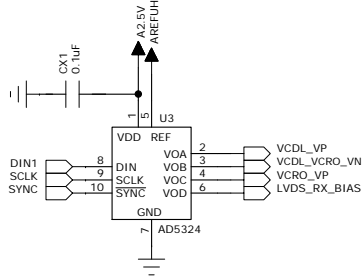
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TITLE: CHAMP\_Eval



Design: GSV

Page Description: CHAMP\_DAC

REV: A

DATED: 9-NOV-2010

[UH\_DACs]

SHEET: 4 OF 7

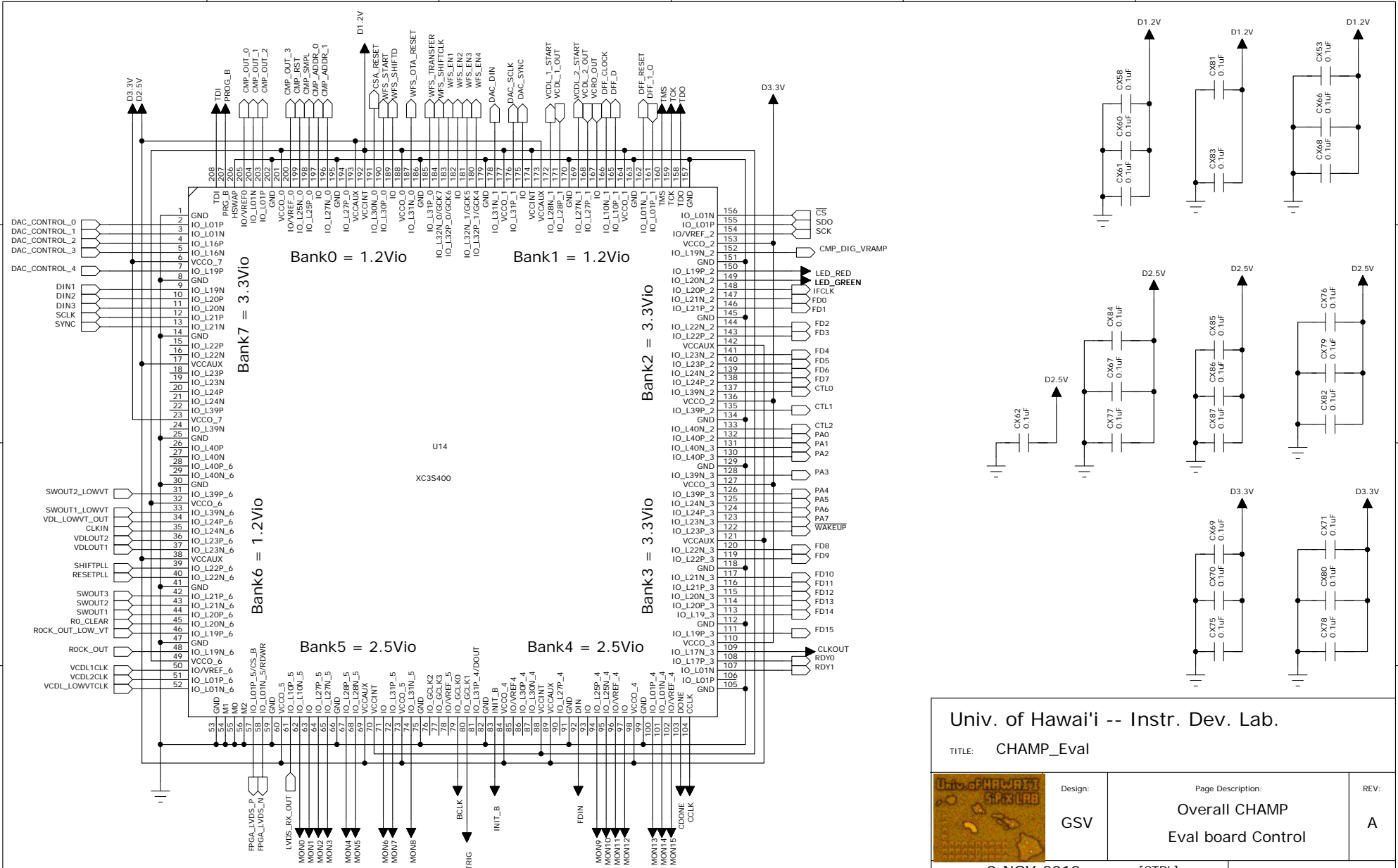
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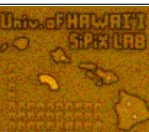
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DATED: 9-NOV-2010		[CTRL]	REV: A
SHEET: 5 OF 7			

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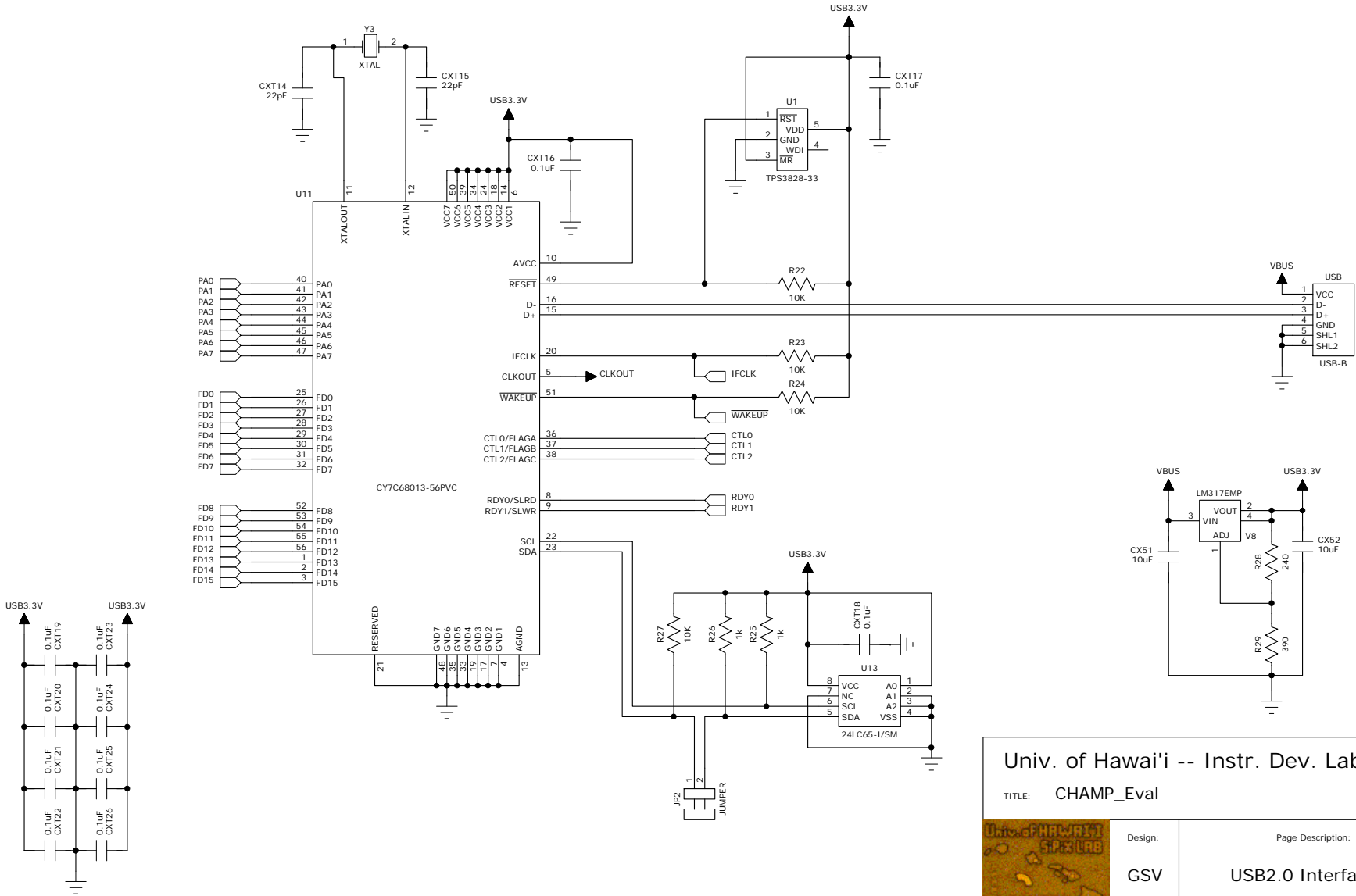
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TITLE: CHAMP\_Eval

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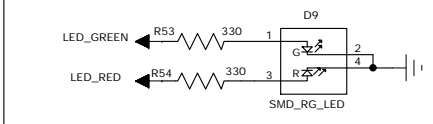
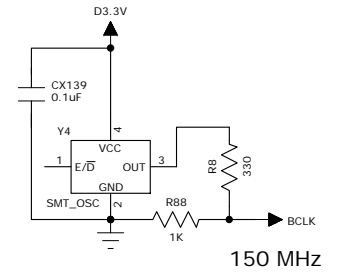
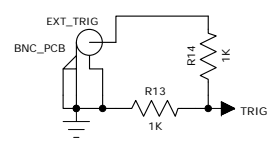
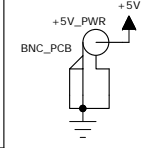
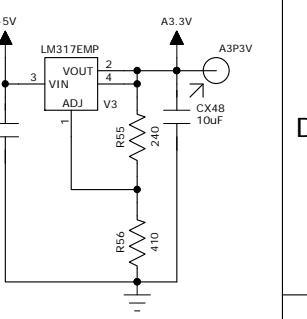
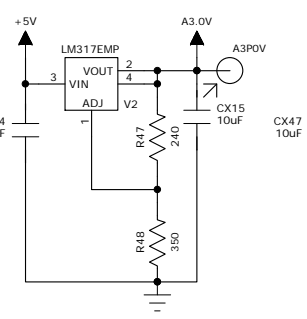
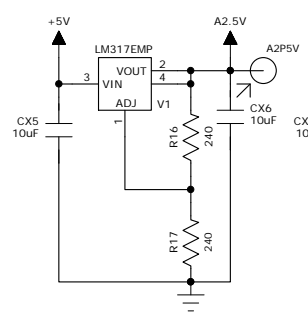
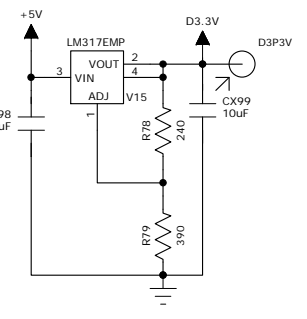
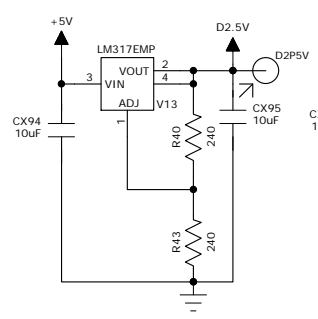
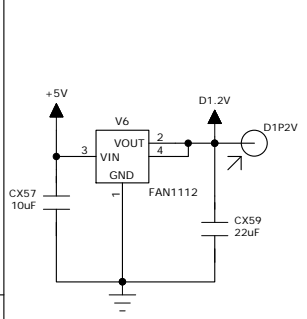
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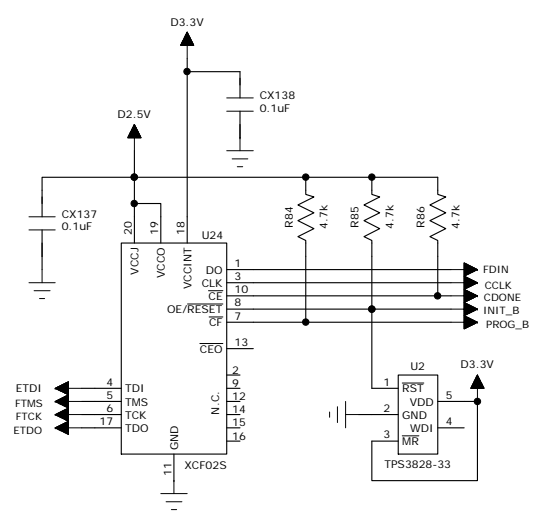
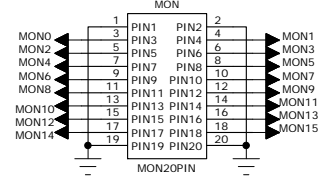
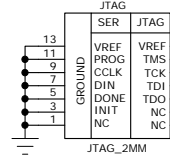
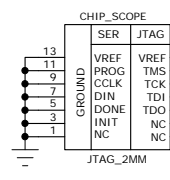
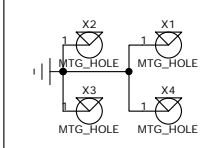
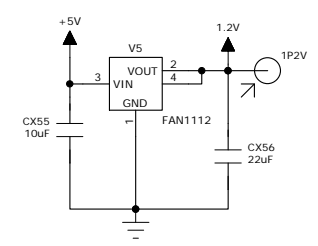
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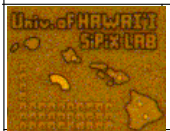


1.2V power for ASIC



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TITLE: CHAMP\_Eval

	Design:	Page Description:	REV:
	GSV	Power Block	A

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