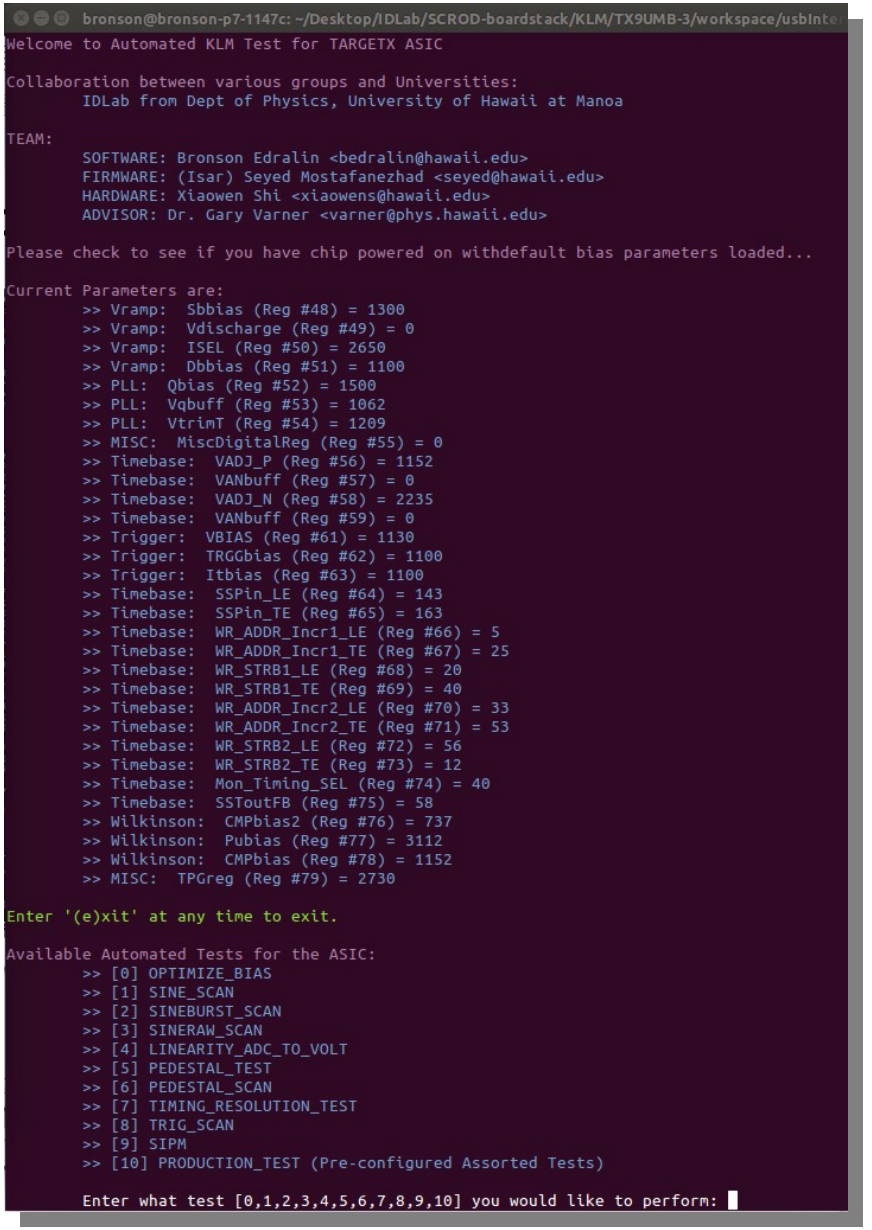
KLM: TARGETX

User-Interface for Testing TARGETX
Testing Overview
Bronson Edralin
04/17/15

TARGETX Test Team

- **TARGETX Waveform Sampling/Digitizing ASIC**
  - Designer
    - Dr. Gary S. Varner
  - Features
    - 1 GSa/s
    - 16 Channels
      - NOTE: 16th Channel used to inject sinusoid for testing.
    - 512 Windows
    - 32 Samples per Window
  - Used for?
    - KLM Sector of the Belle II Detector system in Japan
- **TARGETX Test Team at University of Hawaii**
  - Software
    - Bronson Edralin
  - Firmware
    - Dr. Seyed “Isar” Mostafanezhad
  - Hardware
    - Xiaowen Shi
  - Advisor
    - Dr. Gary S. Varner
  - Special Thanks to...
    - Peter Orel, Lauri “Vihtori” Virta

User Interface for Testing TARGETX



Default Registers: BiasRev #1.1

Signal	Register #	Default Value (old)	Run values	Default Value (new)
SSTIN_N				
VADJ_P	56	1152		
VADJ_N	58	2235		
ISEL	50	2650		
Vdischarge	49	0		
WL_CLK_p			63.7 MHz	
CMPbias2	76	737		
Pubias	77	3112		
Qbias	52	1500		
VANbuff	57	0		
Vqbuff	53	1062		
SSToutFB	75	58		
VtrimT	54	1209		
CMPbias	78	1152		

Signal	Register #	Default Value (old)	Run values	Default Value (new)
Mon_Timing_SEL	74	40		
WR_ADDR_Incr1 LE	66	13		
WR_ADDR_Incr1 TE	67	33		
WR_STRB1 LE	68	20		
WR_STRB1 TE	69	40		
WR_ADDR_Incr2 LE	70	33		
WR_ADDR_Incr2 TE	71	53		
WR_STRB2 LE	72	56		
WR_STRB2 TE	73	12		
VBIAS	61	1130		

Projected Implementations to Automate Certain Tests

√ **OPTIMIZE_BIAS**
- Using Infinite Sinusoid
- Be able to choose what bias register value to change
- Stitch all windows and plot all waveforms onto one graph
- Fit to Expected Sinusoid and plot it per waveform
- Plot Residuals
- Use Avg Chi-Squared Test to Quantify Best Fit (Multiple events increase accuracy)
- Plot Chi-Squared Test Scores vs Bias Register Value

√ **SINE_SCAN**
- Same as above but doesn't prompt to optimize biases.
- Asks how many graphs do you want.

√ **SINEBURST_SCAN**
- Using Burst Sinusoid
- Be able to set parameter of the Delay and Cycles of the Sinusoidal Burst Pulse
  - Ex. Delay = 1us:1us:4us
  - Ex. Cycles = 3
- Scan all 512 windows and plot onto one graph
- Make individual plots for every series of 4 windows

• **LINEARITY_TEST**
- Control Digital DC Power Supply Remotely
- Be able to set parameter for input dc voltage
  - Ex. Input = 0mV:1mV:300mV
- Plot results to show dynamic range
- Regression Analysis to fit a line/curve of best fit to results to extract transfer function so we can convert ADC Count to Voltage

√ **PEDESTAL_TEST**
- Total of 16,384 analog storage cells
- Keep input function generator OFF
- Perform Histogram on select cells for 5,000 Events
- Histogram will tell us 2 things:
  - Mean = Should be centered around zero if Pedestals were generated from firmware and subtracted properly
  - Std Deviation = if reasonable or defective storage cell

√ **TIMING_RESOLUTION_TEST**
- Find Zero Crossings at Rising Edges to calculate Period
- Plot Histogram of Period
- Spatial dependence on starting position time was observed so timing correction was made which displayed even better timing resolution

• **TRIG_SCAN**
- Heatmap of trigger frequency for different thresholds by using a set High Voltage DAC value with a High Voltage Reference between 69V & 75V
- HV_DAC = 10, 100; Threshold=3400:1:3700
- Isar (UH) sorting out details in firmware

• **SIPM**
- Plot temperature and currents

• **FINALLY**: Results must be properly logged in a Database or external hard drive. This means data must be organized well in a csv file initially with the proper headers. Folders must be in an appropriate hierarchical order

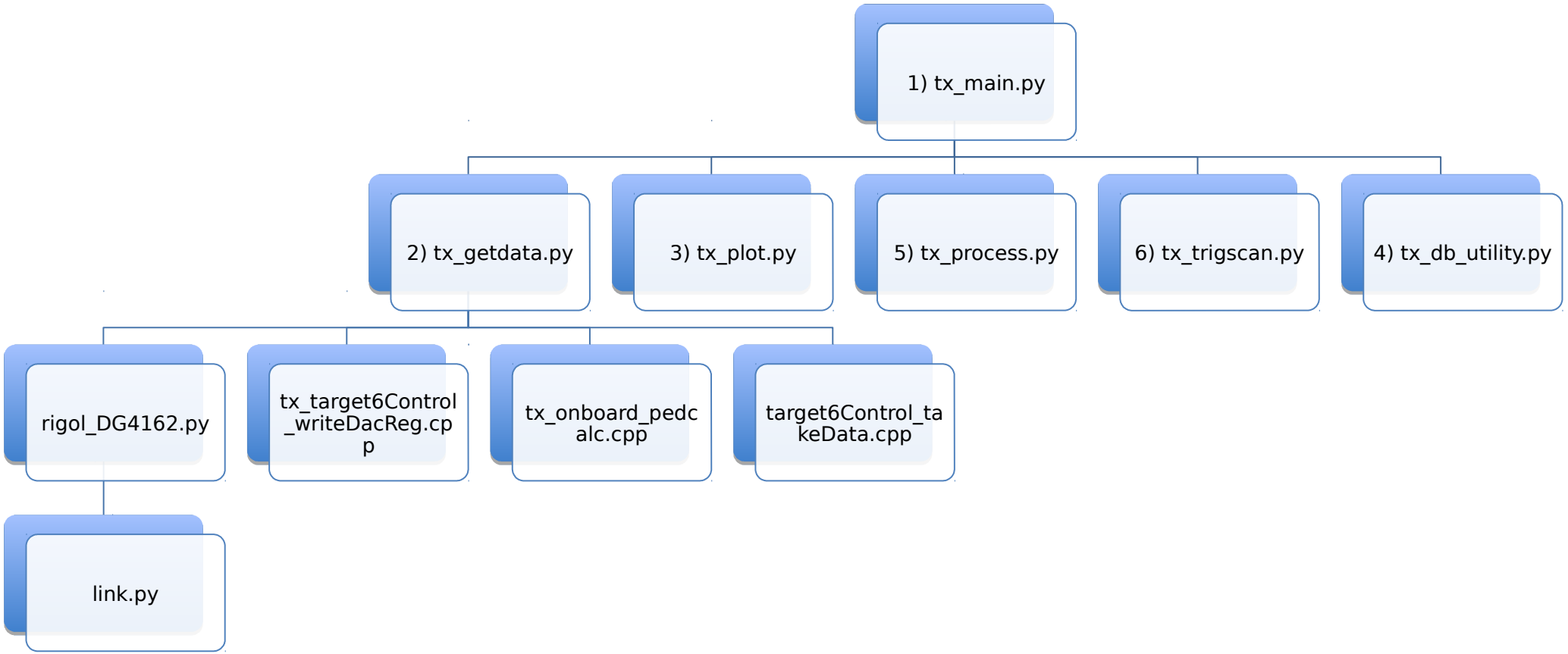
NOTE: Green means implemented, Red means not implemented yet, Yellow means in development

Estimation of Time to Complete each Test

- **OPTIMIZE_BIAS**
  - Randomly pick 4 Windows (200 Events, 100 Bias Sweep)
    - **3 Hours, 40 Minutes**
  - Randomly pick 4 Windows (1 Event, 4000 Bias Sweep)
    - **8 Hours, 45 Minutes**
  - Generates 1 plot with all windows stitched together
  - Generates 2*1 plot (dot or line) per bias value change for each set of 4 Windows (2*128 plots minimum for all 512 Windows)
    - Scales Sinusoid Amplitude to 1 and fits it to Expected Sinusoid with unity amplitude
    - Generates chi-squared test score for each fit and add to csv file
    - Generate 1 plot for chi-squared test score vs bias value
    - Generates total residual plot and errorbar of residuals for each fit.
  - Generates 1 connected scatter plot per 4 windows stitched
- **SINE_SCAN**
  - Windows 0 – 512 (1 Event)
    - ~~16 Minutes~~... Now 11 Minutes 36 Seconds
  - Same as OPTIMIZE_BIAS just no bias changed
- **SINEBURST_SCAN**
  - Windows 0 – 512 (1 Event)
    - ~~16 Minutes~~... Now 11 Minutes 36 Seconds
  - Generates 1 plot with all windows stitched together
  - Generates 1 plot for each set of 4 Windows (128 plots minimum for all 512 Windows)
    - Does not do fit
- **LINEARITY_ADC_TO_VOLT**
  - To Be Determined
- **PEDESTAL_TEST**
  - Randomly pick 4 Windows (5000 Events)
    - **50 Minutes**
  - Generates 2*128 histograms of ADC Count for analog storage cells
    - 128 histograms including Outliers
    - 128 histograms filtering Outliers
  - Generates 2*1 errorbars for analog storage cells in mean and std
    - 1 errorbar including Outliers
    - 1 errorbar filtering Outliers
  - Generates 1 plot for percentage of outliers across 128 analog storage cells
- **TIMING_RESOLUTION_TEST**
  - Randomly pick 4 Windows (5000 Events)
    - **50 Minutes**
  - Randomly pick 4 Windows (100000 Events)
    - **16 Hours 52 Minutes**
- **TRIG_SCAN (for RHIC Board)**
  - HV_DAC = 10, 100; Threshold=3400:1:3700
    - **6 Hours, 23 Minutes, 48 Seconds**
- **PRODUCTION_TEST**
  - Decide on what tests to actually perform
  - With future changes to be made to new motherboard, we will be able to perform a test sweep across all 10 TARGETX ASICs in one go.

NOTE: Red means not implemented yet

Layout of Scripts Written [1/2]



Layout of Scripts Written [2/2]

1. **main.py**
    1. User Interface that help ensure right inputs
2. **tx_getdata.py**
    1. Write new bias register values
    2. Turn function generator on/off remotely in between pedestal generation
        1. Leave output off if 'PEDESTAL_TEST'
    3. Collect data
    4. Parse data
    5. Save data
3. **tx_plot.py**
    1. Plot all waveforms on one graph
    2. Histograms, plots for numerous tests
4. **tx_db_utility.py**
    1. Upload test data to PostgreSQL database
5. **tx_process.py**
    1. SINEBURST_SCAN
        1. Plot Sinusoids in Appropriate Windows
    2. PEDESTAL_TEST
        1. Plot Histogram per Analog Storage Cell
        2. Extract Mean, std. Save in csv file
5. **tx_process.py (continued)**
    3. OPTIMIZE_BIAS or SINE_SCAN
        1. Fit observed sinusoid with expected sinusoid
            1. Scale amplitudes to unity
            2. Synchronization w/ Matched Filter
        2. Plot fitted sinusoids on multiple plots
        3. Chi-Squared Test (Goodness of Fit) quantize results saving scores on csv
            1. Plot results from chi-squared test
    4. LINEARITY_ADC_TO_VOLT
        1. Determine Amplitude of Sinusoid
        2. Plot Amplitude: Voltage vs ADC Count
        3. Extract ADC to Voltage Transfer Function
    5. TIMING_RESOLUTION_TEST
        1. Find zero crossings to determine Period
        2. Plot histogram of Period
6. **tx_trigscan.py**
    1. TRIG_SCAN
        1. Plot heatmap of trigger count for different thresholds per HV_DAC value
7. **tx_production.py or tx_production_parallel.py**
    1. PRODUCTION_TEST
        1. Choose ASIC #0-9
        2. Bunch of Pre-Configured Tests

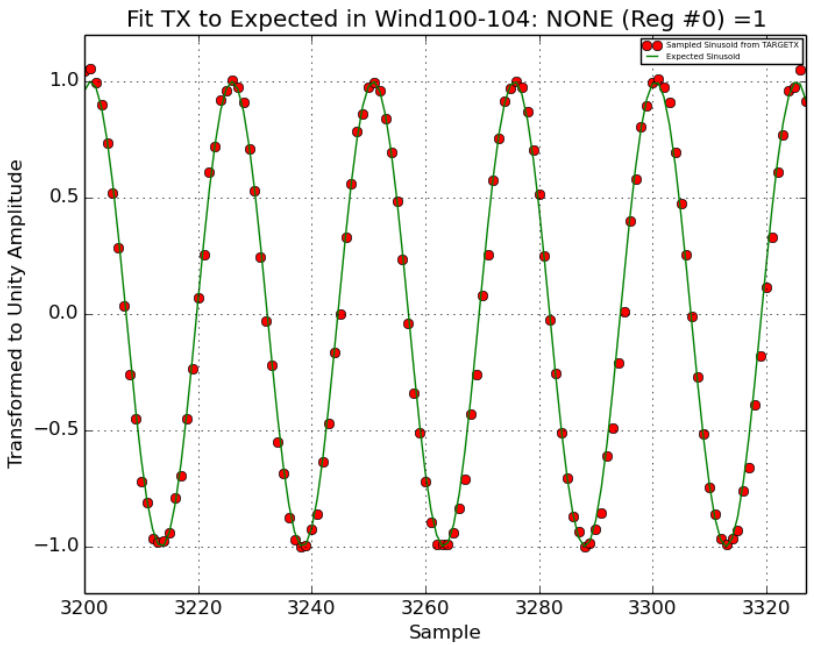
NOTE: Red means not implemented yet, Yellow means in development

How Pedestals are done?

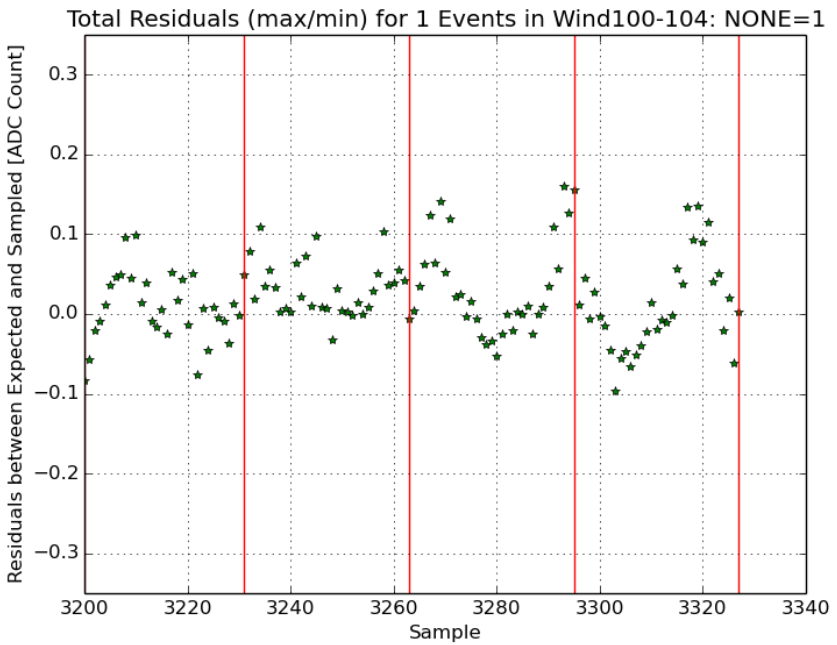
- AC Coupled Input
  - Steps
    - Change Bias Register Value
    - Turn OFF Func Gen
    - Generate Pedestals
    - Turn ON Func Gen
    - Get Data
- DC Coupled Input
  - Steps
    - Change Bias Register Value
    - Turn ON Func Gen
      - Change Amplitude to 1mVPP (smallest)
    - Generate Pedestals
    - Turn ON Func Gen
      - Change Amplitude back to Default Amplitude
    - Get Data

OPTIMIZE_BIAS & SINE_SCAN

Fit Sampled Waveform to Expected Sinusoid by using Matched Filter for Synchronization



Residuals by subtracting sampled by expected value from same data plotted on left

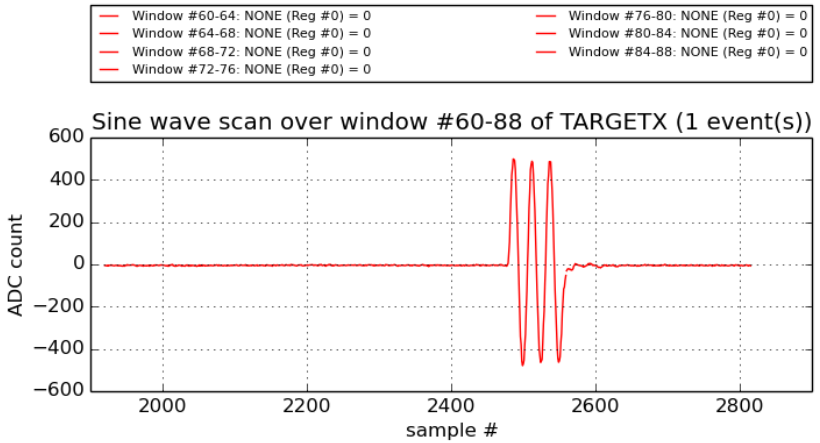


NOTE: Chi-Squared Results used to quantify results and choose optimum bias register value

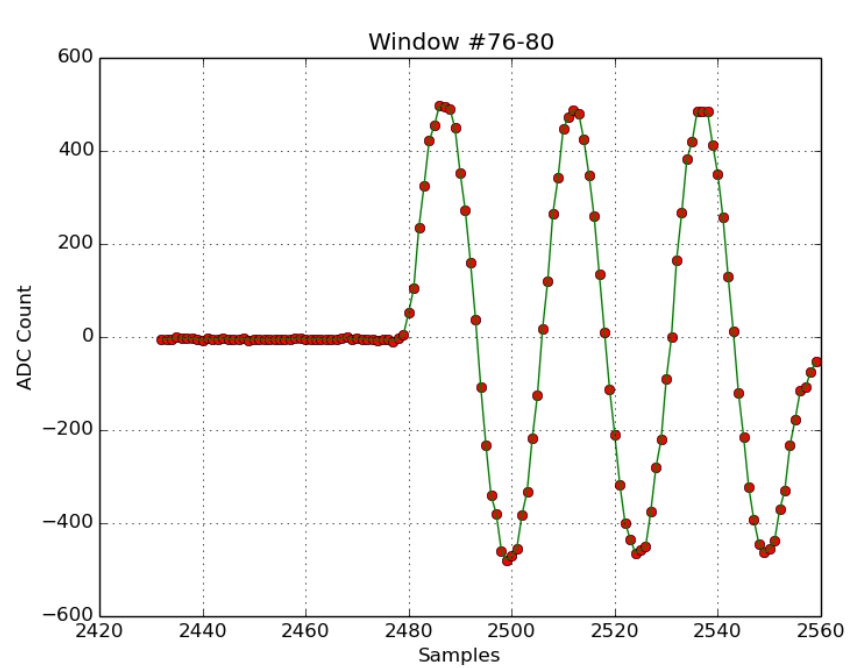
**** More plots can be seen by performing test ****

SINEBURST_SCAN

Ability to scan all 512 windows and plot them



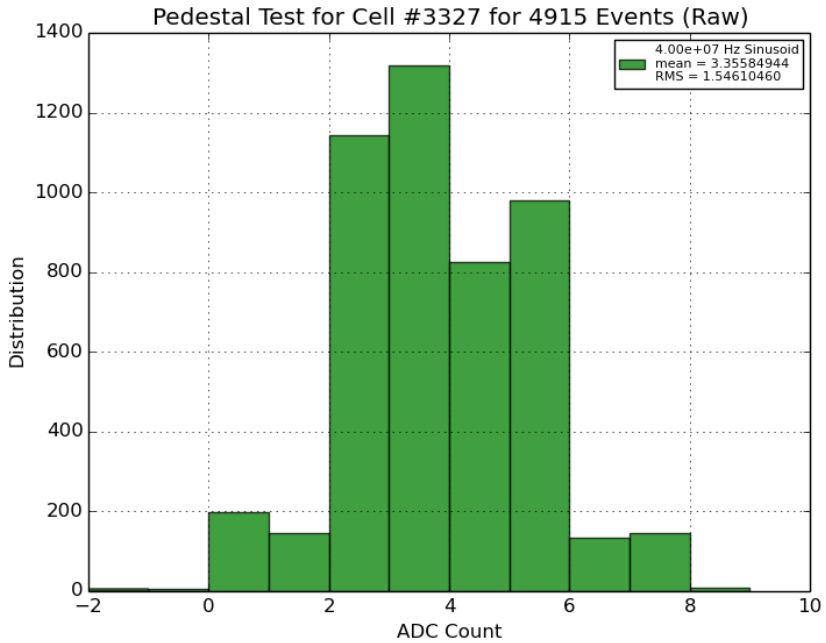
A typical waveform readout is made of 4 windows



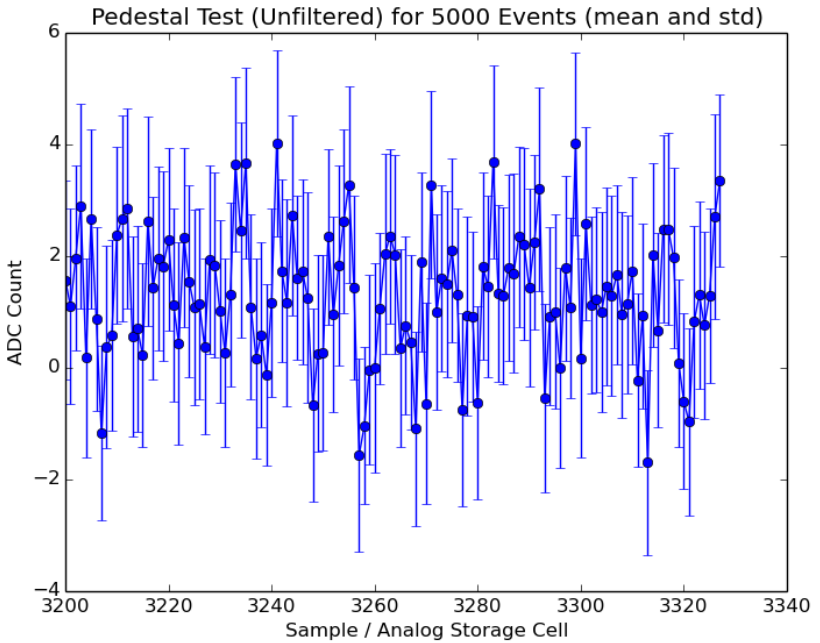
**** More plots can be seen by performing test ****

PEDESTAL_TEST

Histogram of one cell



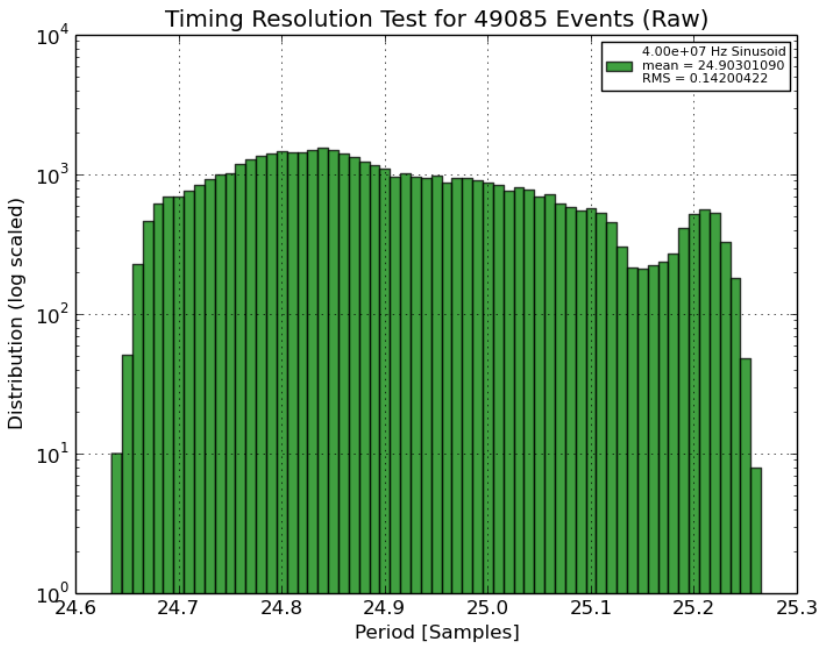
Errorbar plot of mean and std per cell (128 cells)



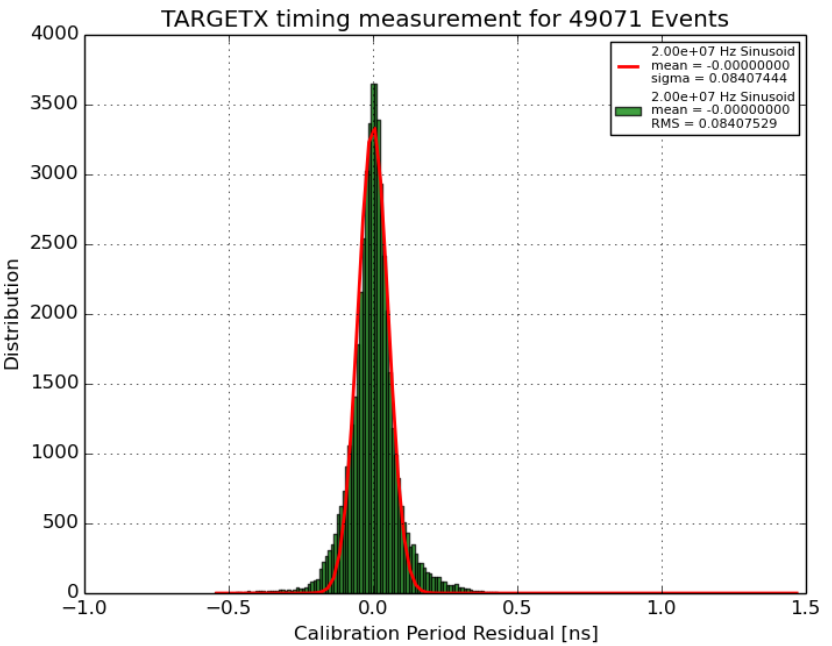
**** More plots can be seen by performing test ****

TIMING_RESOLUTION_TEST

*You can estimate the TARGETX sampling rate by multiplying the mean by the known frequency of the input signal (20MHz*49.94272829 = **0.998855 GSa/s**)*



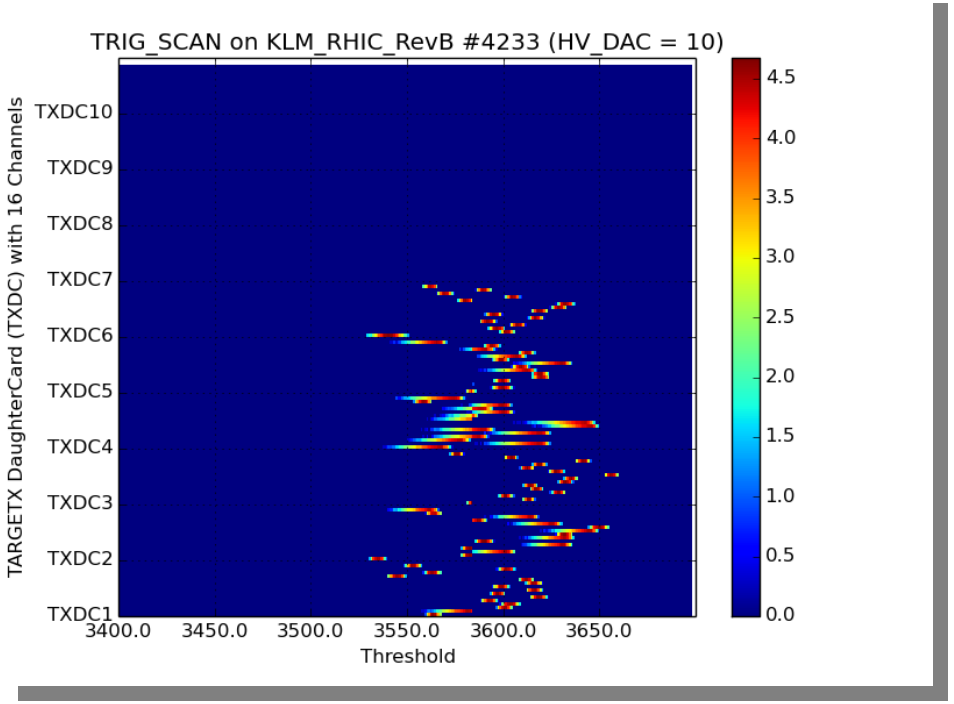
*Spatial Dependence was shown on the starting position time. After correcting for this, the histogram below as obtained which displayed that we were getting **84 ps time resolution**.*

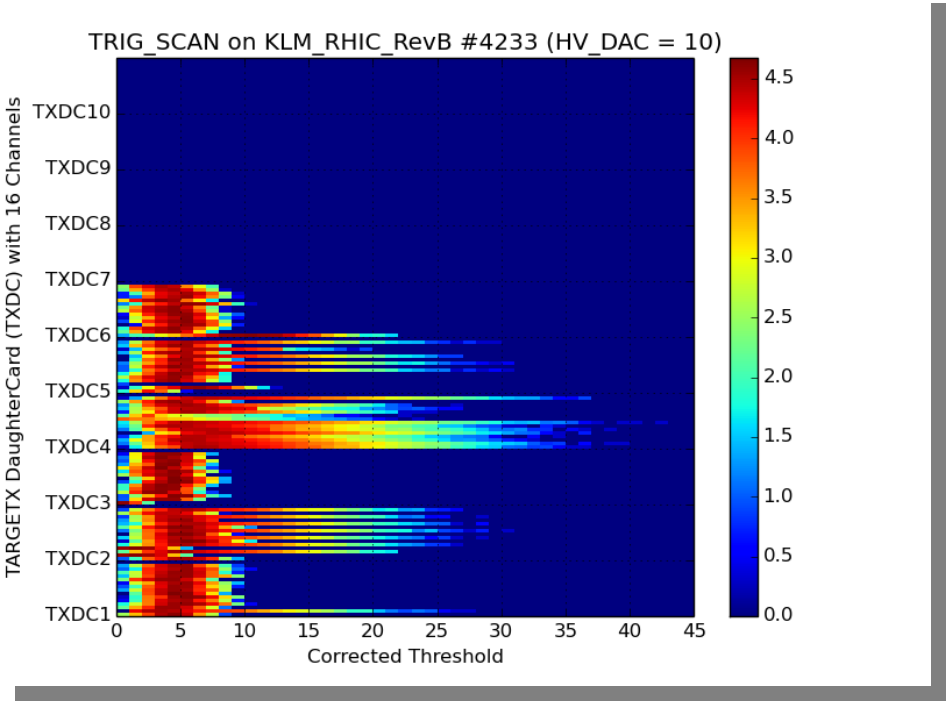


**** More plots can be seen by performing test ****

TRIG_SCAN

TXDC1-6 connected on MotherBoard,
but only TXDC1, TXDC2, TXDC4, TXDC5 & TXDC6 cables connected to RHIC Board





NOTE: This particular test is still in development stage where Isar (UH) is working out details in Firmware.

**** More plots can be seen by performing test ****

PRODUCTION_TEST

List of tasks for production:

- **OPTIMIZE_BIAS**
  - Randomly choose 4 Windows for readout
  - 5 Events
  - Choose all 10 ASICs (ASICno 0-9 or TXDC1-10) on MotherBoard
  - 10 Bias Register Value sweep (around 58) on SSTOUTFB (Reg #75)
  - *Optimize the most sensitive Timebase Bias Register*
- **SINE_SCAN**
  - Choose all 512 Windows for readout
  - 5 Events
  - Choose all 10 ASICs (ASICno 0-9 or TXDC1-10) on MotherBoard
  - *Verify a clean visual of a sinusoid*
- **PEDESTAL_TEST**
  - Randomly choose 4 Windows for readout
  - 5000 Events
  - Choose all 10 ASICs (ASICno 0-9 or TXDC1-10) on MotherBoard
  - *Look for outliers*
- **TRIG_SCAN**
  - HV_DAC = 10, 100
  - Threshold = 3400:1:3700
  - *Verify hardware trigger*
- **SIPM**
  - Read out currents and temperature
  - *Verify health of board*

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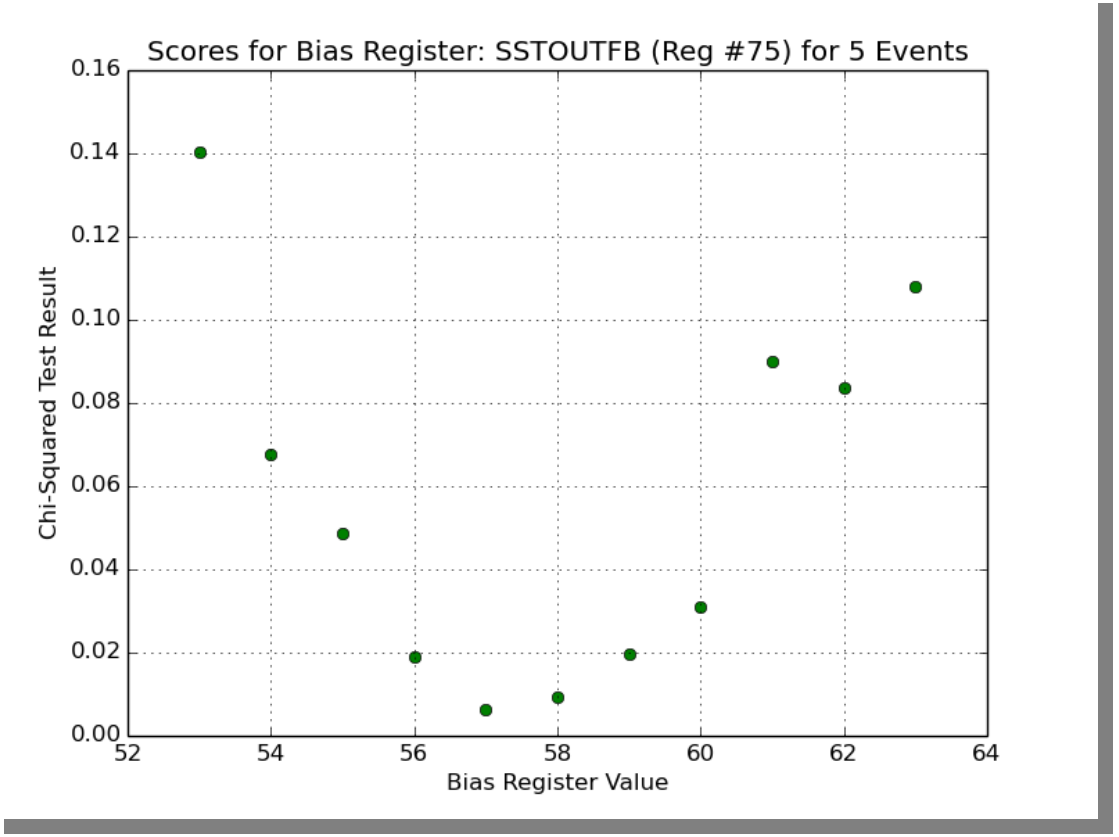
PRODUCTION TEST:
1) OPTIMIZE_BIAS [1/4]

"Fitting and Chi-Squared Test Algorithm" *to choose optimum bias register value*

1. Control a function generator to inject a 40MHz Sinusoid with 900mVPP Amplitude
2. Readout and construct waveform "X"
3. Scale amplitude of waveform "X" to unity amplitude
4. Construct an expected sinusoid "E" by sampling (at 0.997530400 GSa/s which was found by the TIMING_RESOLUTION_TEST) a 40MHz Sinusoid with unity amplitude
5. Use matched filter to achieve synchronization for fitting with waveforms "X" and "E"
6. Plot synchronized waveforms "X" and "E" onto same plot and call it Fitting#
7. Plot residuals for "X" and "E"
8. Calculate Chi-Squared Result of "X" and "E" and log these raw values
9. Use average of the raw values of the Chi-Squared Results for waveforms with multiple events to determine optimum bias register value

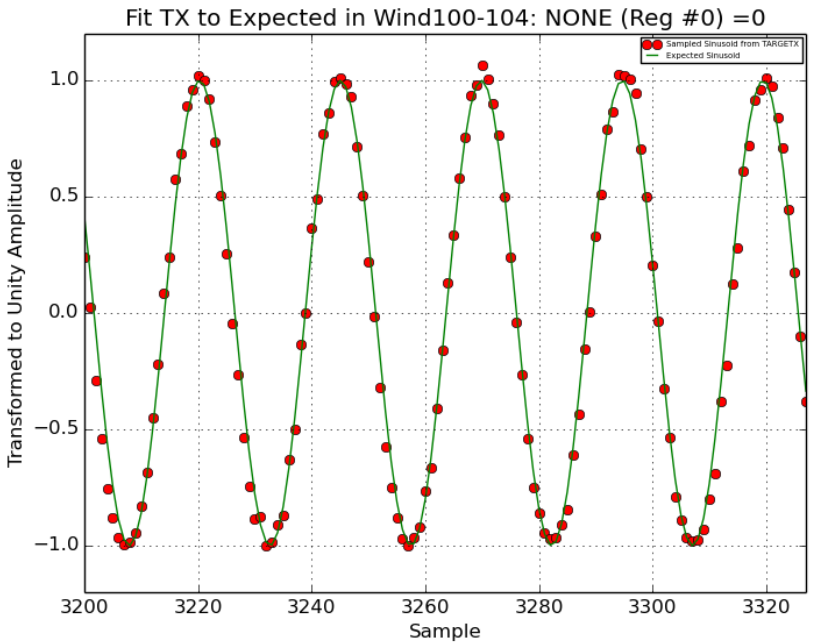
PRODUCTION TEST:
1) OPTIMIZE_BIAS [2/4]

Optimum SSToutFB Value Chosen

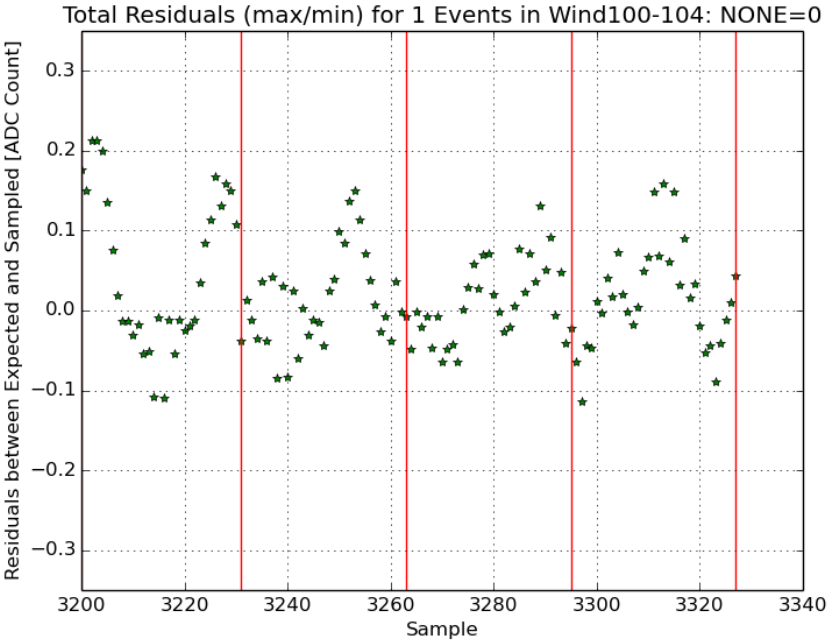


PRODUCTION TEST:
1) OPTIMIZE_BIAS [3/4]

TARGETX Sampling Speed and/or Frequency of Function Generator Changes

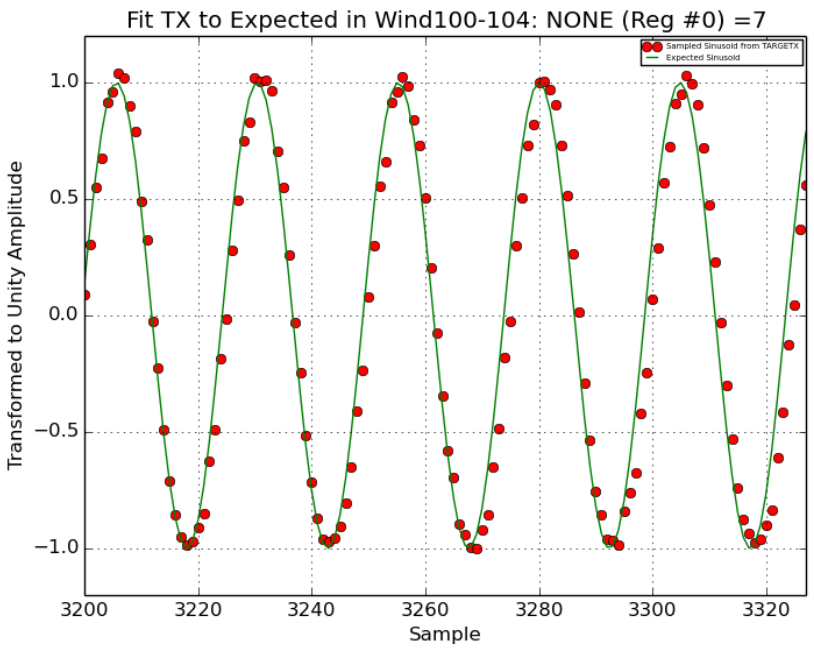


The variance of the sampling speed and/or frequency of the input waveform will affect the fitting which can be seem from looking at the residuals (see next slide)

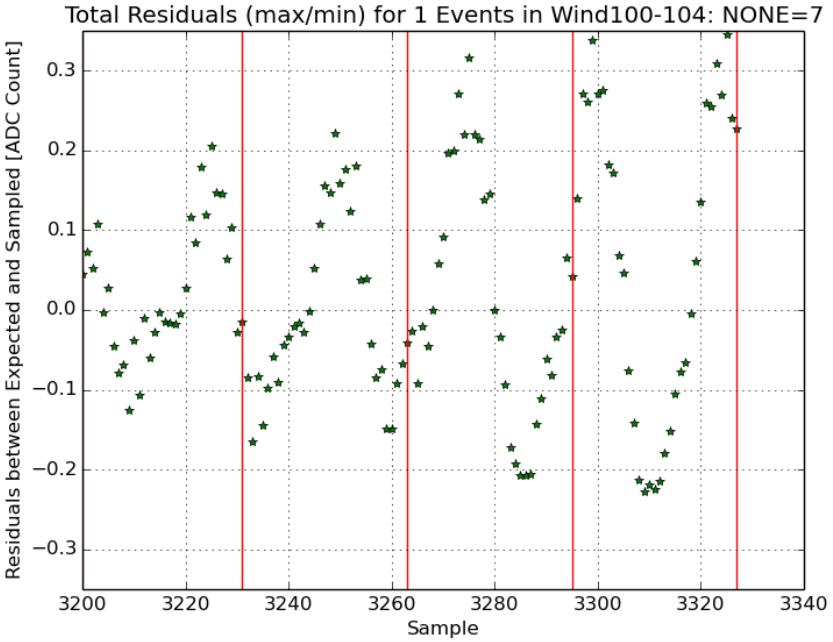


PRODUCTION TEST:
1) OPTIMIZE_BIAS [4/4]

TARGETX Sampling Speed and/or Frequency of Function Generator Changes

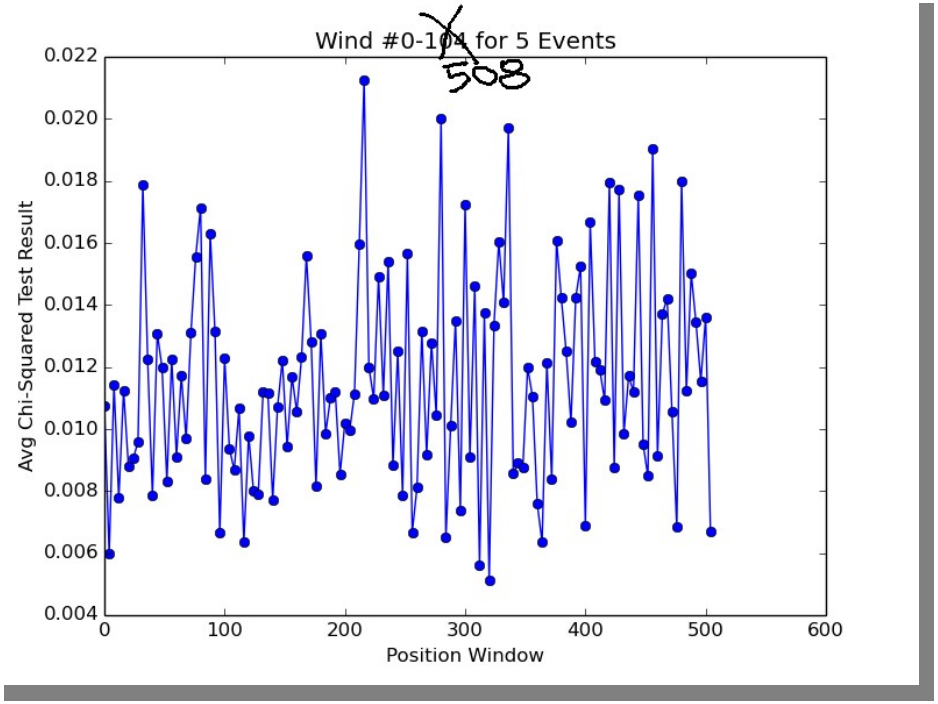


The variance of the sampling speed and/or frequency of the input waveform will affect the fitting which can be seem from looking at the residuals

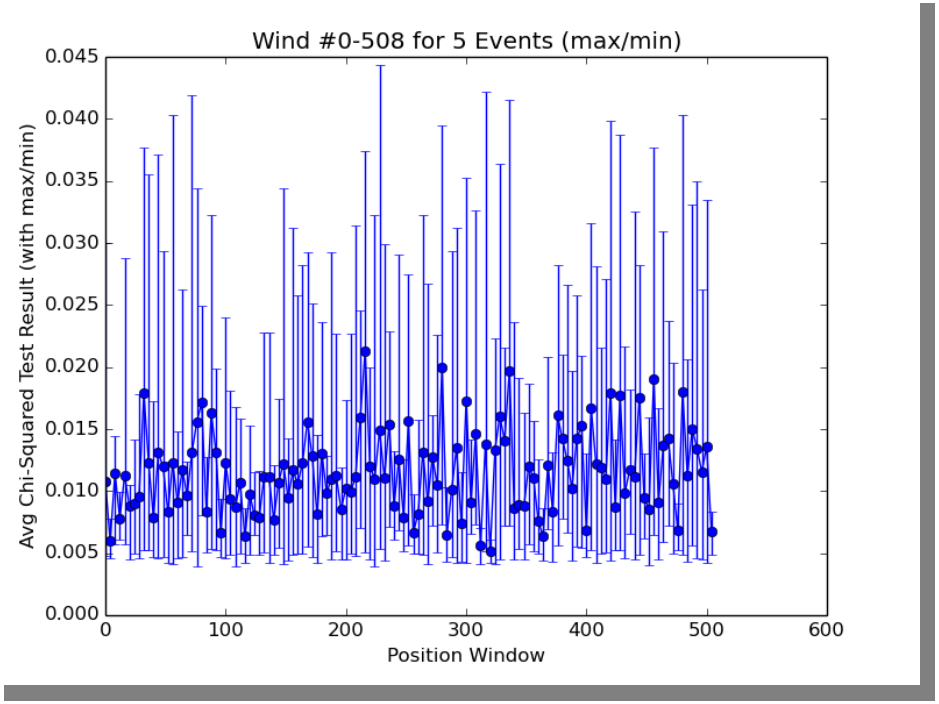


PRODUCTION TEST:
2) SINE_SCAN [1/2]

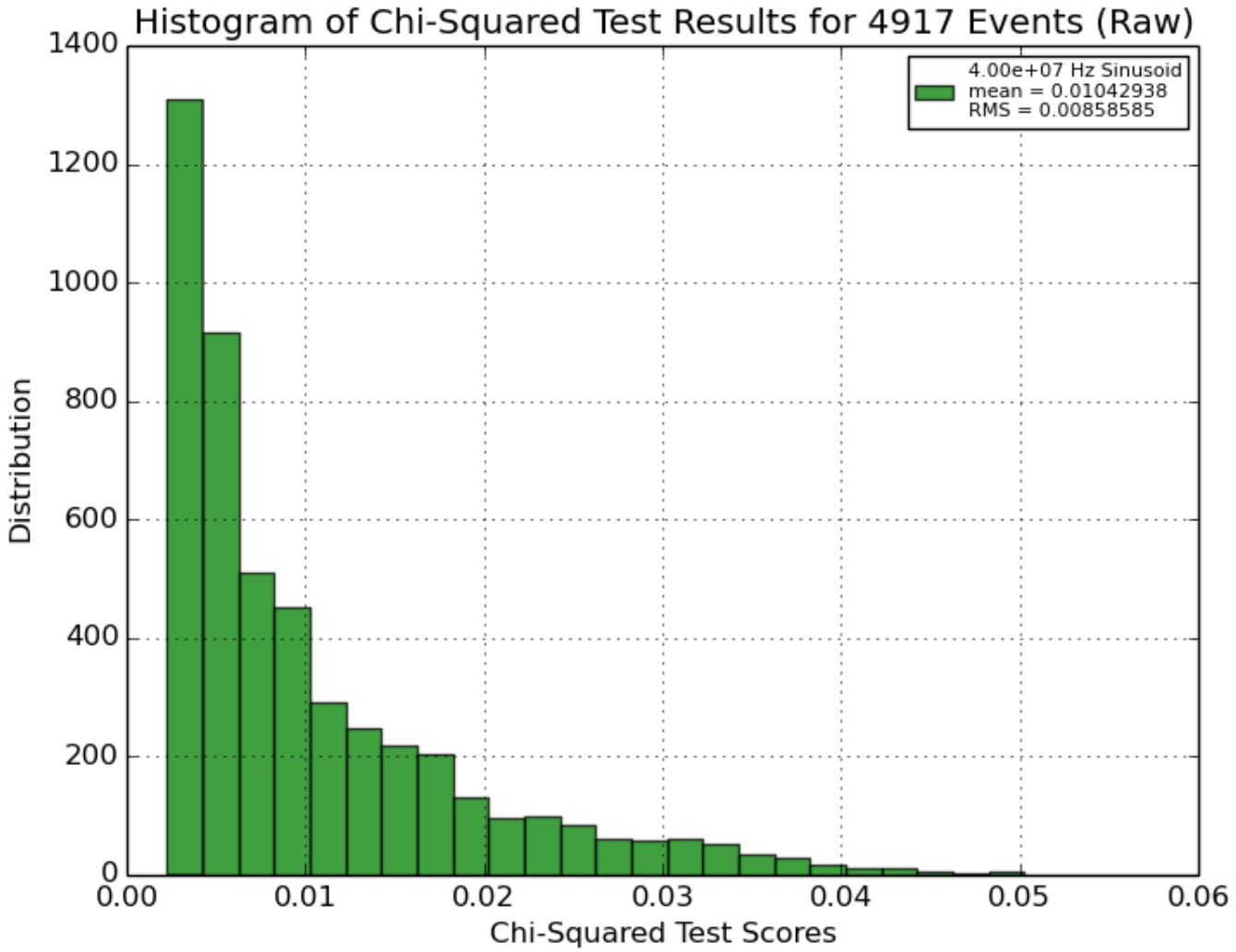
Avg Chi-Squared Scores Across all Windows



Avg Chi-Squared Scores (with errorbars) Across all Windows

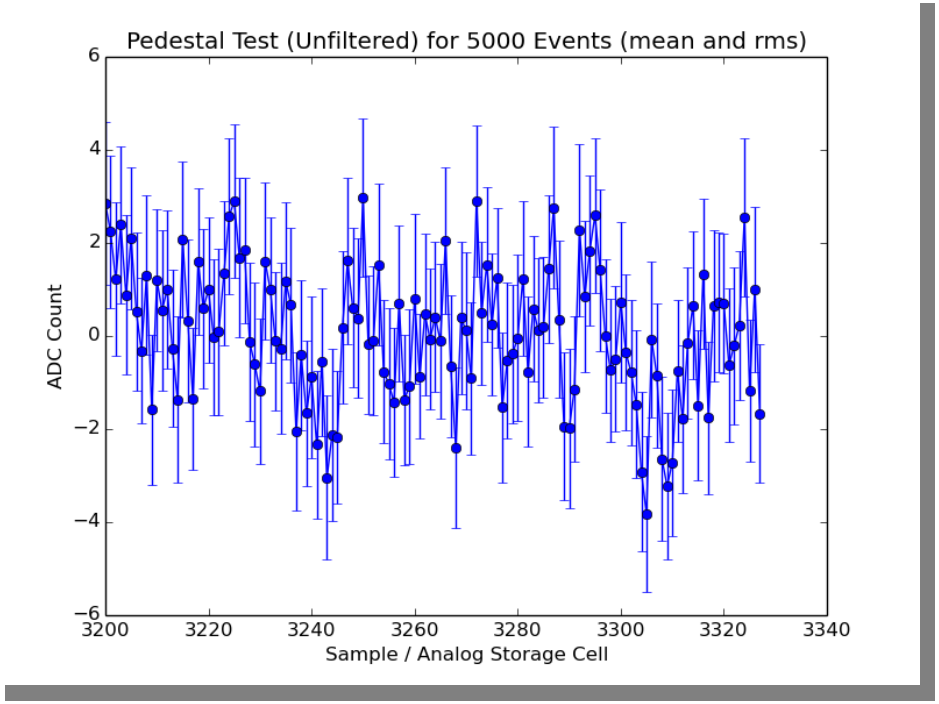


PRODUCTION_TEST:
2) SINE_SCAN [2/2]

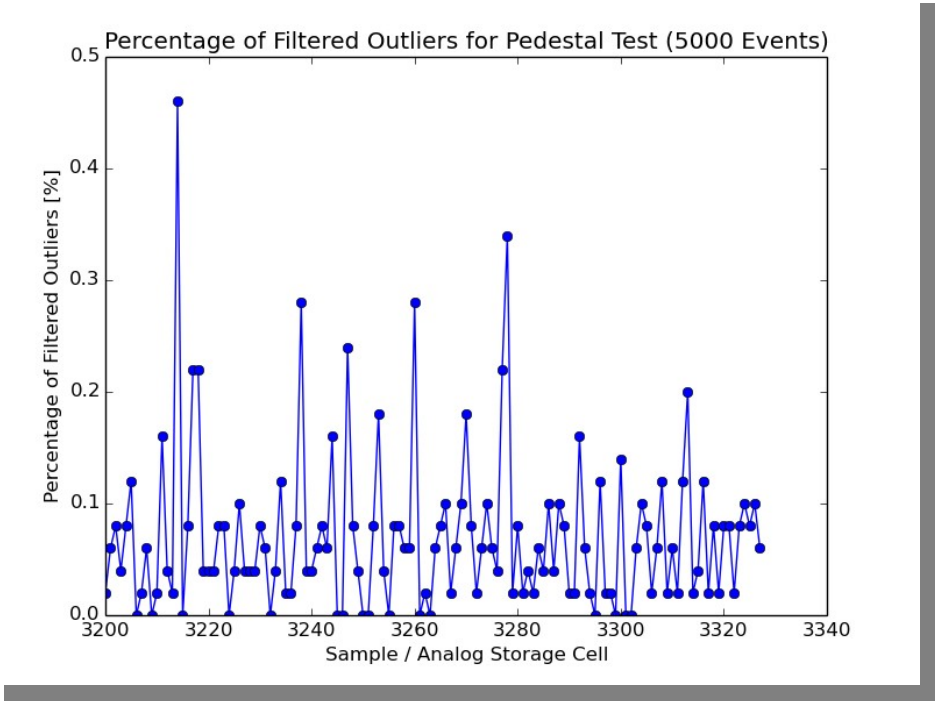


PRODUCTION TEST:
3) PEDESTAL_TEST [1/3]

Errorbar plot of Pedestals



Outlier Detection Algorithm may be used to help determine defective chips maybe



PRODUCTION TEST:
3) PEDESTAL_TEST [2/3]

Filtering Outliers: z-score and Chebychev's Theorem

- Z-score

$$z_i = \frac{\left|\left(x_i - mean\left(x\right)\right)\right|}{std\left(x\right)}$$

  - Referred to as a standardized value and denotes number of standard deviations x_i is from mean
- Chebyshev's theorem
  - For any data set, at least $1 - 1/z^2$ of data values must be within z standard deviations from mean, where z minus any value is greater than 1
  - Any Distribution
    - For z = 2: At least 75% of values are there
    - For z = 3: At least 89% of values are there
    - For z = 4: At least 94% of values are there
    - For z = 5: At least 96% of values are there

PRODUCTION TEST:
3) PEDESTAL_TEST [3/3]

Filtering Outliers: REJECT_OUTLIERS Algorithm

REJECT_OUTLIERS(data, m=6)

```
1.  for i = 0 to length(data)
2.      num[i] = abs(data[i] – median(data))
2.  mdev = median(num)
3.  if (mdev)
4.      for i = 0 to length(data)
5.          z_modified[i] = num[i]/mdev
6.  else z_modified = 0
7.  for i = 0 to length(data)
8.          if (z_modified[i] < m)
9.              filtered_data.append(data[i])
10. return filtered_data
```

O(n) run-time

Iglewicz-Hoaglin Method

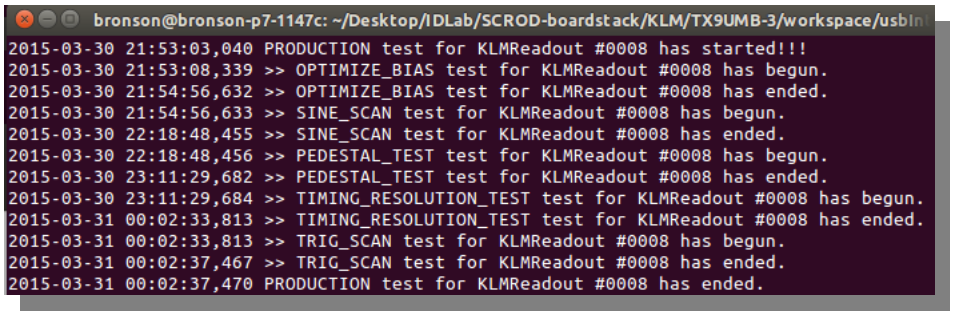
- median(x) can be used as a measure of location when distribution is skewed due to attached outliers
- mdev is called the median absolute deviation because it is basically:

$$mdev(x) = median(|(x_i - median(x))|)$$

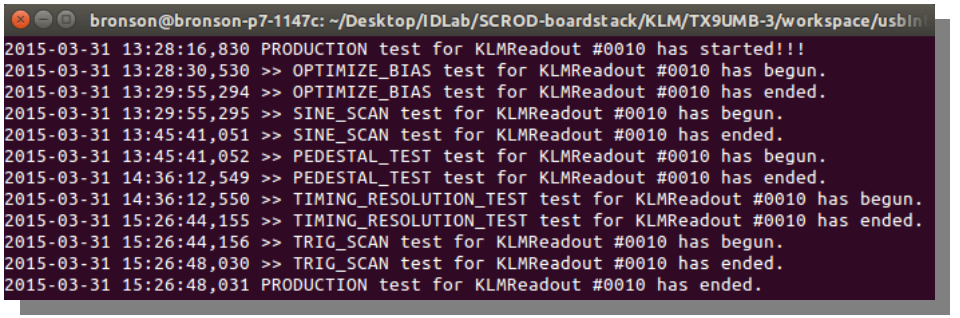
$$z_i = \frac{|(x_i - median(x))|}{mdev(x)}$$

PRODUCTION_TEST:
Parallel Processing

- **BEFORE:** Data Acquisition & Data Processing were Sequential
  - OPTIMIZE_BIAS (5 Events, 4 Windows)
    - VANI's Comp: 0 hour(s), 21 min(s), 21 sec(s)
    - Bronson's Comp: 0 hour(s), 18 min(s), 9 sec(s)
  - SINE_SCAN (5 Events, 508 Windows)
    - VANI's Comp: 4 hour(s), 58 min(s), 23 sec(s)
    - Bronson's Comp: 4 hour(s), 2 min(s), 16 sec(s)
  - PEDESTAL_TEST (5k Events, 4 Windows)
    - VANI's Comp: 9 hour(s), 24 min(s), 40 sec(s)
    - Bronson's Comp: 8 hour(s), 51 min(s), 9 sec(s)
  - TOTAL
    - VANI's Comp: **14 hour(s), 44 min(s), 24 sec(s)**
    - Bronson's Comp: **13 hour(s), 11 min(s), 34 sec(s)**



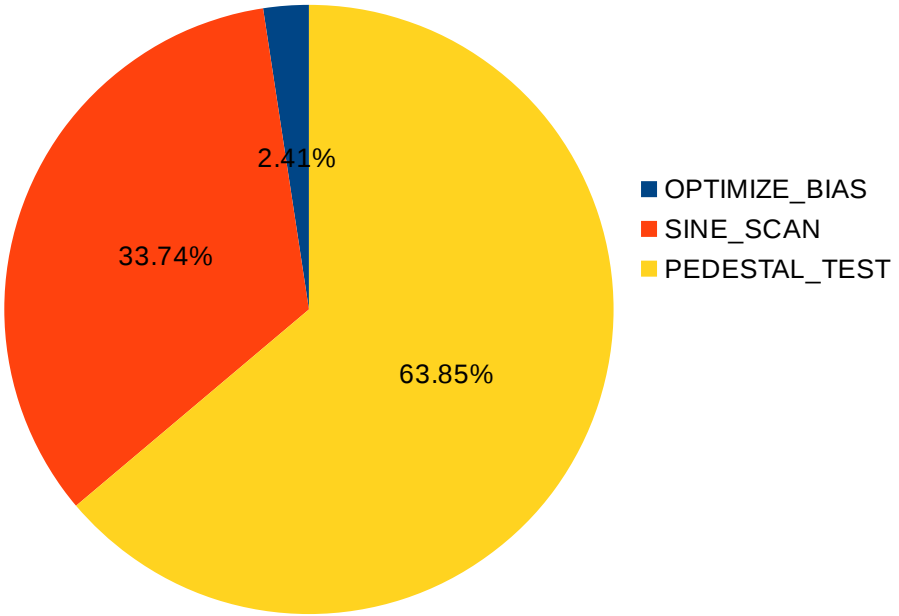
- **NOW:** Data Acquisition and Data Processing are in Parallel
  - OPTIMIZE_BIAS
    - VANI's Comp:
    - Bronson's Comp: 0 hour(s), 14 min(s), 35 sec(s)
  - SINE_SCAN
    - VANI's Comp:
    - Bronson's Comp: 2 hour(s), 37 min(s), 40 sec(s)
  - PEDESTAL_TEST
    - VANI's Comp:
    - Bronson's Comp: 8 hour(s), 25 min(s), 29 sec(s)
  - TOTAL
    - VANI's Comp: **1 Gig Memory Could not Handle it**
    - Bronson's Comp: **11 hour(s), 19 min(s), 48 sec(s)**



PRODUCTION_TEST:
Run-Time

10 TARGETX ASICs with SCROD (revA) as Readout

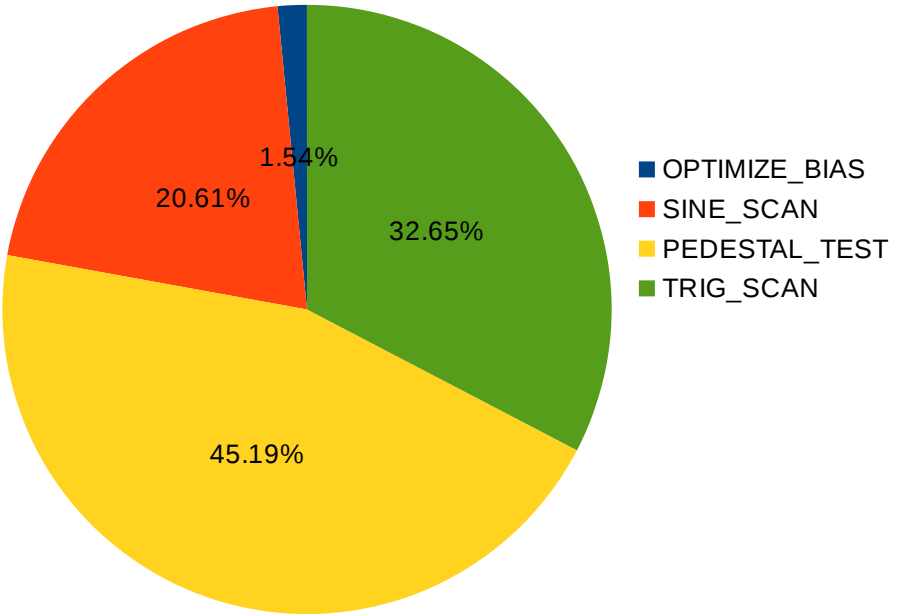
Including MotherBoard Testing



- **Data Acquisition & Data Processing without RHIC**
  - VANI's Comp (Sequential): **14 hour(s), 44 min(s), 24 sec(s)**
  - Bronson's Comp (Parallel): **11 hour(s), 19 min(s), 48 sec(s)**

10 TARGETX ASICs with SCROD (revA) as Readout

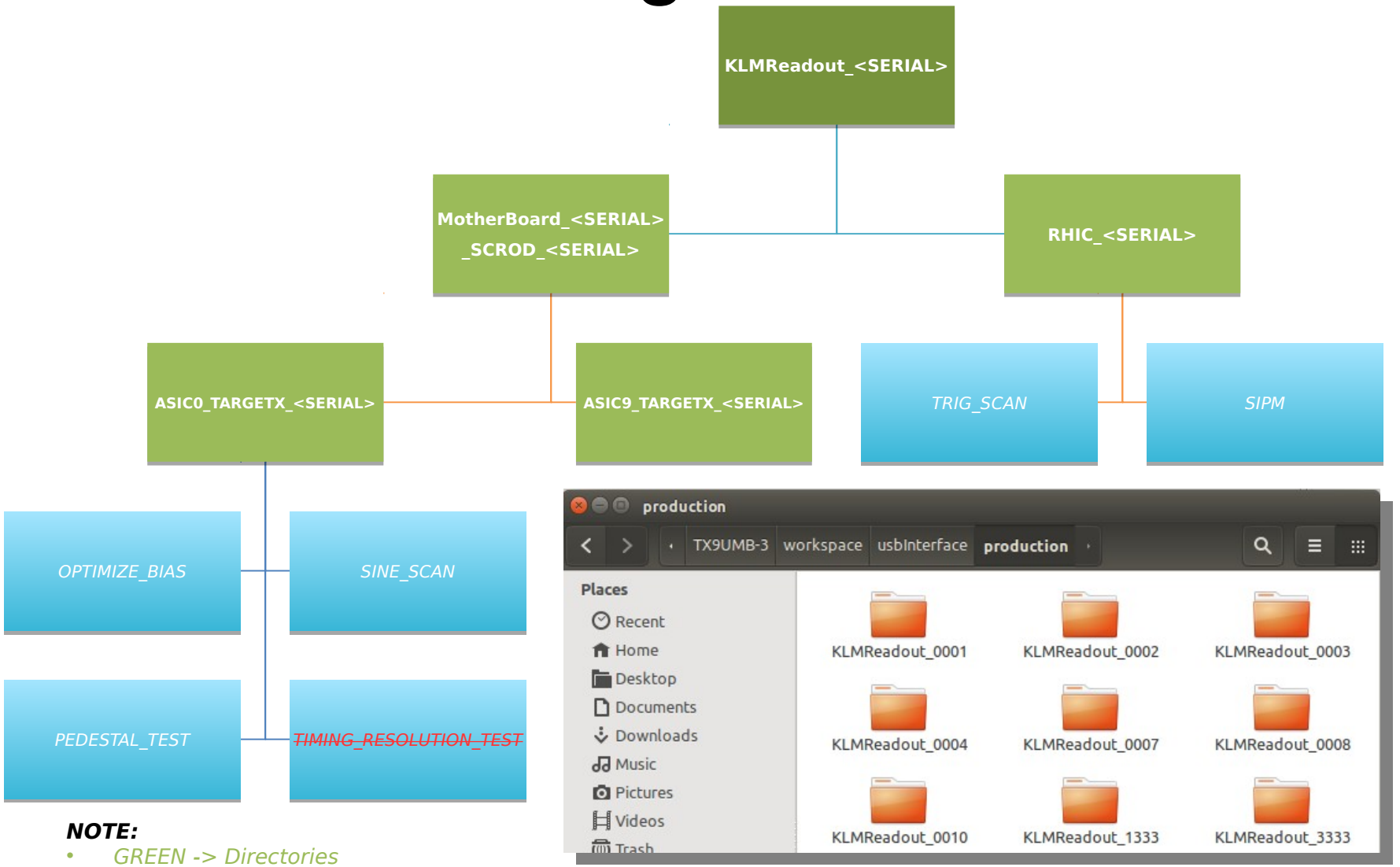
Including MotherBoard and RHIC Board Testing



- **Data Acquisition & Data Processing with RHIC**
  - VANI's Comp (Sequential): **21 hour(s), 8 min(s), 12 sec(s)**
  - Bronson's Comp (Parallel): **17 hour(s), 43 min(s), 36 sec(s)**

Note: Not Including Testing the Health of Board which includes Temperature and Current

PRODUCTION_TEST: Storing of Data



NOTE:

- *GREEN -> Directories*
- *TEAL -> Test Directories*

PRODUCTION_TEST: Logging Data [1/3]

DESCRIPTION: *OPTIMIZE_BIAS, SINE_SCAN, PEDESTAL_TEST*

DESCRIPTION (~/Desktop/IDLab/SCROD-boardstack)

Open Save Undo

DESCRIPTION

```
BIASREV = 1
OPERATOR = Bronson_Edralin
DATETIME = 2015.03.31_13.29.55
TEST = SINE_SCAN

BOARD:
>> ASIC = TARGETX
>> ASICno = 2
>> ASIC_Serial = 0025
>> ASIC_CH16_DC_Coupled = True
>> MotherBoard = KLM_TX_9U_MB_RevB
>> MotherBoard_Serial = 2343
>> SCROD = SCROD_revA4
>> SCROD_Serial = 5
>> RHIC = KLM_RHIC_RevB
>> RHIC_Serial = 4323

INPUT:
>> InputSignal = SINUSOID
>> InputAmplitude_VPP = 900e-03
>> InputFrequency_Hz = 40e06
>> InputBurst = OFF
>> InputOffset_V = 0
>> InputBurstDelay_us = 0
>> InputBurstCycles = 3
>> InputBurstTrigger = INT
>> OutputImpedance = 50

PARAMETER:
>> Min Window = 0
>> Max Window = 508
>> Number of Events = 5
>> Bias Register Name = NONE
>> Bias Register Value Start = 0
>> Bias Register Value Interval = 1
>> Bias Register Value End = 1
```

Plain Text Tab Width: 8 Ln 37, Col 1 INS

DESCRIPTION: *TRIG_SCAN, SIPM*

*DESCRIPTION (~/Desktop/IDLab/SCROD-boardstack)

Open Save Undo

DESCRIPTION *DESCRIPTION

```
BIASREV = 1
OPERATOR = Bronson_Edralin
DATETIME = 2015.03.31_15.26.44
TEST = TRIG_SCAN

>> ASIC = TARGETX
>> ASIC0_Serial =
>> ASIC1_Serial =
>> ASIC2_Serial = 0025
>> ASIC3_Serial =
>> ASIC4_Serial =
>> ASIC5_Serial =
>> ASIC6_Serial =
>> ASIC7_Serial =
>> ASIC8_Serial =
>> ASIC9_Serial =
>> ASIC0_CH16_DC_Coupled = True
>> ASIC1_CH16_DC_Coupled = True
>> ASIC2_CH16_DC_Coupled = True
>> ASIC3_CH16_DC_Coupled = True
>> ASIC4_CH16_DC_Coupled = True
>> ASIC5_CH16_DC_Coupled = True
>> ASIC6_CH16_DC_Coupled = True
>> ASIC7_CH16_DC_Coupled = True
>> ASIC8_CH16_DC_Coupled = True
>> ASIC9_CH16_DC_Coupled = True
>> MotherBoard = KLM_TX_9U_MB_RevB
>> MotherBoard_Serial = 2343
>> SCROD = SCROD_revA4
>> SCROD_Serial = 5
>> RHIC = KLM_RHIC_RevB
>> RHIC_Serial = 4323

INPUT:
>> InputSignal = SIPM
>> HighVoltageValue_V = 71.1
>> HighVoltageStatus = ON
```

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PRODUCTION_TEST: Logging Data [2/3]

Optimized SSToutFB values properly logged (Note: only ASIC #2 connected)

optimizebias.csv - LibreOffice Calc

Liberation Sans | 10 | J30

	A	B	C	D	E	F	G	H	I
1	FileType:	OPTIMIZE_BIAS							
2	FileRev:	1							
3	BiasRev:	1							
4									
5	ASIC:	TARGETX							
6	RHIC:	KLM_RHIC_RevB							
7	MotherBoard:	KLM_TX_9U_MB_RevB							
8	SCROD:	SCROD_revA4							
9									
10	DateTime	ASICno	ASIC_Serial	ASIC_CH16_DC_Coupled	KLMReadout_Serial	MotherBoard_Serial	RHIC_Serial	SCROD_Serial	SSToutFB-75_Value
11	2015.04.09_21.13.50	0	003A	False	3	none	none	5	63
12	2015.04.09_21.16.04	1	42	False	3	none	none	5	63
13	2015.04.09_21.18.10	2	25	True	3	none	none	5	57
14	2015.04.09_21.20.17	3	001A	False	3	none	none	5	60
15	2015.04.09_21.22.24	4	000e	False	3	none	none	5	60
16	2015.04.09_21.24.34	5	39	False	3	none	none	5	63
17	2015.04.09_21.26.40	6	003d	False	3	none	none	5	56
18	2015.04.09_21.28.48	7	001d	False	3	none	none	5	53
19	2015.04.09_21.30.56	8	003b	False	3	none	none	5	57
20	2015.04.09_21.33.04	9	003F	False	3	none	none	5	56

PRODUCTION_TEST: Logging Data [3/3]

Production_log with DateTime logged