

6

5

4

3

2

1

D

C

B

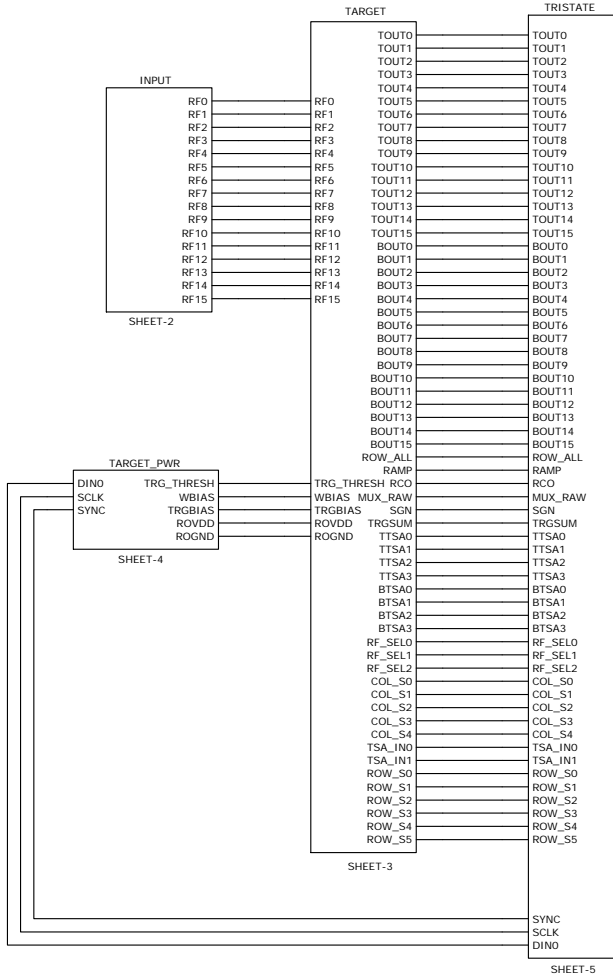
A

D

C

B

A



As Built

Layer Definitions

- Top Copper routing
- Layer 2 split AGND/GND
- Layer 3 split A.5V
- Bottom Copper split Vped/D2.5V fill

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TITLE: TARGET ASIC Daughtercard

IDL_10_005



Design: GSV

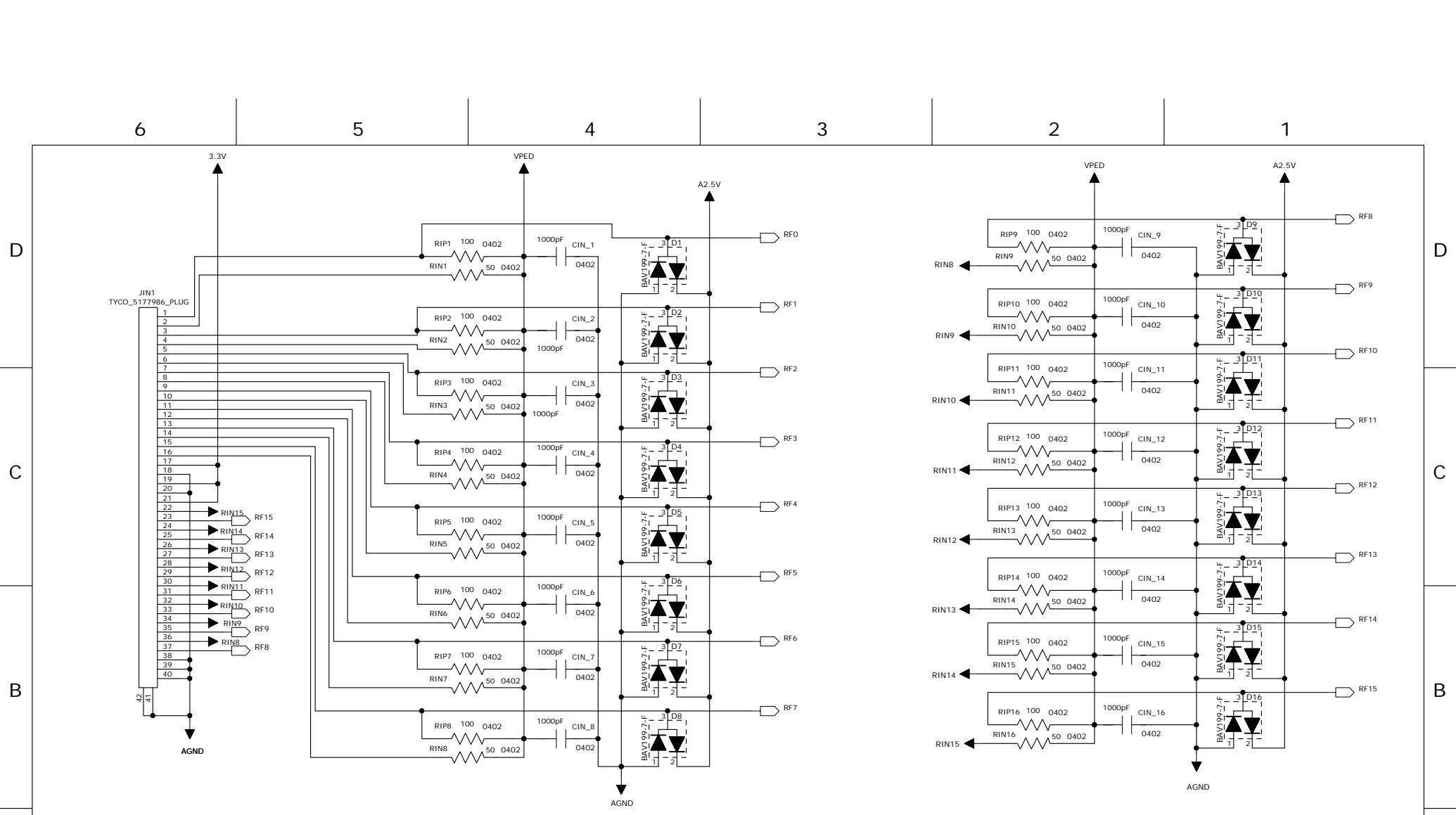
Page Description: TOP Block DC_TARGET_RevA

REV: A

DATED: 29-DEC-2010


[TOP]

SHEET: 1 OF 5



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TITLE: TARGET ASIC Daughtercard IDL_10_005

	Design:	Page Description:	REV:
	GSV	Input Block DC_TARGET_RevA	A

DATED: 28-DEC-2010 [TOP] SHEET: 2 OF 5

6 5 4 3 2 1

D

C

B

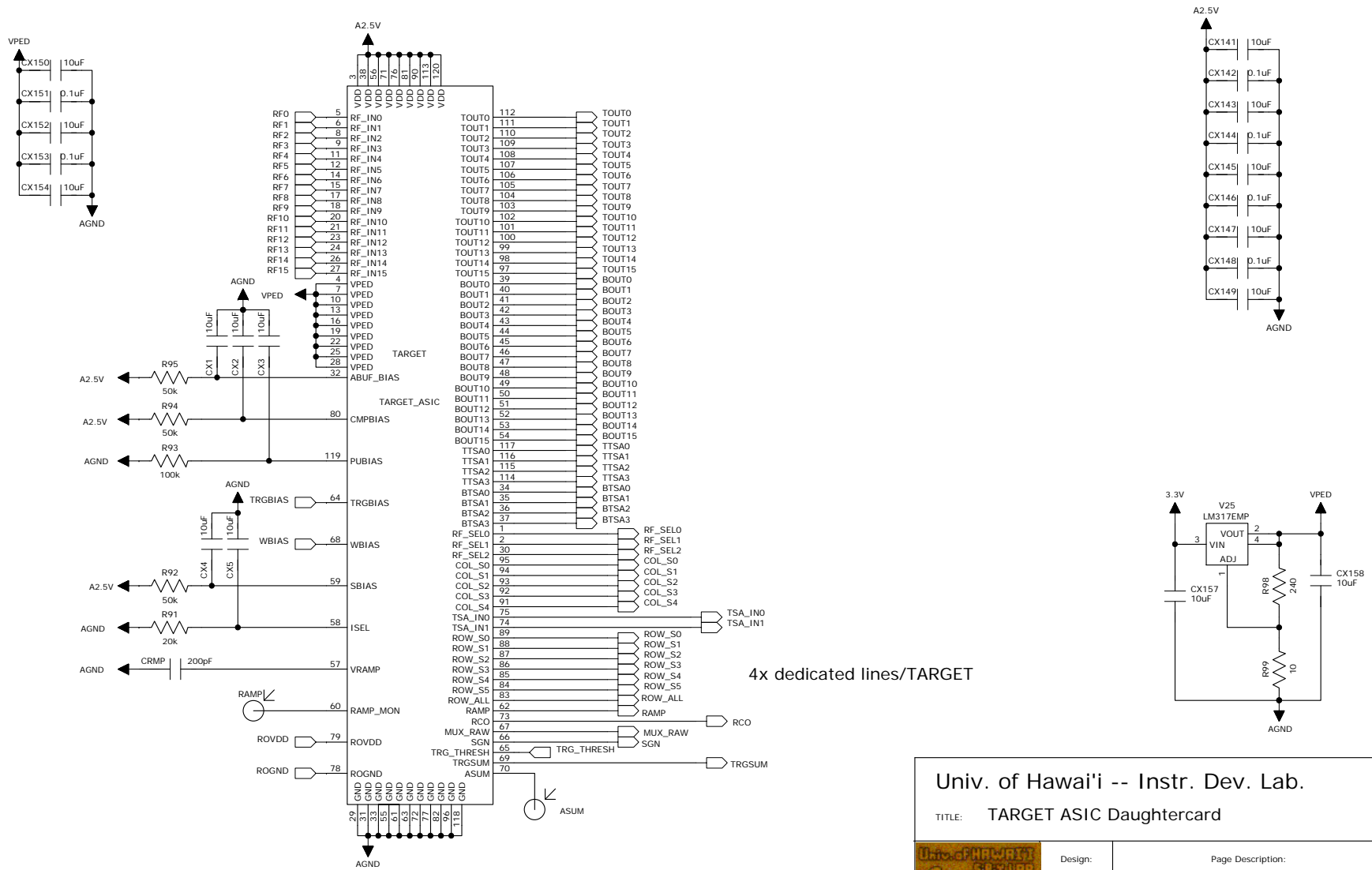
A

D


C

B

A



4x dedicated lines/TARGET

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TITLE: TARGET ASIC Daughtercard			
	Design:	Page Description:	REV:
	GSV	TARGET Block	A
DATED: 23-DEC-2010		[TARGET]	SHEET: 3 OF 5

6

5

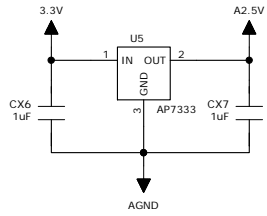
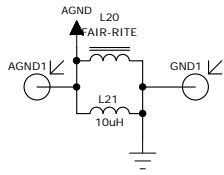
4

3

2

1

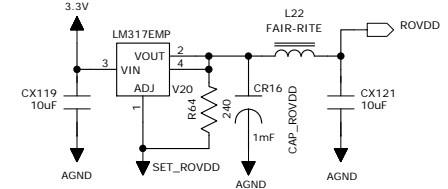
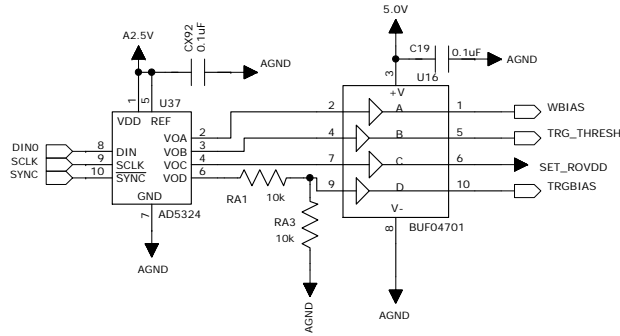
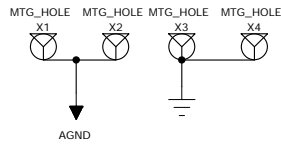
D



C

B

A

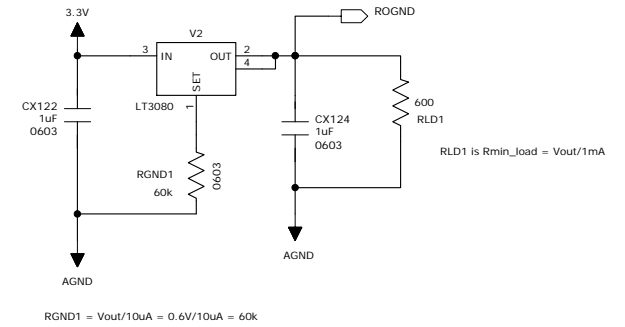


D

C

B

A



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TITLE: TARGET ASIC Daughtercard



Design: GSV

Page Description: Power and DAC Block

REV: A

DATED: 28-DEC-2010

[TARGET_PWR]

SHEET: 4 OF 5

D

D

C

C

B

B

A

A

6

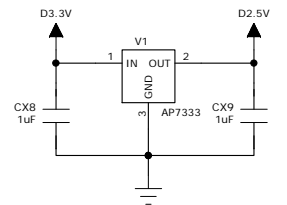
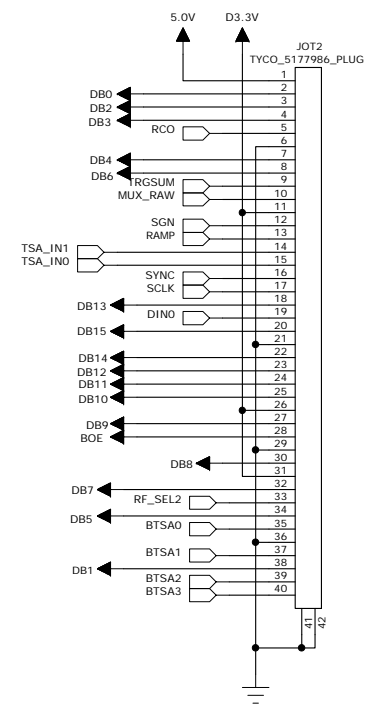
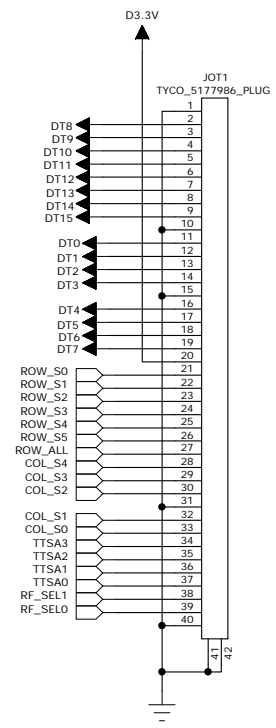
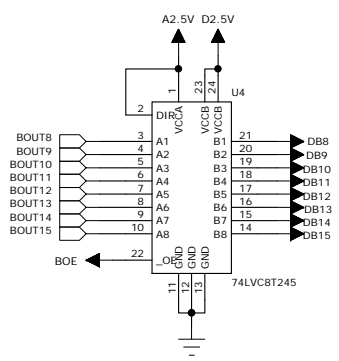
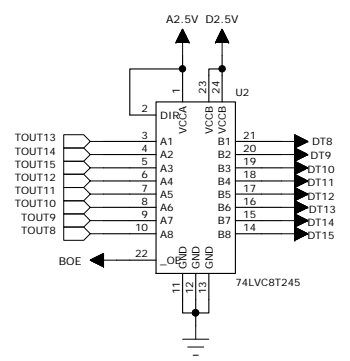
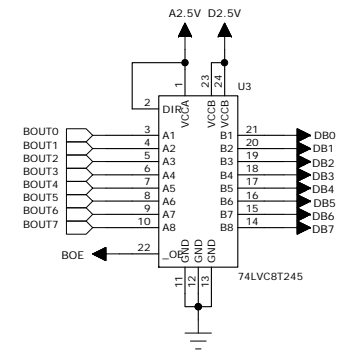
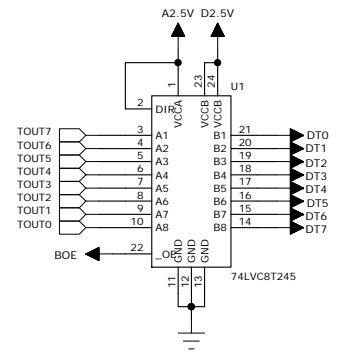
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4

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2

1



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TITLE: TARGET ASIC Daughtercard

	Design:	Page Description:	REV:
	GSV	Tristate Output Data Select	A

DATED: 28-DEC-2010 [TRISTATE] SHEET: 5 OF 5