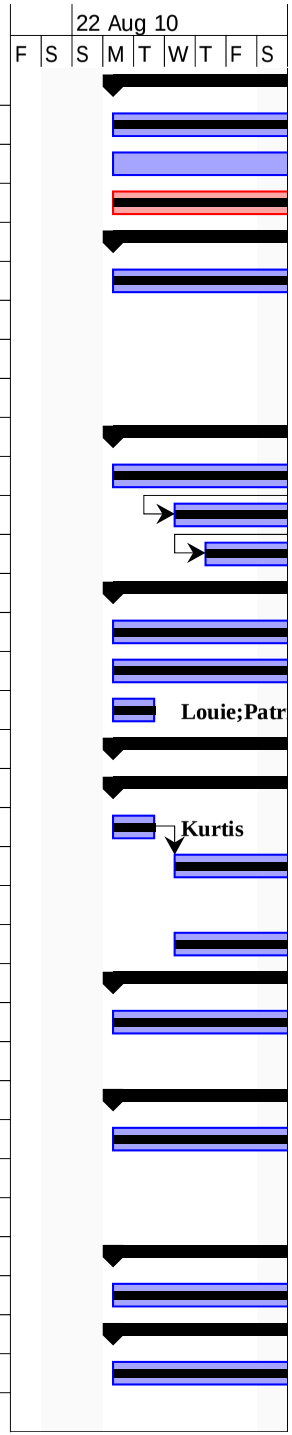
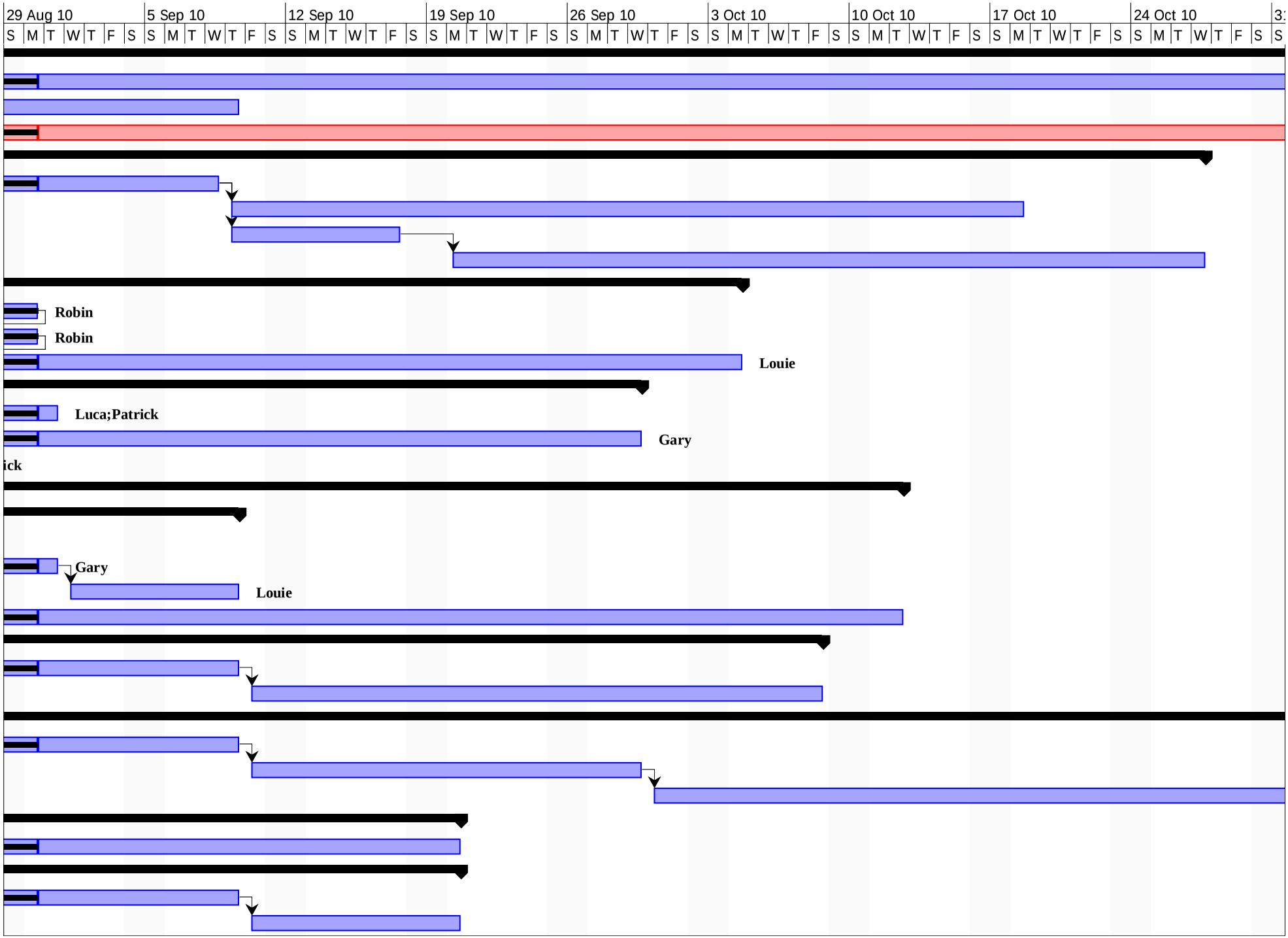
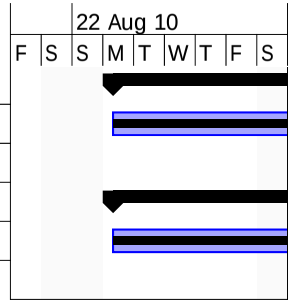
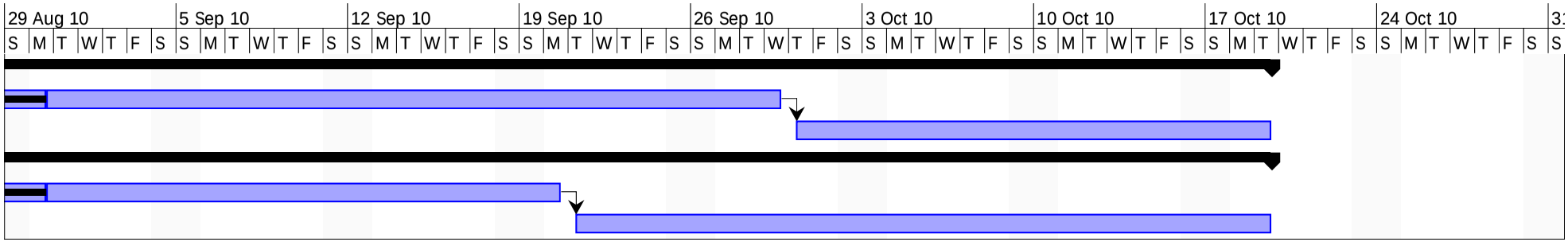
		Name	Duration	Finish	Predecessors	Resource Names
1		**iTOP development**	**60 days**	**11/12/10 5:00 PM**		
2		BLAB3B ASIC	60 days	11/12/10 5:00 PM		
3		DXF of new BLAB3 cards	14 days	9/9/10 5:00 PM		
4		iTOP beamtest (Kurtis capture)	65 days	11/19/10 5:00 PM		
5		**xFEL**	**48 days?**	**10/27/10 5:00 PM**		
6		Next beam run	13 days?	9/8/10 5:00 PM		
7		ROE2 board	28 days	10/18/10 5:00 PM	6	
8		2x more 8x fiber Tx/Rx boards	7 days	9/17/10 5:00 PM	6	
9		STURM2 readout module	28 days	10/27/10 5:00 PM	8	
10		**KLM**	**31 days**	**10/4/10 5:00 PM**		
11	✔	single amp cards	6 days	8/30/10 5:00 PM		Robin
12	✔	15-channel amp board	4 days	8/30/10 5:00 PM	11	Robin
13		TARGET readout board	28 days	10/4/10 5:00 PM	12	Louie
14		**ARA**	**28 days**	**9/29/10 5:00 PM**		
15		Testbed Firmware	7 days	8/31/10 5:00 PM		Luca;Patrick
16		IRS2	28 days	9/29/10 5:00 PM		Gary
17	✔	USB prog/IF board	2 days	8/24/10 5:00 PM		Louie;Patrick
18		**mTC**	**37 days**	**10/12/10 5:00 PM**		
19		**BLAB3A ASIC**	**14 days**	**9/9/10 5:00 PM**		
20	✔	Gain/BW OK?	2 days	8/24/10 5:00 PM		Kurtis
21		Layout complete	5 days	8/31/10 5:00 PM	20	Gary
22		Eval board?	7 days	9/9/10 5:00 PM	21	Louie
23		Moduleschematic	35 days	10/12/10 5:00 PM		
24		**ATF2 coded aper xRay read...**	**35 days**	**10/8/10 5:00 PM**		
25		STURM2packaging	14 days	9/9/10 5:00 PM		
26		Schematics for readout module	21 days	10/8/10 5:00 PM	25	
27		**LAPPD**	**56 days**	**11/8/10 5:00 PM**		
28		CHAMP test board - schematics	14 days	9/9/10 5:00 PM		
29		CHAMP test board - layout	14 days	9/29/10 5:00 PM	28	
30		BLAB-based readout board?	28 days	11/8/10 5:00 PM	29	
31		**US CTA**	**21 days**	**9/20/10 5:00 PM**		
32		TARGET2 ASIC	21 days	9/20/10 5:00 PM		
33		**Lightspin**	**21 days**	**9/20/10 5:00 PM**		
34		debug LARC module	14 days	9/9/10 5:00 PM		
35		Initial sensors for test	7 days	9/20/10 5:00 PM	34	




29 Aug 10
5 Sep 10
12 Sep 10
19 Sep 10
26 Sep 10
3 Oct 10
10 Oct 10
17 Oct 10
24 Oct 10
S M T W T F S
Robin
Robin
Louie
Luca;Patrick
Gary
ick
Gary
Louie

		Name	Duration	Finish	Predecessors	Resource Names
36		**SSL XS MCP**	**42 days**	**10/19/10 5:00 PM**		
37		CSA design study	28 days	9/29/10 5:00 PM		
38		CSA layout	14 days	10/19/10 5:00 PM	37	
39		**ANITA3**	**42 days**	**10/19/10 5:00 PM**		
40		SHORT revision	21 days	9/20/10 5:00 PM		
41		LAB4 ASIC	21 days	10/19/10 5:00 PM	40	




29 Aug 10
5 Sep 10
12 Sep 10
19 Sep 10
26 Sep 10
3 Oct 10
10 Oct 10
17 Oct 10
24 Oct 10
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