August 10, 2021

University of Hawaii: ID-Lab Visit

Larry Ruckman
TID-ID Electronic Systems Department Head

U.S. DEPARTMENT OF ENERGY
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

Who am I? (Part 1 of 2)

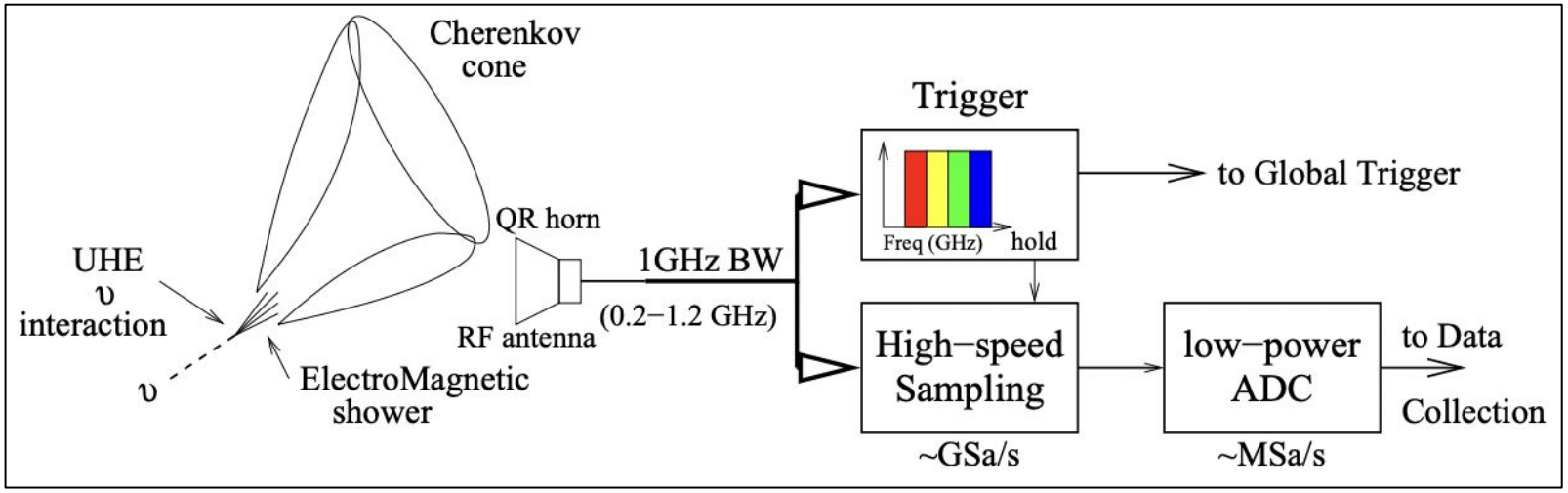
- Originally from Sandy, Utah
- Came to Hawaii on a cheerleading scholarship (2003 - 2005)

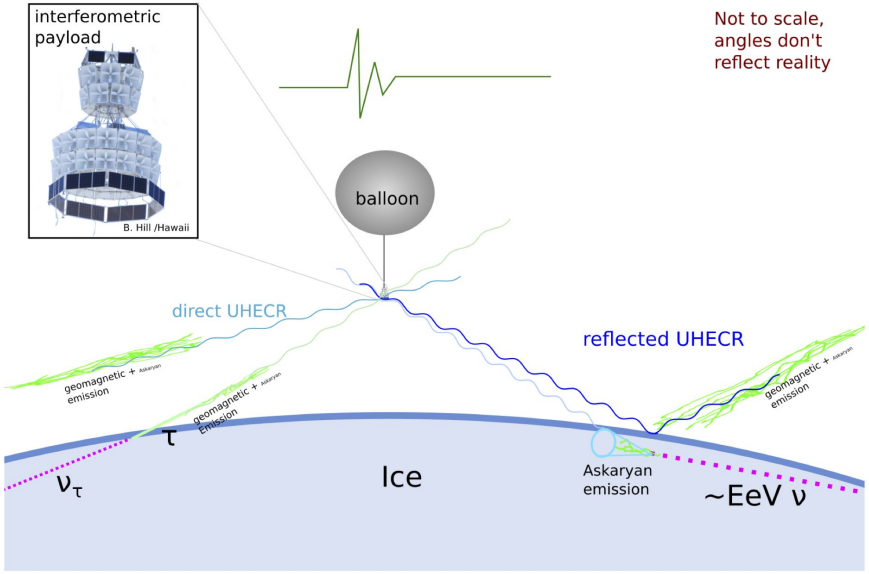
Who am I? (Part 2 of 2)

- B.S. in Physics (2003 - 2007)
- M.S in Physics (2008 - 2010)
  - Gary Varner was my graduate advisor
- Worked in the ID-lab the entire time at Hawaii

ID-Lab Projects: ANITA

- Developed the RF digitizing boards and RF triggering boards for the ANITA flight





ID-Lab Projects: A lot of ASIC Testing

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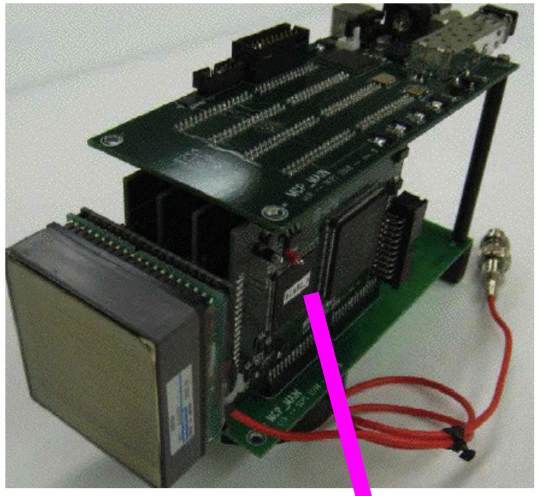
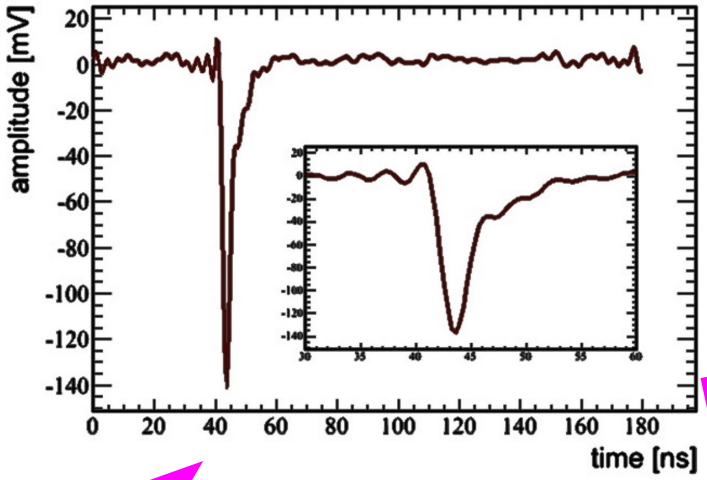
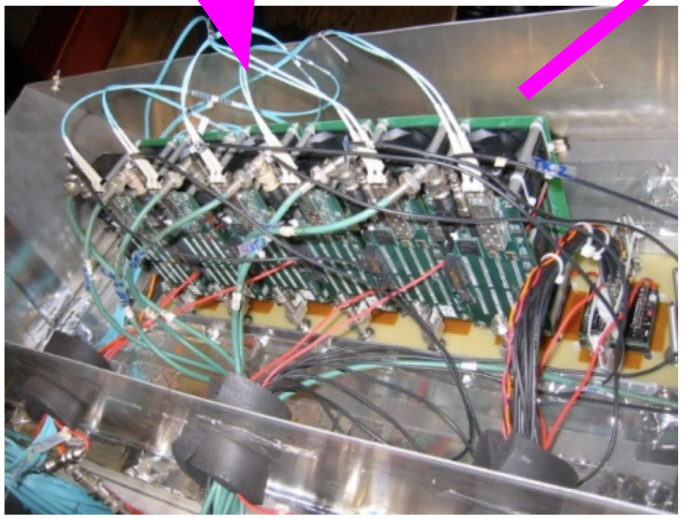
- The Large Analog Bandwidth Recorder and Digitizer with Ordered Readout (LABRADOR) ASIC
  - Nucl Instrum Meth A Vol. 583, 2007, pp. 447-460
- The PRO1 ASIC for Fast Wilkinson Encoding
  - JINST 3:P12003,2008
- A Monolithic Time Stretcher for Precision Time Recording
  - JINST2:P04006,2007
- The First version Buffered Large Analog Bandwidth (BLAB1) ASIC for high luminosity collider and extensive radio neutrino detectors
  - Nucl Instrum Meth A Vol. 591, 2008, pp 534-545
- Sub-10ps Monolithic and Low-power Photodetector Readout
  - Nucl Instrum Meth A Vol. 602, No. 1, 2009, pp. 438-445
- TARGET: A multi-channel digitizer chip for very-high-energy gamma-ray telescopes
  - 10.1016/j.astropartphys.2012.05.016

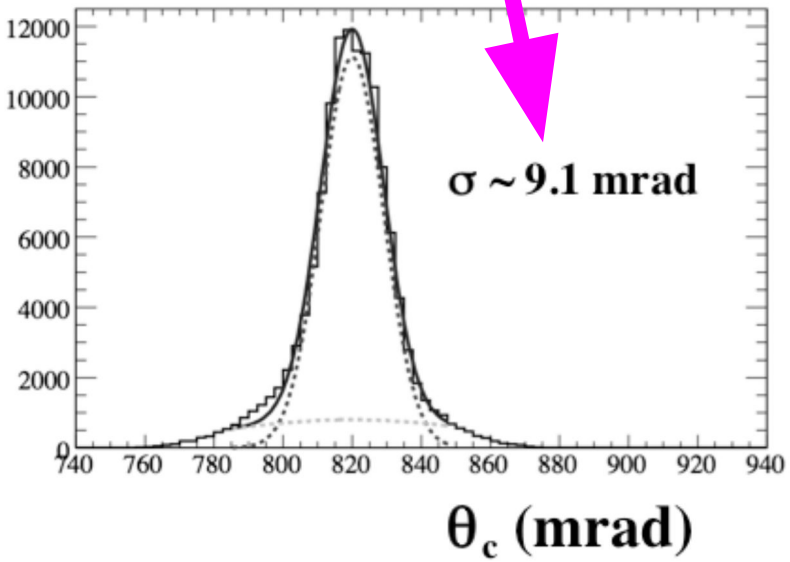
ID-Lab Projects:
Developed Electronics for fDIRC prototype at SLAC (Master Thesis)

SLAC









To quote Gary's 2010 Winter party slide ….

SLAC

Of course, people come to learn … to leave… (or not)

Associate Professor Gary Varner

Dr. Kurtis Nishimura

Larry Ruckman (Masters')
Now with Creare Inc.

Dr. Himansu Sahoo

Andrew Wong (Masters)

Jim Kennedy (6 years) → Matt Andrew

Univ. of HAWAI'I SiPix LAB

Dr. Andres Romero-Wolf
Jet Propulsion Laboratory

After Hawaii, first job was in industries

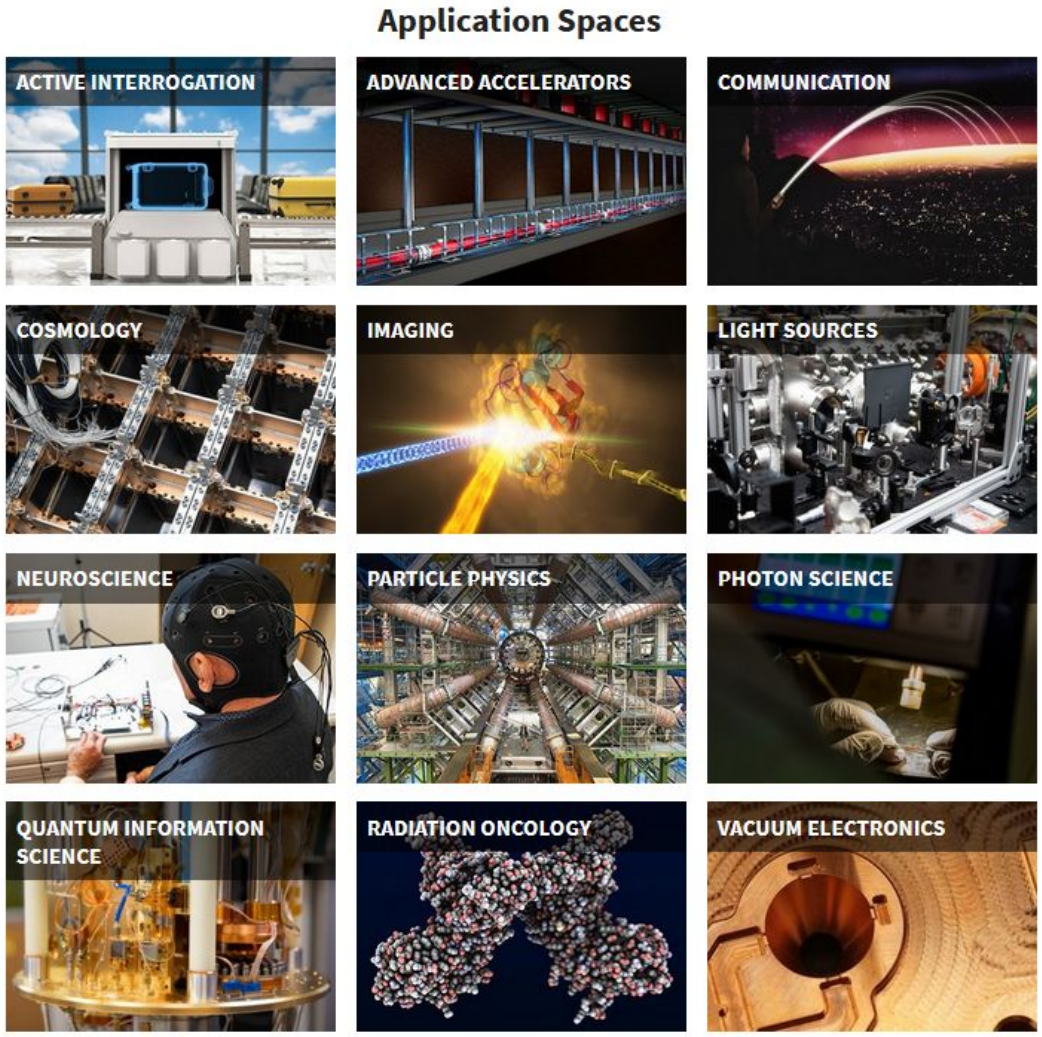
- In 2010 accepted a position as an “electrical engineer” at Creare in New Hampshire
- Worked on a lot of interesting projects
  - Battery Management Systems (BMS)
  - Compact reusable nebulizer for respiratory administration
  - MEMS-based heading sensor for towed sonar array
  - Sensorless turbo-motor (>100 krpm) drive for mass spectrometry applications
  - … and much, much more

Why did I leave New Hampshire?

- Proposed to my girlfriend (now my wife), and she did not want to live in the "snow"
- Thus, I started to apply for jobs where there is no snow
- Kurtis Nishimura (who was currently working at SLAC) recommend that I apply
- Got a job offer to be an electronics engineer in 2013
- Been working at SLAC ever since then (over 8 years)
- In July 2021, I was promoted to "department head"
  - Managing ~20 engineers/technicians

TID-ID-ES @ SLAC

- https://tid.slac.stanford.edu
  - TID: Technology Innovation Directorate
  - ID: Instrumentation Division
  - ES: Electronics Systems
- TID has broad expertise in detector and instrument creation:
  - Sensor design and fabrication
  - Integrated circuit design
  - Micro packaging and interconnects
  - Advanced analog & digital electronics
  - Low-level RF electronics
  - Data acquisition, software
  - Large-scale system integration
- Push all corners of the envelope:
  - High Speed
  - Low power
  - High channel counts
  - Small footprint
  - Large degree of integration
  - Radiation hardness
  - Advanced data movement and handling
- A lot of projects that I could talk about
  - … but I will only highlight a few of them that I am directly involved with for today's presentation



LCLS-II: High Performance Common Platform

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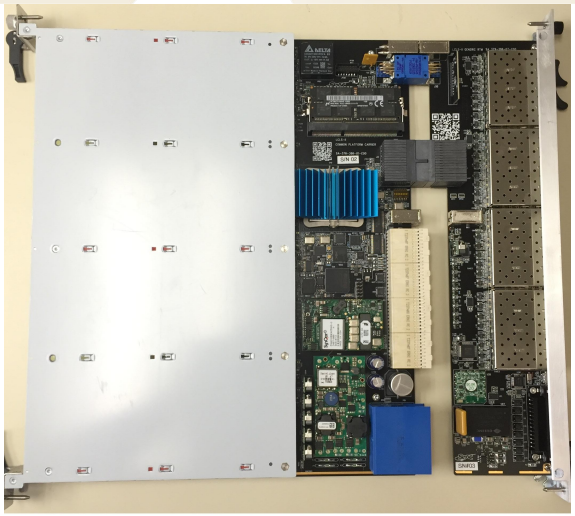
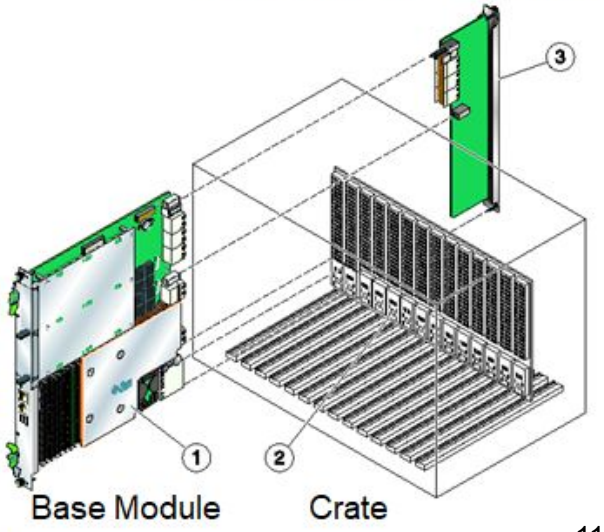
- https://lcls.slac.stanford.edu/
- Linac Coherent Light Source (LCLS)
- Developed a “common platform” that all the accelerator controls could use
  - Timing System
  - Machine Protection System (MPS)
  - Beam Length Monitor (BLEN)
  - Beam Loss monitor (BLM)
  - Beam Charge Monitor (BCM)
  - Beam Position Monitor (BPM)
- Instead of every subsystem designing their own HW/FW/SW
  - We developed a “common platform” for them to use
- Saves money/labor because less HW/FW/SW to develop and maintain
- Developed/optimized this ATCA design for LCLS-II
  - Manufactured over 600+ units
  - Used in non LCLS-II applications as well
- **Highly integrated packing solution**:
  - Includes Electrical Power distribution
  - Includes Power/Cooling Management via Intelligent Platform Management Interface (IPMI)
  - Ethernet Communication via backplane



RTM= Rear Transition Module



ATLAS ITK:
What are we trying to achieve with the lpGBT emulator?

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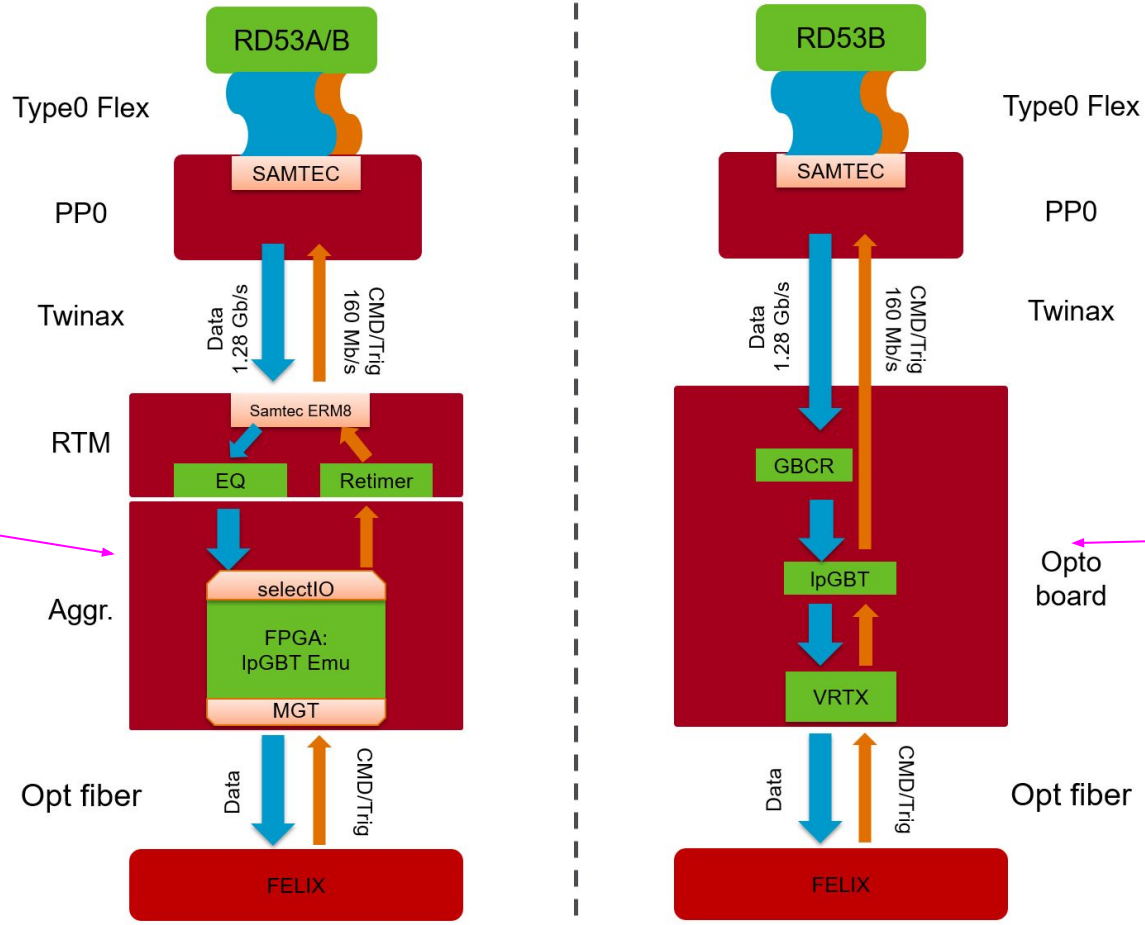
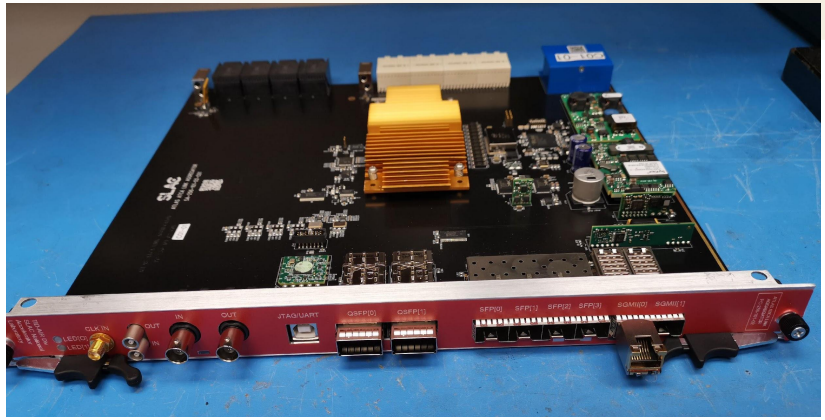


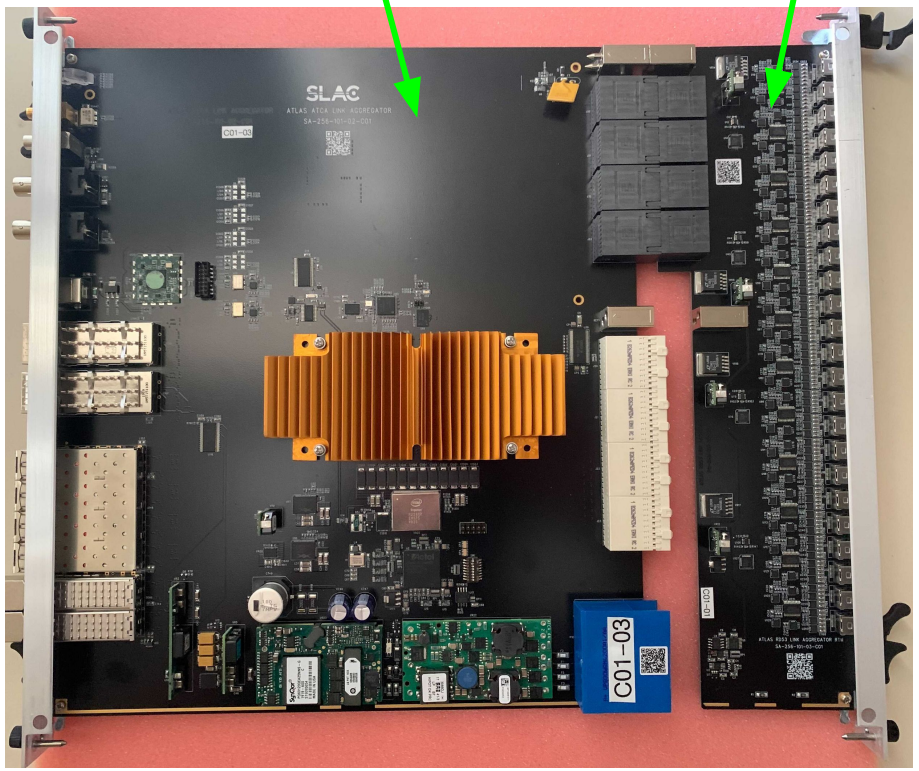
Use a FPGA to "emulate" the OptoBoard functionality as a "stopgap measure" until large OptoBoard production

Few quantities this year. Larger batch can only be expected by summer 2021

- RD53A Demonstrators need to readout up to **<u>134 data links</u>** before abundant OptoBoard availability by summer 2021

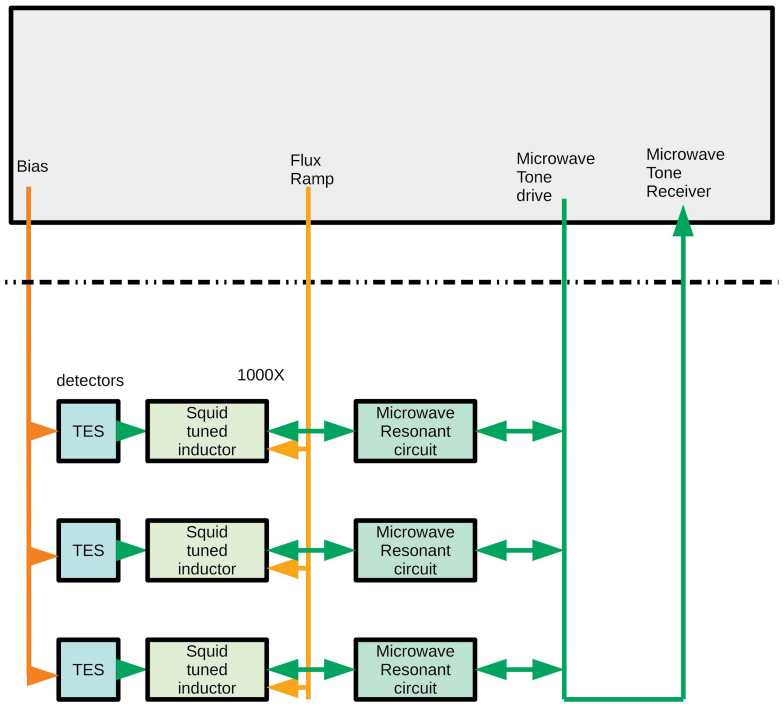
ATLAS ITK: ATCA RD53 Link Aggregator





- ASIC emulation done a a very big FPGA
  - Xilinx Kintex Ultrascale+: KU15P
- Supports up to 12 “emulated” lpGBT ASICs
  - 10.24 Gb/s per lane (122.88 Gb/s total)
- On the Rear Transition Module (RTM):
  - 96 lanes of 1.28 Gb/s AURORA
  - 32 lanes of 160 Mb/s “CMD”
- Additional 2 SFP for 1GbE only (SGMII)
  - Sideband configuration/monitoring
  - Non-data path, slow controls only
- Used as a “stop gap” measure due to OptoBoard delays
  - Modules finally arrived this summer
- Helped us debug a lot of the backend DAQ during early development
  - FELIX platform from CERN
- A lot of recycled technology from LCLS-II common platform

Microwave Multiplexing: SMuRF



Microwave multiplexing is compatible with the detector wafers for TDM

- Each TES is coupled to a SQUID loaded microwave resonator
- Acts as parametric amplifier, with TES signal imprinted on microwave signal
- High multiplexing: 500 channels / coax cable
- Excellent noise performance
- High complexity and signal processing requirements.
- 

Original concept from Kent Irwin and Ben Mates, ~2011

A lot of recycled technology from LCLS-II common platform

SMuRF Components

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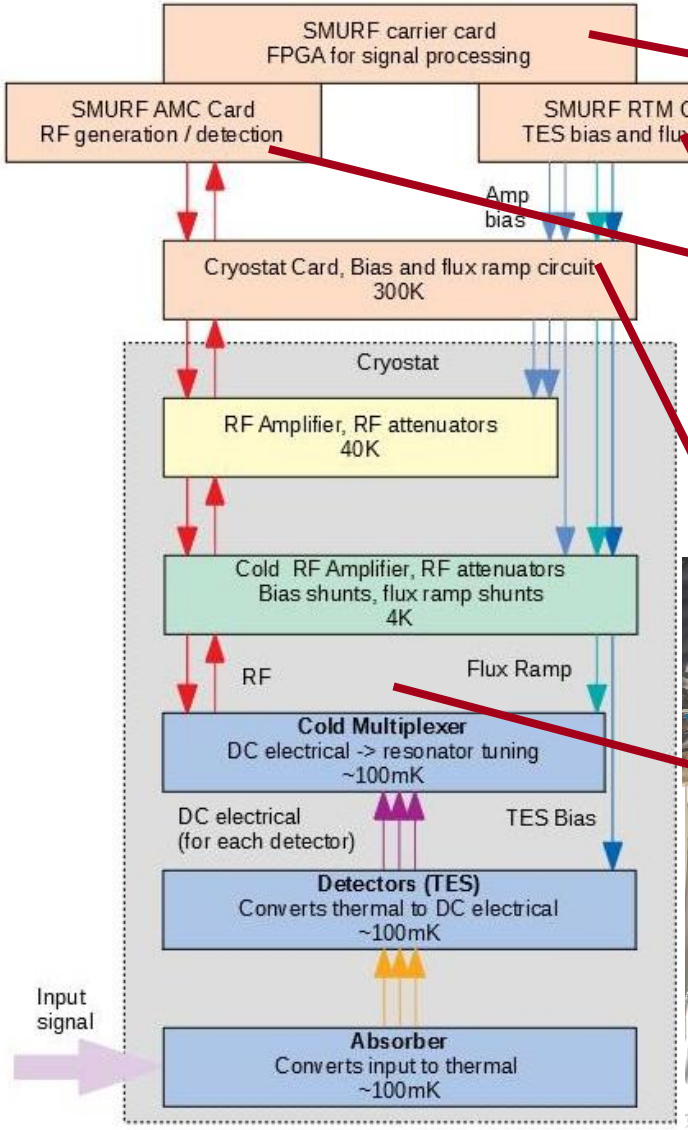
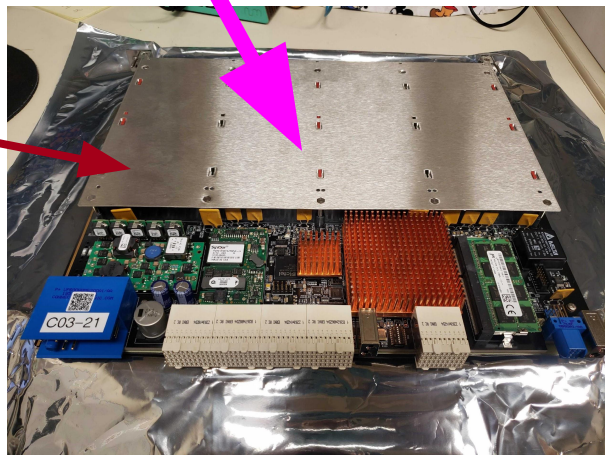
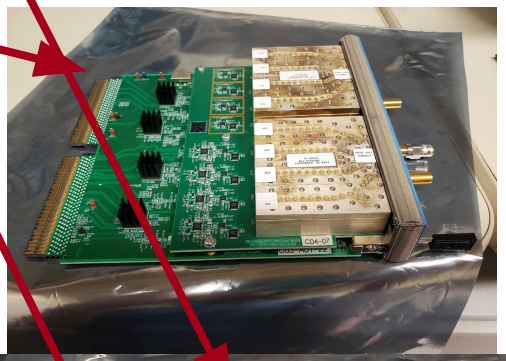
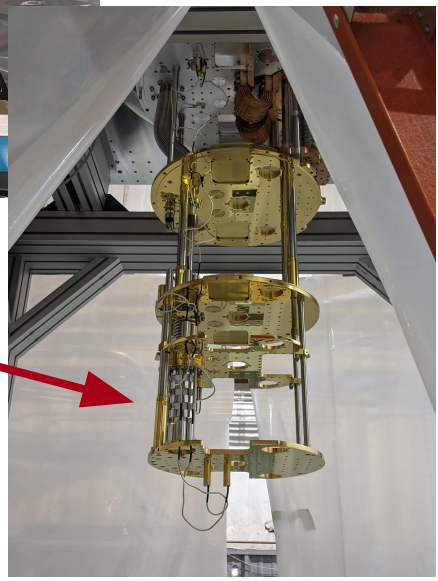






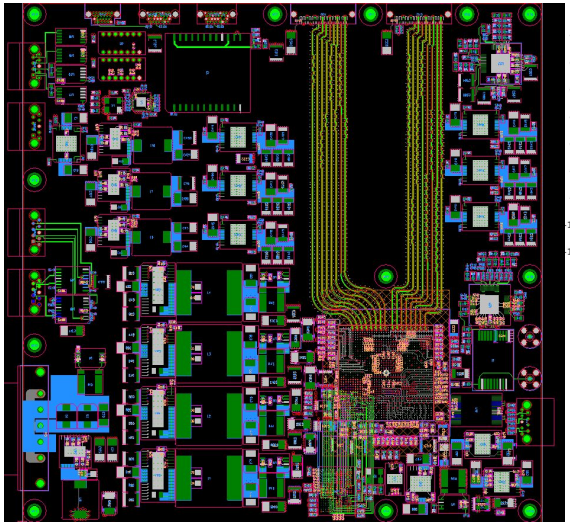


SMuRF in space!!!

Developing hardware, firmware and software for space qualified SMuRF

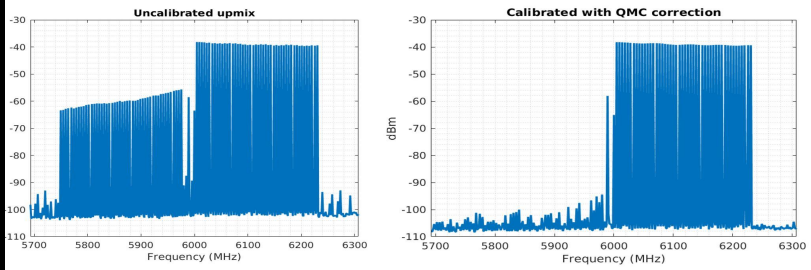
- Current NASA SAT funding targets TRL=6
- All radiation hard, flight hardware (engineering samples)
  - except RFSoC
- Radiation resistant (XQ ruggedized version) of RFSoC
- On-chip latchup mitigation through LVAUX mode
- Board level fault / latchup reset through supervisory microcontroller

Space SMuRF Breadboard



Layout to be completed at end of August 2021

Measured



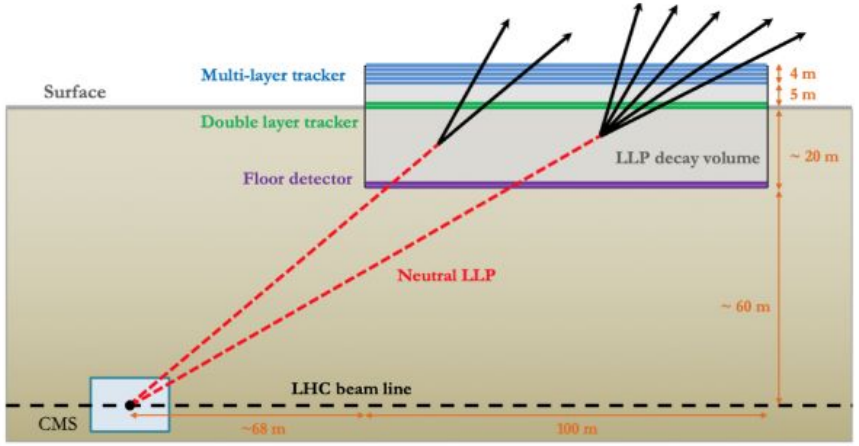
SLAC developed RF calibration algorithm greatly simplifies RF hardware

Being developed for NASA flagship missions (SMuRF will work for two out of 4 proposed missions)

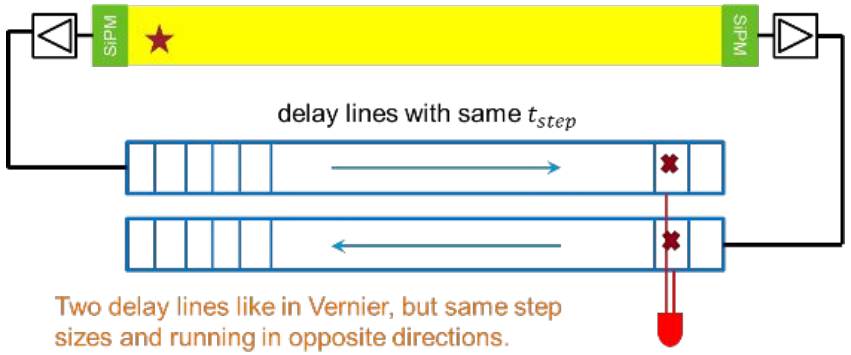
R&D on Low Latency, Largely Distributed Trigger and Data Acquisition Systems (e.g. case study: MATHUSLA)

SLAC

- Example: MATHUSLA (MAssive Timing Hodoscope for Ultra-Stable neutraL pArticles) a detector aimed at detecting long-lived particles (LLPs) originating from CMS interaction point. looking for very rare upward going tracks from CMS beam crossings
- No existing solution
- Requires an extremely largely distributed DAQ system and extreme low latency (9us)
  - Readout and triggering of 10 layers of scintillator arranged in a 10x10 grid of 10m x 10m modules sitting 60m above CMS pit
- Goal: Develop preliminary design/model of frontend readout electronics and DAQ



Front-end readout concept

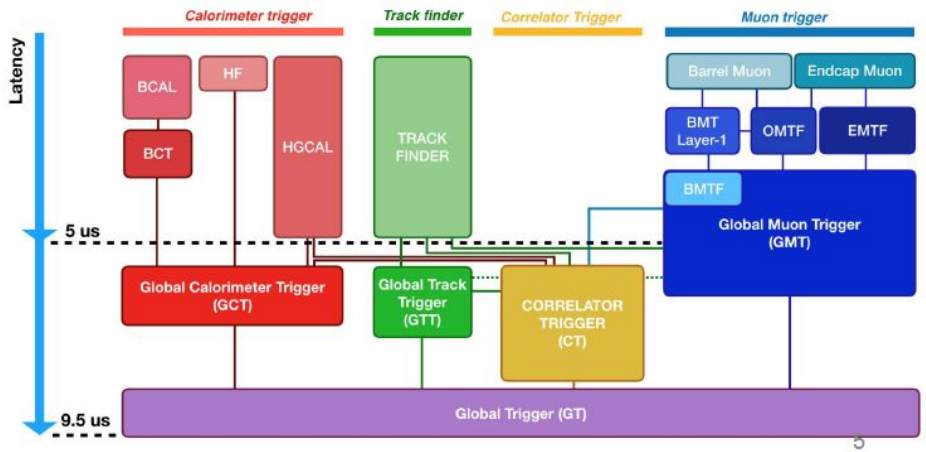


Design Study Status

- MATHUSLA treated as an “external” system to CMS
  - 9 microsec L1 Trigger requirement for Phase-2 HL-LHC
- Identified all trigger latency elements in the system
- Additional work required to design/simulate the low latency tracking and vertex triggering algorithms
- Implementing using FPGAs with 10 Gb/s point-to-point networking for triggering paths

Table 1: Trigger Latency Budget

Item	Location	Latency Description	Minimum (microsec)	Maximum (microsec)	Estimate Type
1	Particle Track	CMS p-p to MATHUSLA	0.363	1.314	Calculation
2	Cabling	Mean Hit Time in Bar to SiPM	0.070	0.100	Calculation
3	FEB	SiPM to ASIC, 1 meters	0.005	0.005	Calculation
4	FEB	ASIC to FPGA, 1 meters	0.005	0.005	Calculation
5	FEB	TDC + Time Coincidence	0.031	0.031	Simulation
6	FEB	Hit Primative Message	0.200	0.400	Simulation
7	FEB	Event Building Hits Messages	0.400	0.400	Simulation
8	FEB	PGPv4 Protocol + GT TX	0.131	0.134	Simulation
9	Cabling	Hit Primative cable, 15 meters	0.070	0.070	Calculation
10	Layer Link Agg	PGPv4 Protocol + GT RX	0.131	0.134	Simulation
11	Layer Link Agg	Event Building Hits Messages	0.013	0.213	Simulation
12	Layer Link Agg	PGPv4 Protocol + GT TX	0.131	0.134	Simulation
13	Cabling	Hit Primative cable, 1 meters	0.005	0.005	Calculation
14	Tower Link Agg	PGPv4 Protocol + GT RX	0.131	0.134	Simulation
15	Tower Link Agg	Event Building Hits Messages	0.013	0.213	Simulation
16	Tower Link Agg	PGPv4 Protocol + GT TX	0.131	0.134	Simulation
17	Cabling	Mesh Network cable,15 meters	0.070	0.070	Calculation
18	Tower Link Agg	PGPv4 Protocol + GT RX	0.131	0.134	Simulation
19	Tower Link Agg	Event Building Mesh Network	0.000	0.000	TBD
20	Tower Link Agg	3x3 Tower Track Messages	0.000	0.000	TBD
21	Tower Link Agg	PGPv4 Protocol + GT TX	0.131	0.134	Simulation
22	Cabling	Trigger Decision cable, 150 meters	0.701	0.701	Calculation
23	Trigger Link Agg	PGPv4 Protocol + GT RX	0.131	0.134	Simulation
24	Trigger Link Agg	Event Build Track Messages	0.013	0.213	Simulation
25	Trigger Link Agg	PGPv4 Protocol + GT TX	0.131	0.134	Simulation
26	Cabling	Trigger Decision cable, 1 meters	0.005	0.005	Calculation
27	System Link Agg	PGPv4 Protocol + GT RX	0.131	0.134	Simulation
28	System Link Agg	Event Build Track Messages	0.013	0.213	Simulation
29	System Link Agg	10x10 Tower Vertex Trigger Module	0.000	0.000	TBD
30	System Link Agg	Trigger Decision Messaging	0.000	0.000	TBD
31	Cabling	CMS Trigger copper cable, 150 meters	0.782	0.782	Calculation
			Total Min (microsec) 4.068	Total Max (microsec) 6.081	



Need the latency tracking and vertex triggering algorithms to be < 3 us

Highlights: Results from the Initial System Studies

- Fairly Large DAQ System
  - 800k SiPM channels
  - 10k frontend FPGA boards
  - 1,111 trigger link aggregation FPGA boards
- For trigger path for entire system
  - Processing >10 MHz of bar hits
  - < 9 us trigger latency is the technical challenge
- For the data path for entire system
  - 2.7 Gb/s (raw bandwidth before triggering)
  - Very low and not considered technical risk

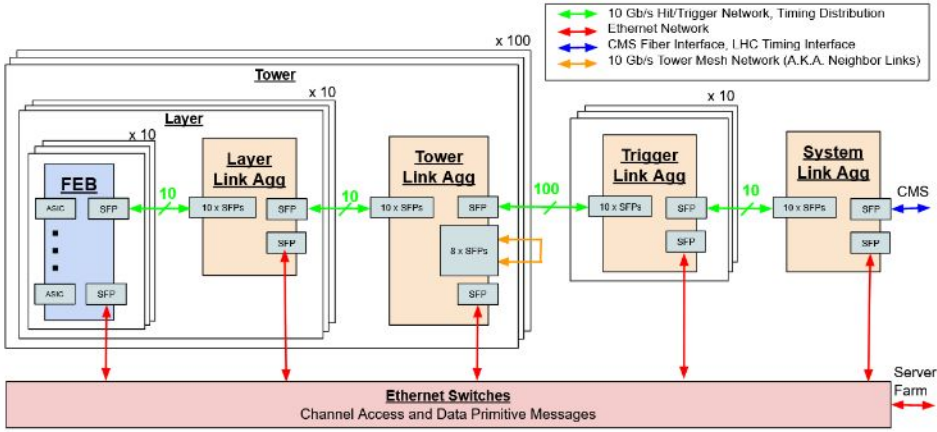


Table 2: Expected SiPM hit rates

	End(kHz)	Bar(Hz)	FEB[kHz)	Layer(kHz)	Tower.Trig(kHz)	Tower.Data(kHz)
SIPM Dark Rate	30.0	36.0	1.4	14.4	86.4	144.0
Cosmic		35.0	1.4	14.0	84.0	140.0
Total		71.0	2.8	28.4	170.4	284.0

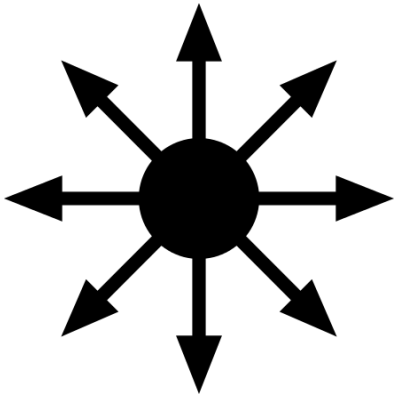
Table 3: Ethernet Streaming Bandwidths for the Data Primitives based on Table 2

	Bar(kb/s)	FEB[Mb/s)	Layer(Mb/s)	Tower(Mb/s)	System(Gb/s)
Data Primitive Streaming	6.8	0.3	2.7	27.3	2.7

SLAC Ultimate RTL Framework (SURF) Firmware

- https://github.com/slaclab/surf
- Open source
- HUGE VHDL library for FPGA development
- Used in Xilinx FPGAs, Intel FPGAs and ASIC digital designs
- VHDL-based IPs for commonly implemented modules
  - Ethernet Library: (1000BASE-KX, 10Gbase-KR, XAUI, IPv4, ARP, DHCP, ICMP, UDP)
  - AXI4 Library: (Crossbar, DMA, FIFO, etc.)
  - AXI4-Lite Library: (Crossbar, AXI4-to-AXI4-Lite bridge, etc.)
  - AXI4 stream Library: (DMA, MUX, FIFO, etc)
  - Device Library: (ADI, Micron, SiliconLabs, TI, etc.)
  - Synchronization Library: (Synchronize bits, buses, vectors, resets, etc)
  - Wrapped Xilinx Library: (clock managers, SEM, DNA, IPROG)
  - Serial Protocols Library: (I2C, SPI, UART, line-code, JESD204B, etc)
  - SLAC Protocols: https://confluence.slac.stanford.edu/display/ppareg/SLAC+Protocols
- SURF is managed and maintained by TID-ID Electronics Systems Department
- New features and bug fixes on a weekly basis

Ruckus: Vivado Build System



- https://github.com/slaclab/ruckus
- Open source
- “Ruckus” is not an acronym
- Compliments the SURF firmware library
- Hybrid Makefile/TCL system
- Integrates the git repo into the Vivado build
  - Provides the git hash at time of build as a readable register
  - Scripts to help with tag releasing and release note generation
- TCL helper function to help with add code into the Vivado project
- Able to reproduce a Vivado project environment without revision controlling the entire Vivado project
  - Example: if Vivado project environment gets “mucked up”:

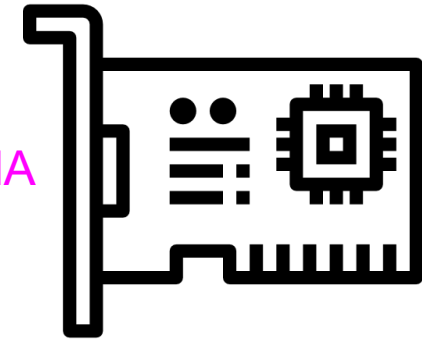
    $ make clean

    $ make gui
- Ruckus is managed and maintained by TID-ID Electronics Systems Department
- Fairly mature and stable. Only requires updating when there is a new Vivado release

Rogue Software

- https://github.com/slaclab/rogue, https://slaclab.github.io/rogue/
- “Rogue” is not an acronym
- Operates either in a python/C++ hybrid or C++ only mode
  - Higher level python for connecting the high performance C++ modules together
- x86-64, ARM32 and ARM64 support
- Able to run on Linux, MAC or windows
  - Windows requires either WSL2, cygwin or Linux virtual machine
- Software tools for both rapid prototyping and experiment deployment
- Lots of ways to run the rogue software
  - 100% C++ only code
  - python script (non-GUI)
  - EPICS
  - Python GUI (e.g. PyQT, PyDM, etc)
- Uses ZeroMQ to connect multiple heterogeneous DAQ software clients to same software server
  - Example:**Simultaneously** running on EPICS while debugging hardware in custom python GUI
- Rogue is managed and maintained by TID-ID Electronics Systems Department

PCIe FW/SW Framework



- https://github.com/slaclab/axi-pcie-core
- Open source
- Firmware framework for BAR0 AXI-Lite interface with up to 8 DMA lanes
  - 256 TDEST per DMA lane (up to 2048 destinations total)
- Provide a “common platform” firmware frame and software kernel driver for any Xilinx PCIe card
  - Common Xilinx Dev board support
    - AC701, KC705, KCU105, KCU116, VCU128
  - Common Xilinx Data Center Card support
    - U50, U200, U250, U280, KCU1500
  - Much more card support can be added as needed
- Demonstrate up to 103 Gb/s for large frames (PCIe GEN3 x 16, 1MB frames)
- Demonstrate > 4MHz frame rate for small frame (<128B) without frame batching
- Managed and maintained by TID-ID Electronics Systems Department

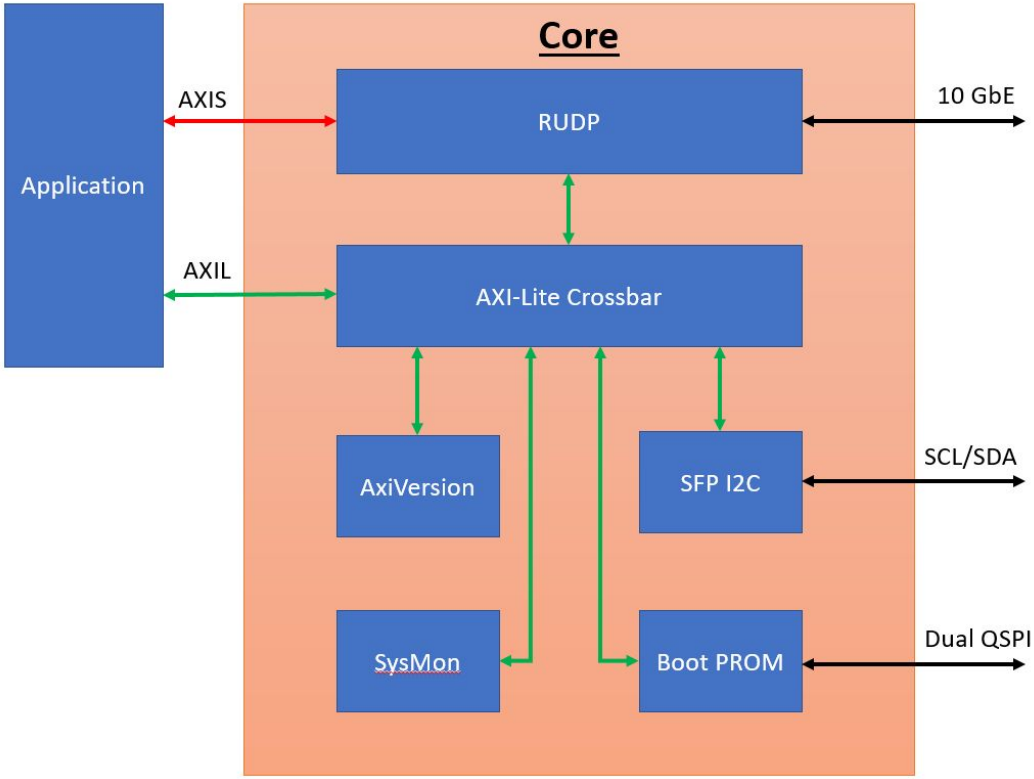
Zynq Ultrascale+ FW/SW Framework

SLAC

- https://github.com/slaclab/axi-soc-ultra-plus-core
- Open source
- Firmware framework for AXI-Lite interface with up to 8 DMA lanes
  - 256 TDEST per DMA lane (up to 2048 destinations total)
- Provide a “common platform” firmware frame and software kernel driver for any Zynq Ultrascale+
  - Common Xilinx Dev board support
    - ZCU102 (non-RFSoC)
    - ZCU111 (RFSoC GEN1)
    - ZCU208 (RFSoC GEN3)
    - SLAC’s 2nd Generation NASA RFSoC Board (RFSoC GEN3)
  - Much more Zynq Ultrascale+ board support can be added as needed
- Fairly new platform development. Inspired by the work done on axi-pcie-core
- Managed and maintained by TID-ID Electronics Systems Department

Development Board Example

- surf/ruckus/rogue compliments each other
- Question: How can I get started?
  - Answer: We provide a working example that someone can copy and modified
- https://github.com/slaclab/Simple-10GbE-RUDP-KCU105-Example
- https://slaclab.github.io/Simple-10GbE-RUDP-KCU105-Example/



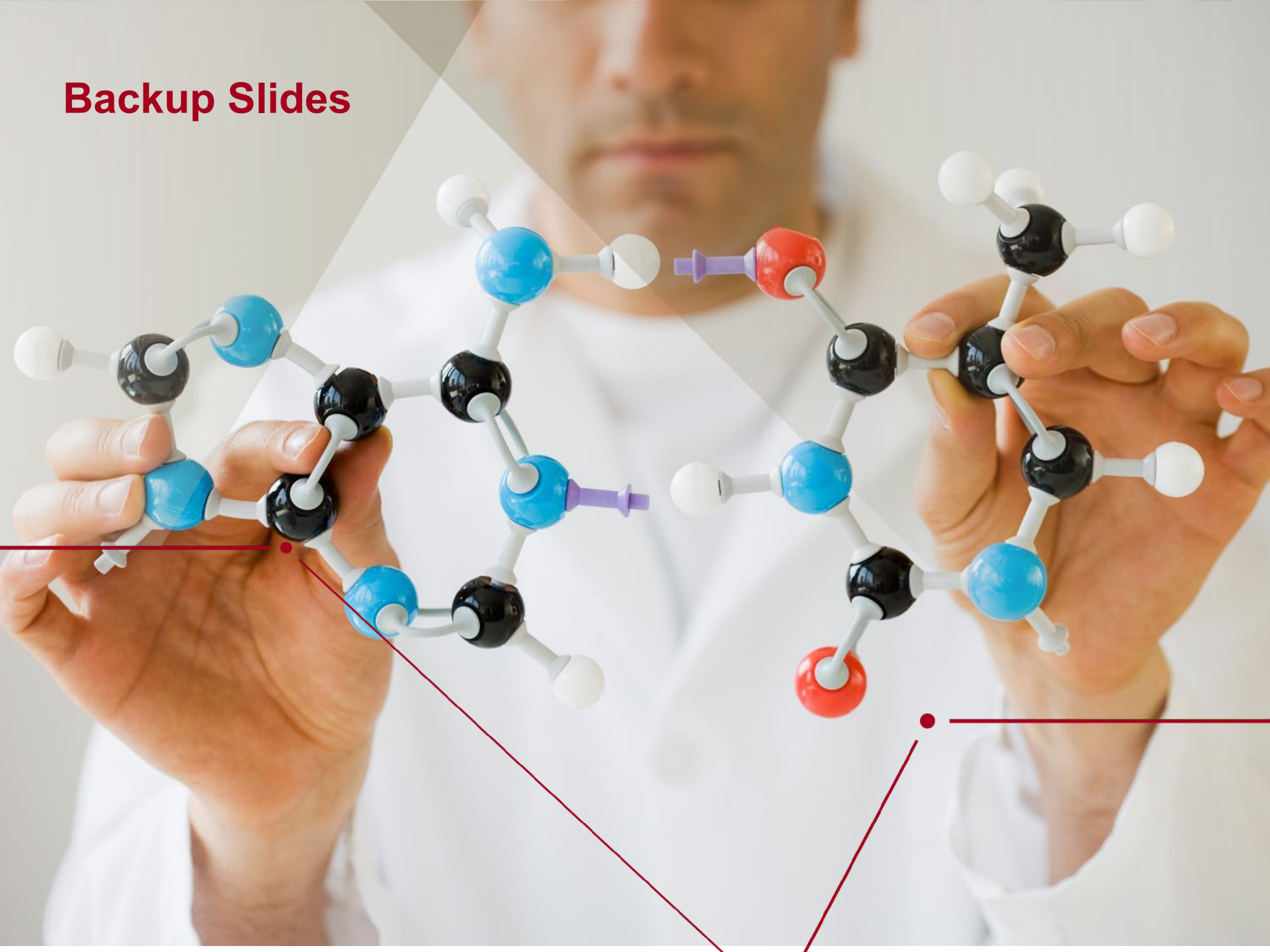
Open Job Positions

- Currently 4 open positions in TID-ID-ES department
  - Analog Engineer, level 2 (Job# 4416)
  - Analog Engineer, level 3 (Job# 4419)
  - Digital Engineer level 2 (Job# 4417)
  - Digital Engineer level 3 (Job# 4418)

Summer Internship

- https://careers.slac.stanford.edu/jobs-slac/educational-and-outreach-programs
- SLAC offers a variety of internship opportunities along with mentorship opportunities created to help you be successful in your career interests
- We host a few interns in our department every year (even during COVID)

Backup Slides

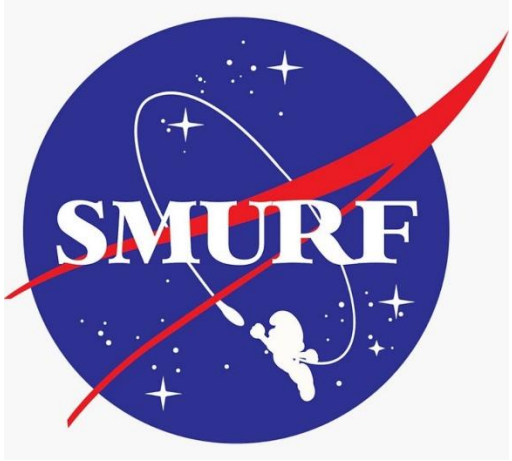


Quantum Systems

Signals Intelligence

Defense

X-ray Science

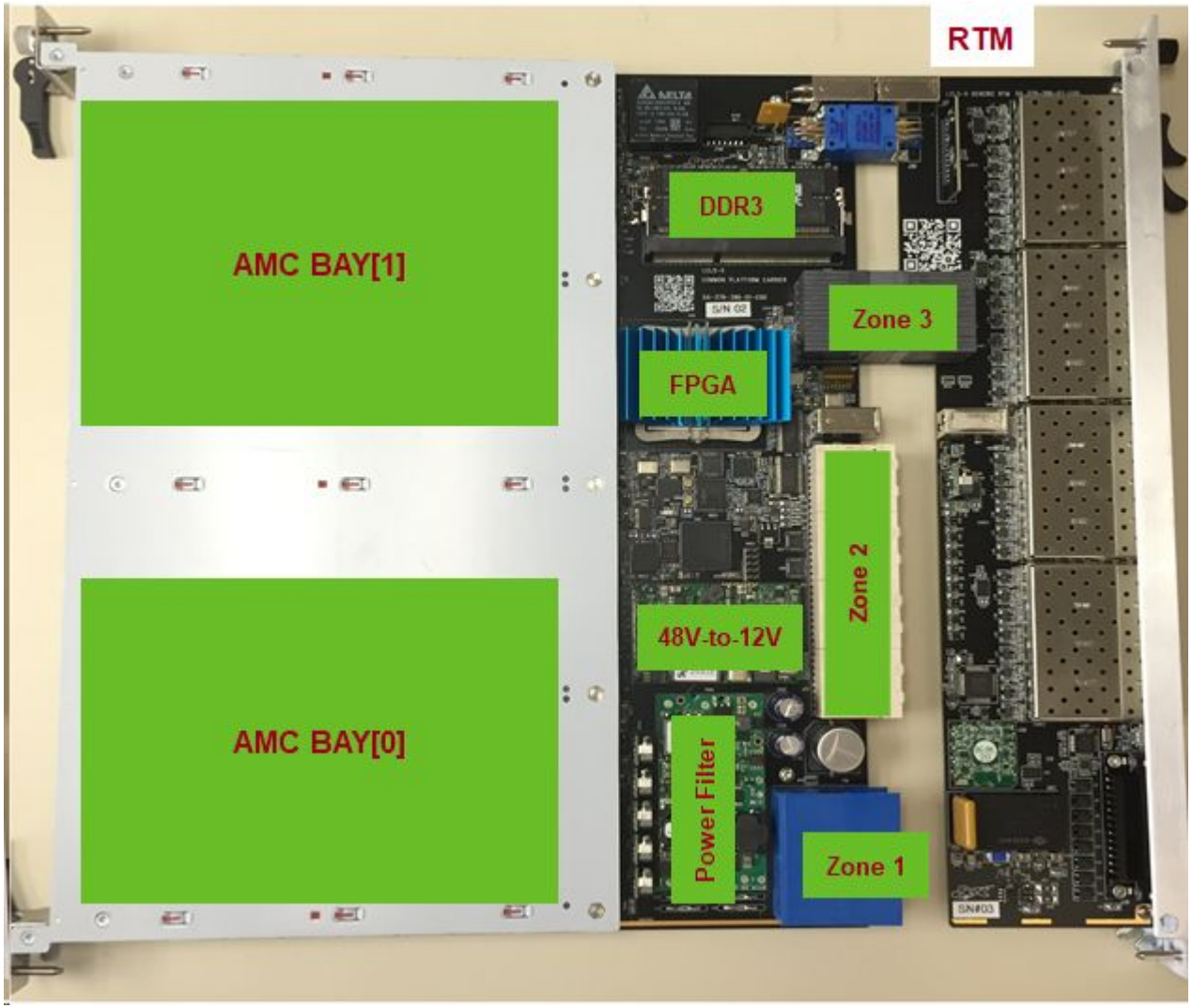


Space

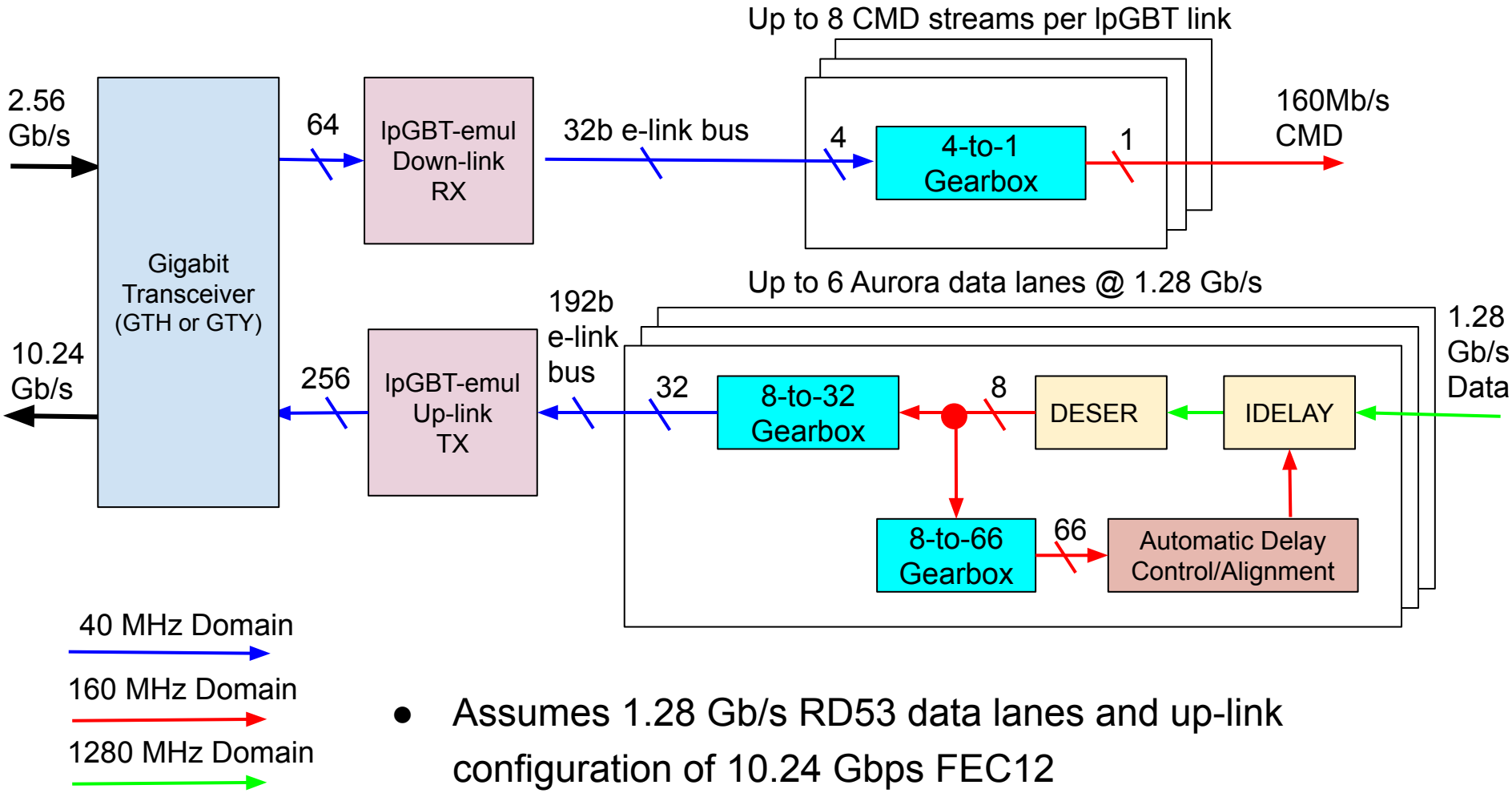
Cosmology

LCLS High Performance System: ATCA Common Platform Design

SLAC

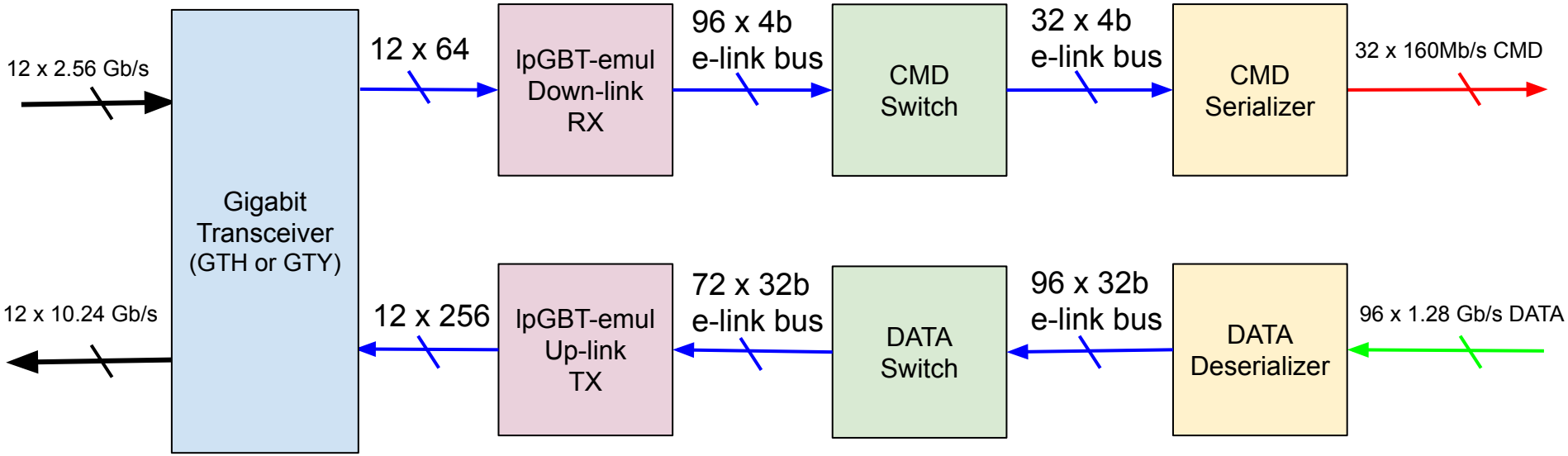


Single Lane lpGBT-emulator: Firmware Block Diagram



- Assumes 1.28 Gb/s RD53 data lanes and up-link configuration of 10.24 Gbps FEC12

Link Agg. + lpGBT-emulator: 12 Lanes Firmware Block Diagram



40 MHz Domain

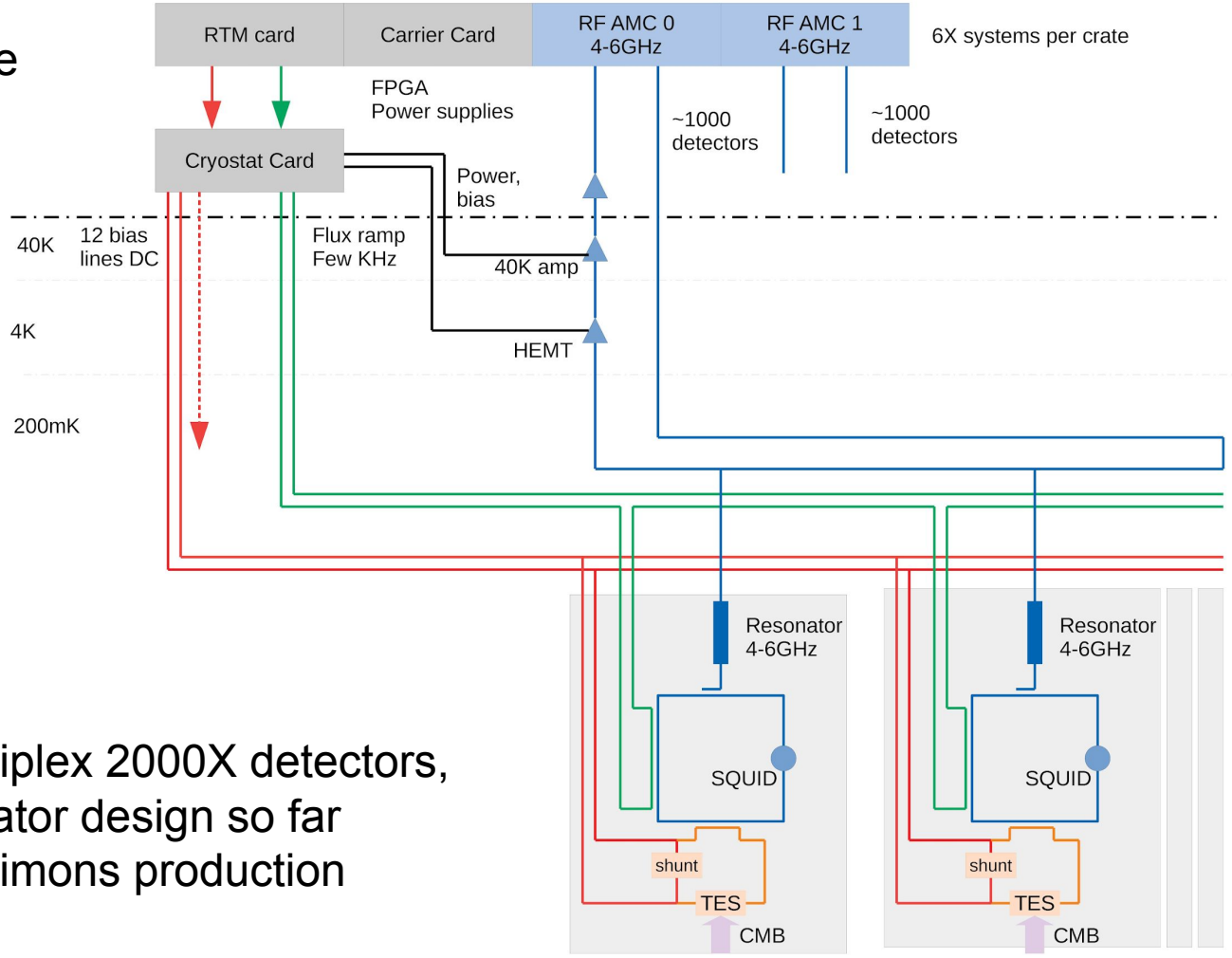
160 MHz Domain

1280 MHz Domain

- **Any** downlink eLINK can be mapped to any CMD port
- **Any** uplink eLINK can be mapped to any DATA port
- CMD/DATA switch configurable via the SGMII's slow control interface

Microwave Multiplexing in More Detail

6X systems per crate

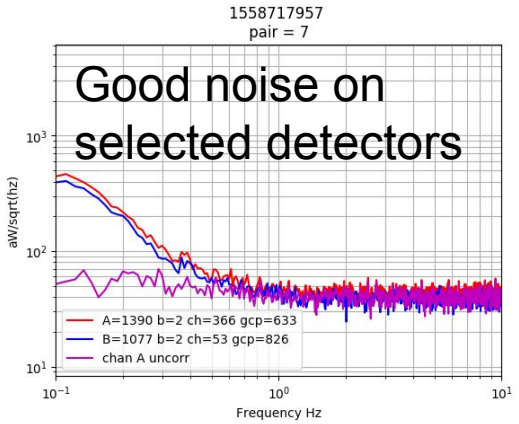


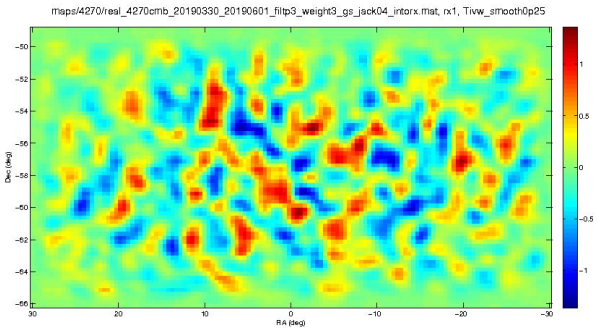
- Broadband RF
- Precision Analog
- Signal processing

Electronics can multiplex 2000X detectors, but cryogenic resonator design so far limits to 1000X for Simons production system.

Smurf Status

Test system installed at BICEP telescope at south pole





CMB map measured with SMuRF (but had some technical issues)

- **Simons Observatory CMB telescope**
- Completed final design review, meeting all requirements
- In production ~40X cards

- **BICEP-Array CMB telescope**
- Will use ~20X SMuRF cards
- South pole deployment 2022?

Mesh Network for 3 Tower x 3 Tower Track Decision

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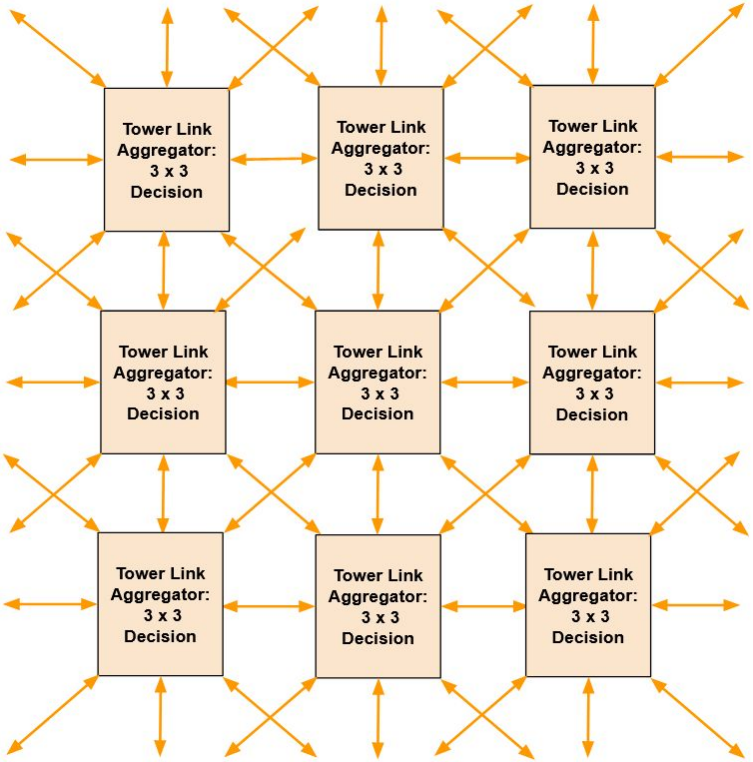
Mesh Network (Zoomed In)



10 Tower x Tower Mesh Network