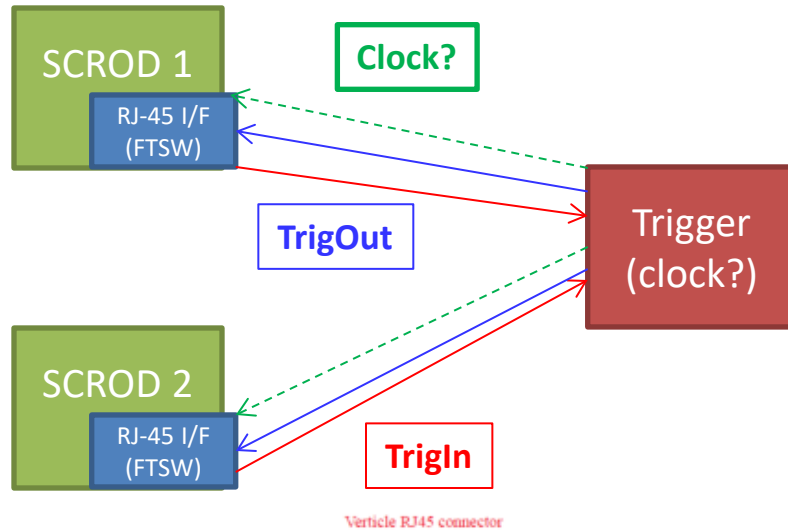
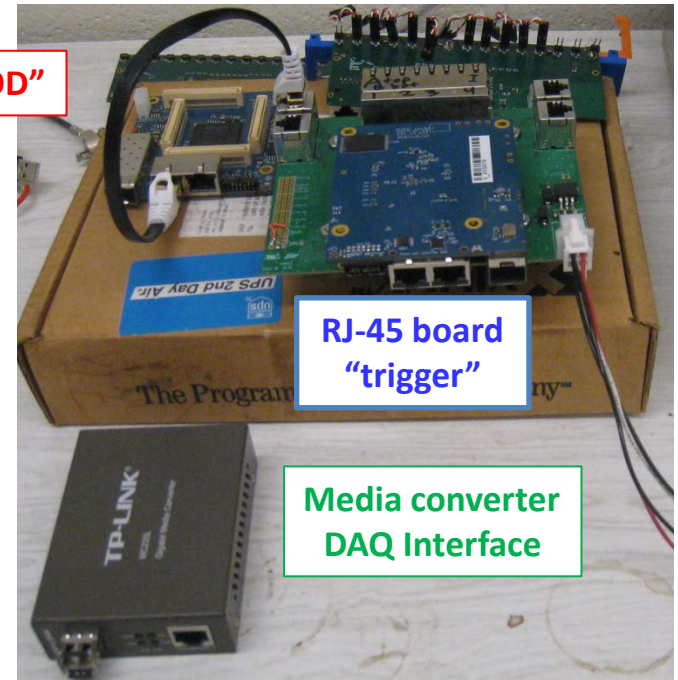


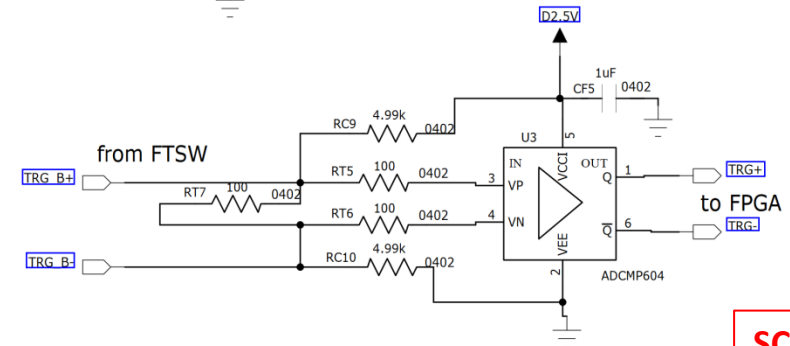
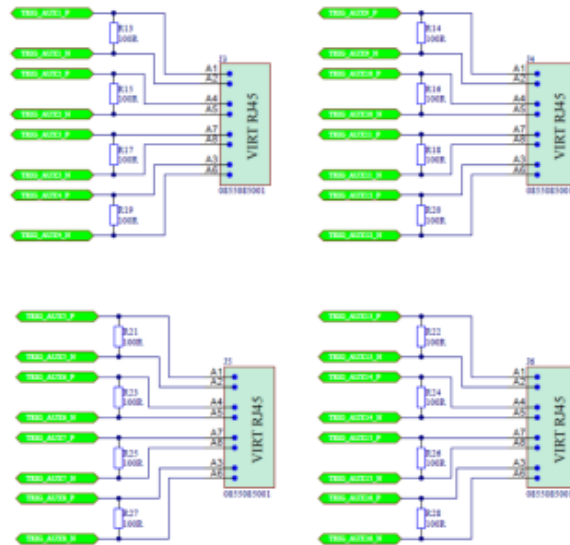
HMB 3.1000 v2 trigger – test bench



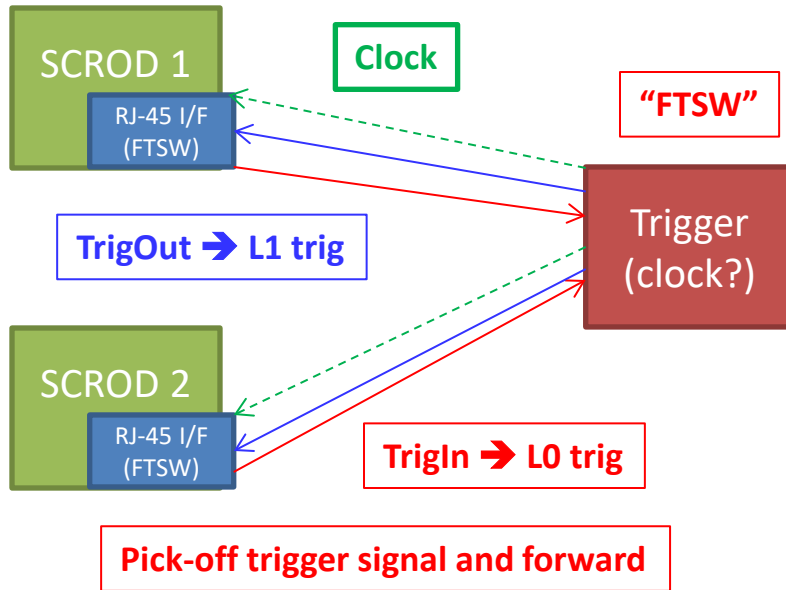
"KLM SCROD"



Notes:
-If internal FPGA diff termination is not available install 100ohm resistors



HMB 3.1000 v2 trigger – test bench



- Use “byte-link” protocol
- Clock (21MHz), 210Mbps (DDR)
- Trigger latency ~ 100ns

