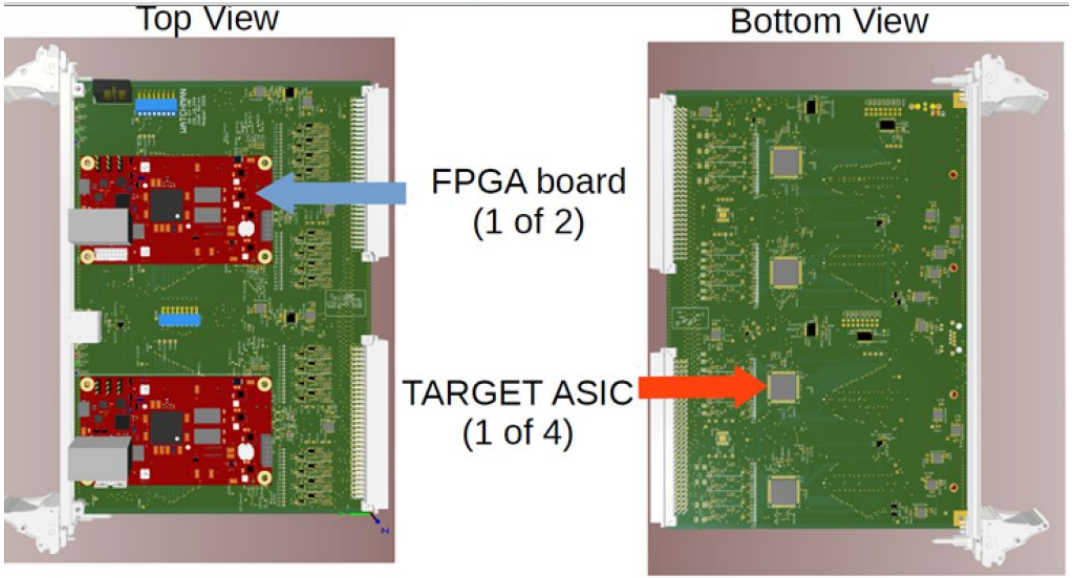
TARGETC readout boards

Salvador Ventura
Jose Duron, Gary Varner, Kurtis Nishimura

HMB kick-off meeting
08-21-2020

16U VME Card

- 4 TARGETCs
- 16 PMT inputs.
- Gain stages for each PMT input: :x10, x1, x1/10 and x1/100.
- 2 trigger mechanisms to improve sensitivity and minimize false triggers.
- 2 Microzed Boards, Zynq Z020

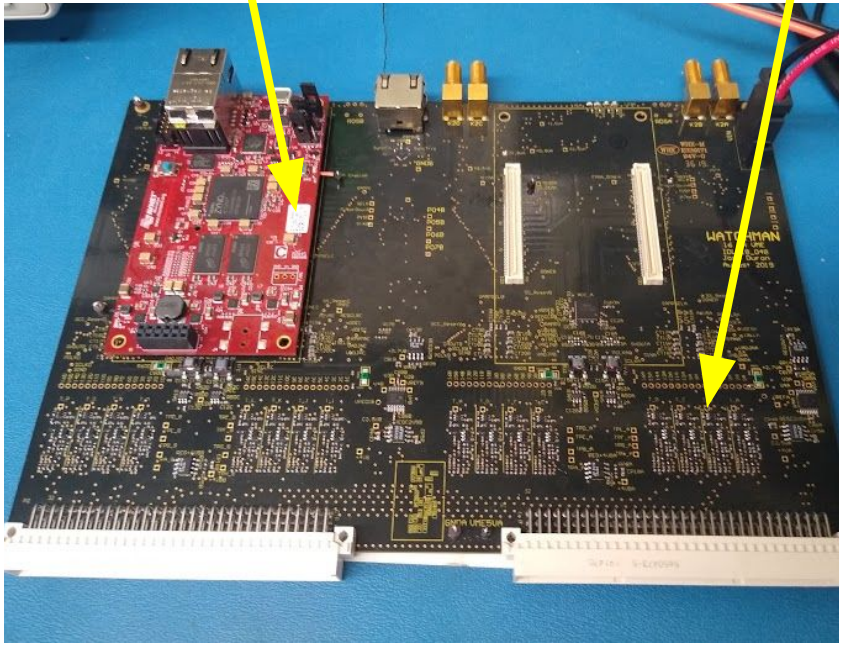


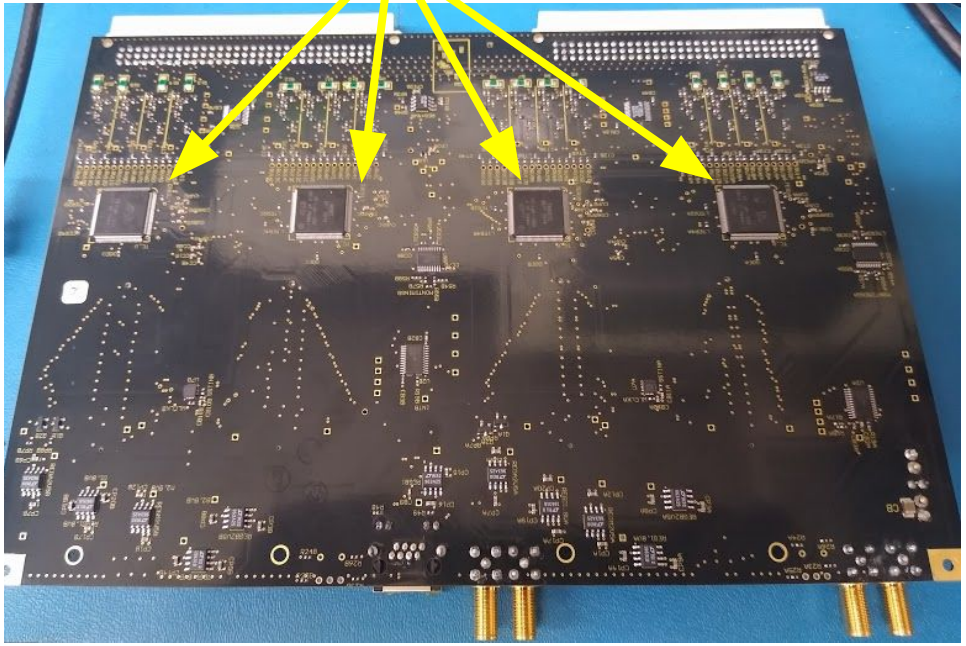
TARGETC Readout for WATCHMAN

Microzed board

Gain stages

TARGETCs





TARGETC Readout for WATCHMAN

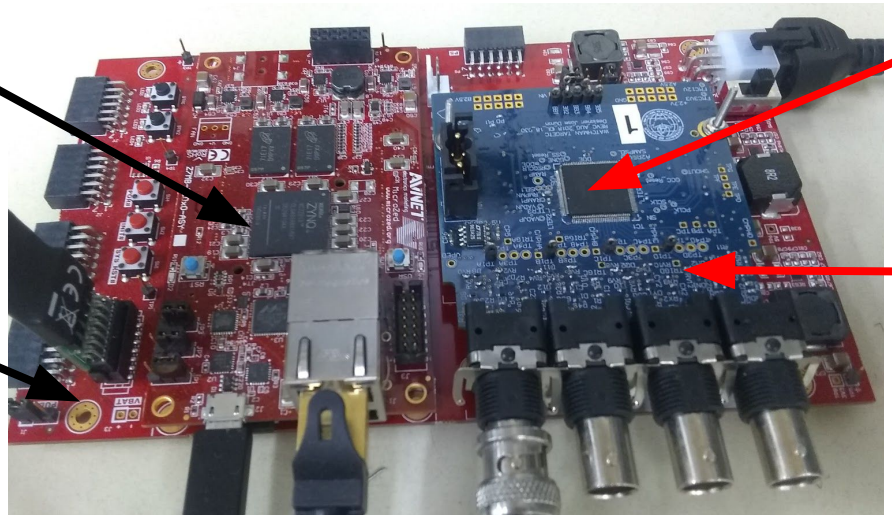
FMC Board

- **TARGETC. A 1GSa/s, 12-bit, 16-channel** Wilkinson ADC, which was designed and fabricated by Gary Varner's ASIC group at UH-Manoa.

-A **ZYNQ SoC** by Xilinx with an FPGA and a dual-core ARM processor.

MicroZed Board
Zynq-7000 SOC
FPGA+ ARM Proc.

FMC carrier board

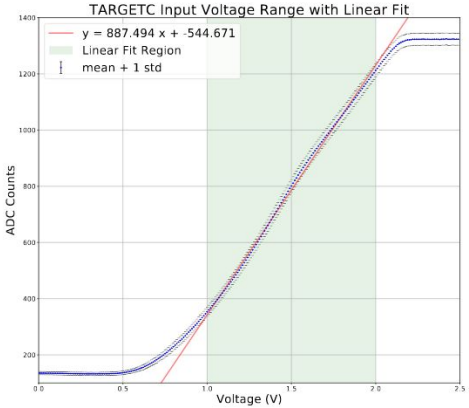


x1, x10,x0.1 and x0.01 gain stages

Done:

Firmware including:

- Interface with TARGETC
- Auto trigger algorithm: sel storage array address to write and windows to digitize from trigger signal.
- Data transfer

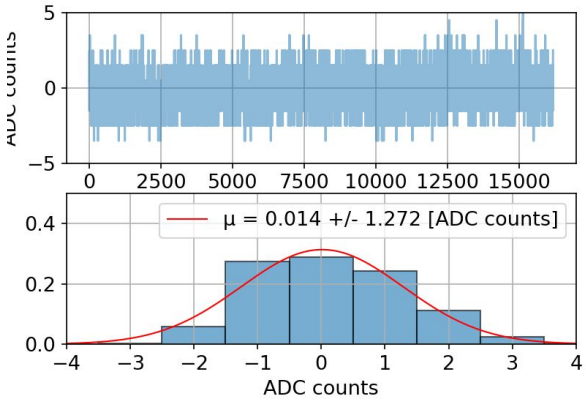


Dynamic range

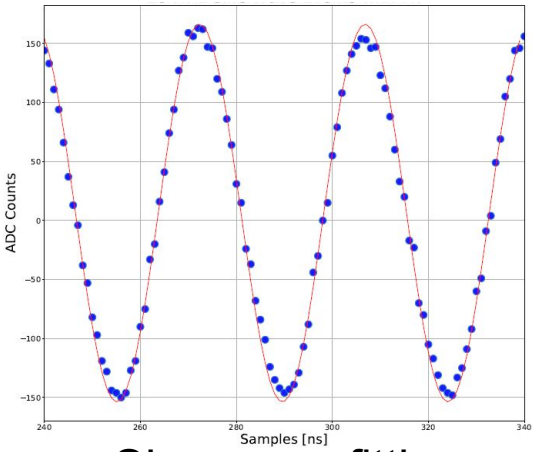
4 PMT-channel FMC board characterization

Current status:

- Migration from FMC board to VME board

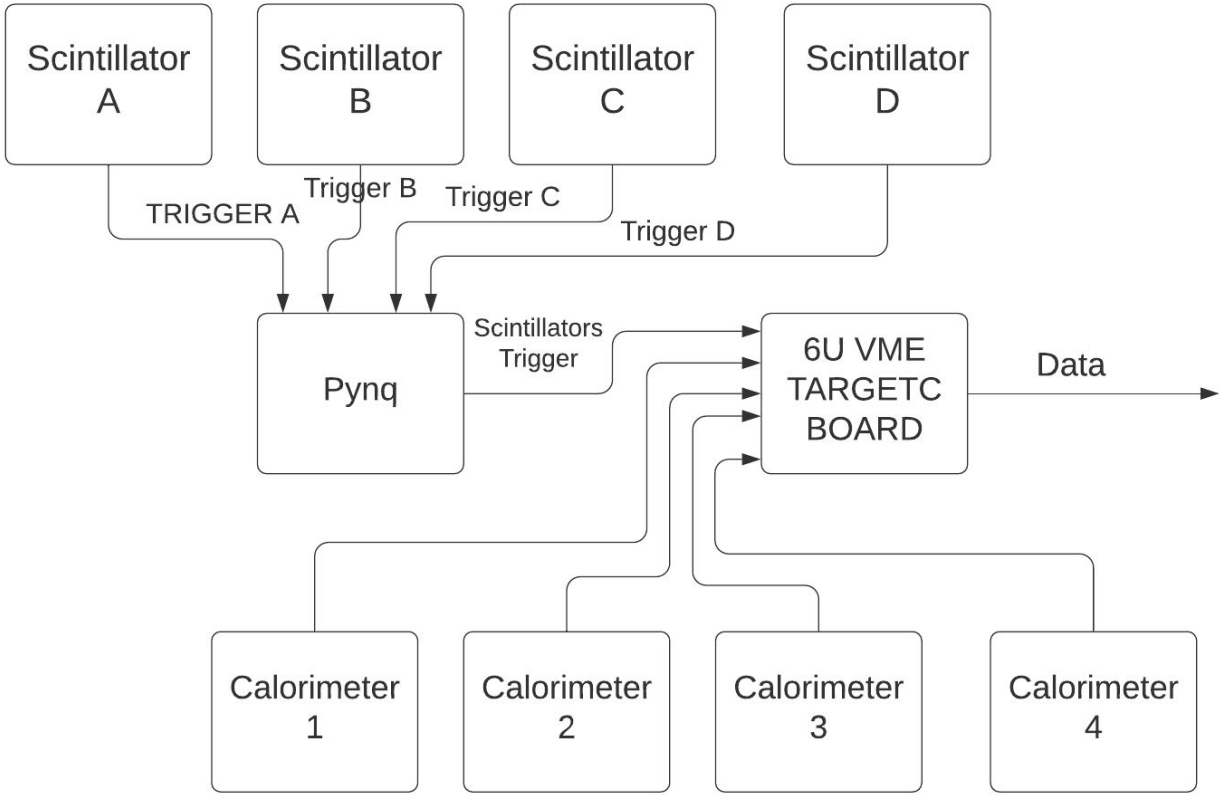


Noise

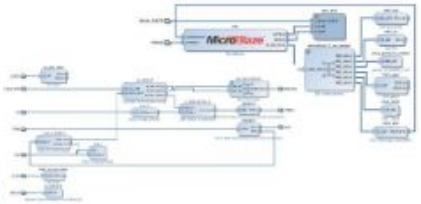


Sine wave fitting

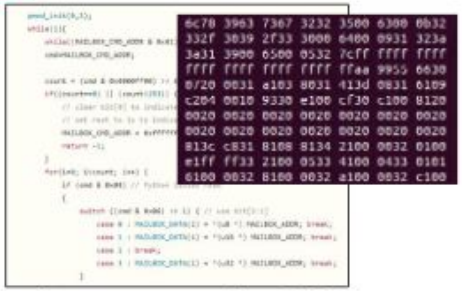
Hawaii Muon Beamline



FPGA overlays – hardware libraries



Step 1:
Create an FPGA design for a class of related applications



Step 2:
Export the bitstream and a C API for programming the design

Step 3:
Wrap the C API to create a Python library

Step 4:
Import the bitstream and the library in your Python scripts and program

XILINX.

https://github.com/Xilinx/PYNQ_Workshop