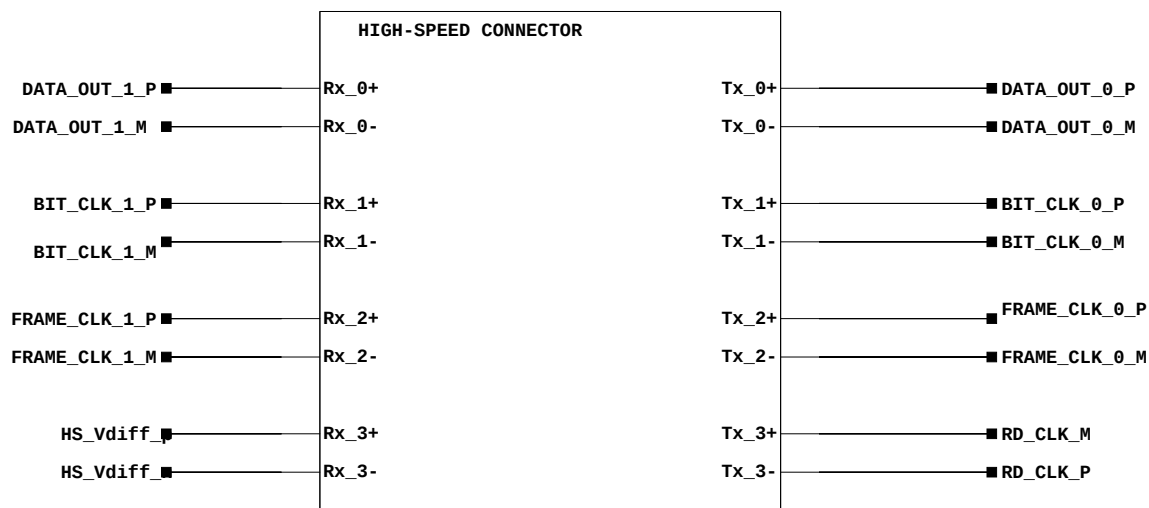
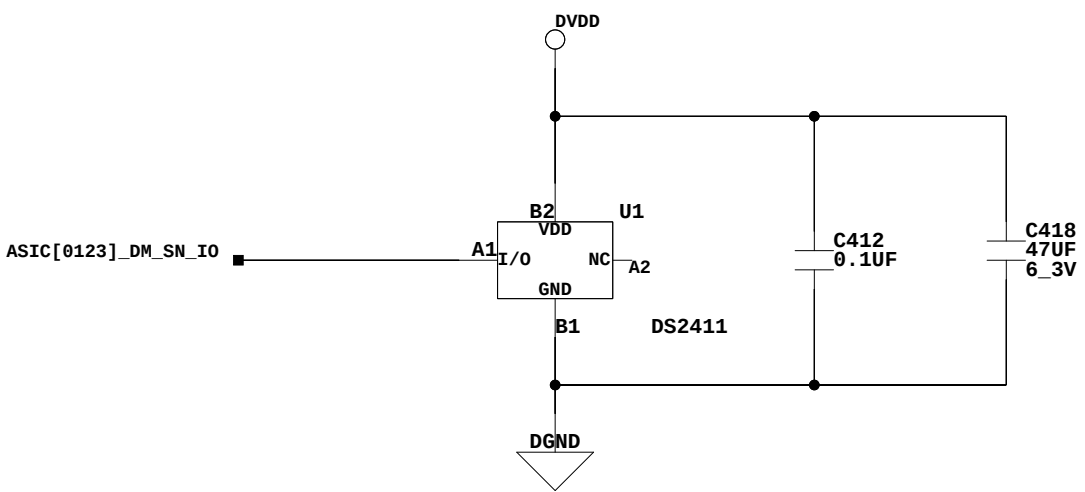


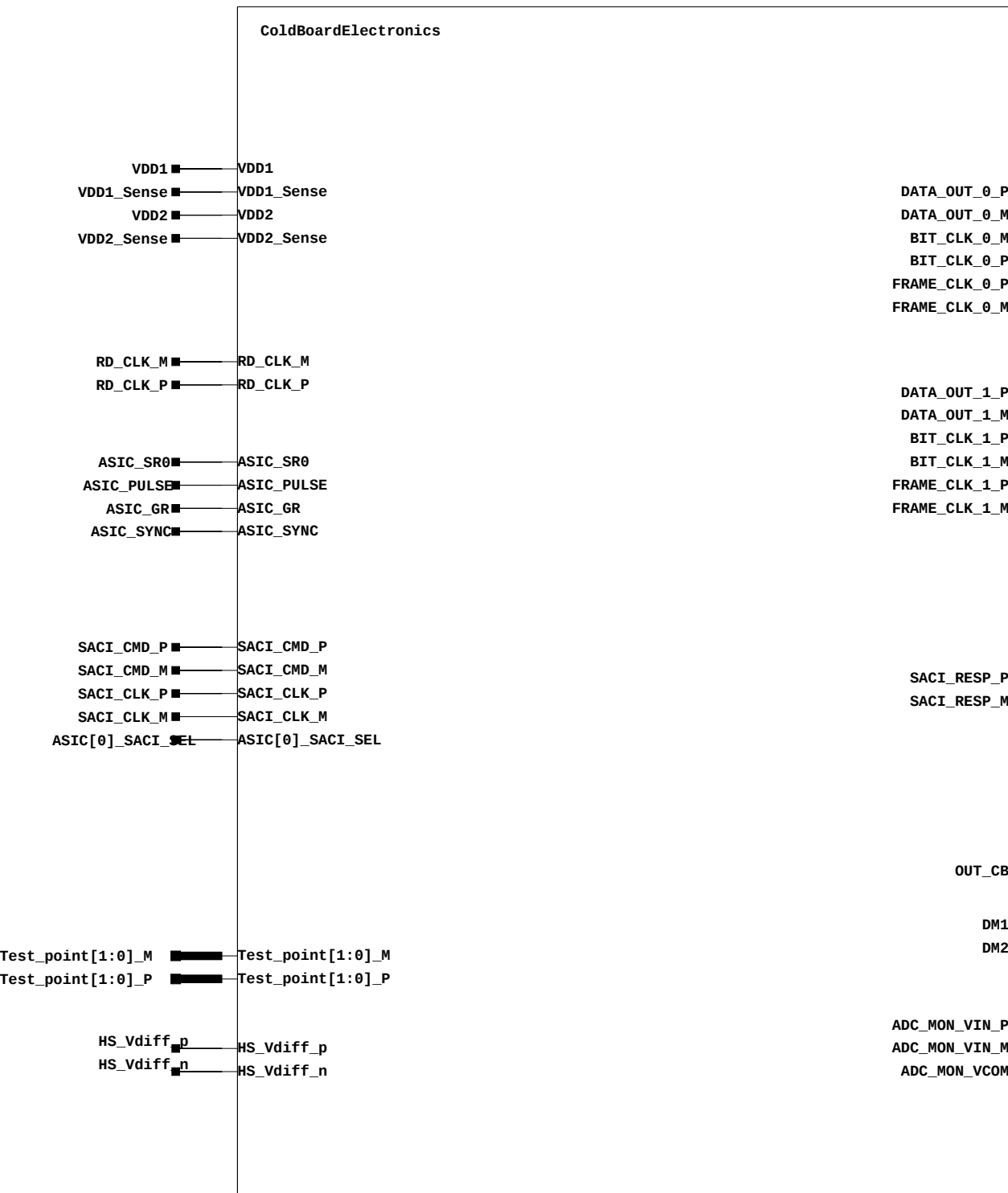
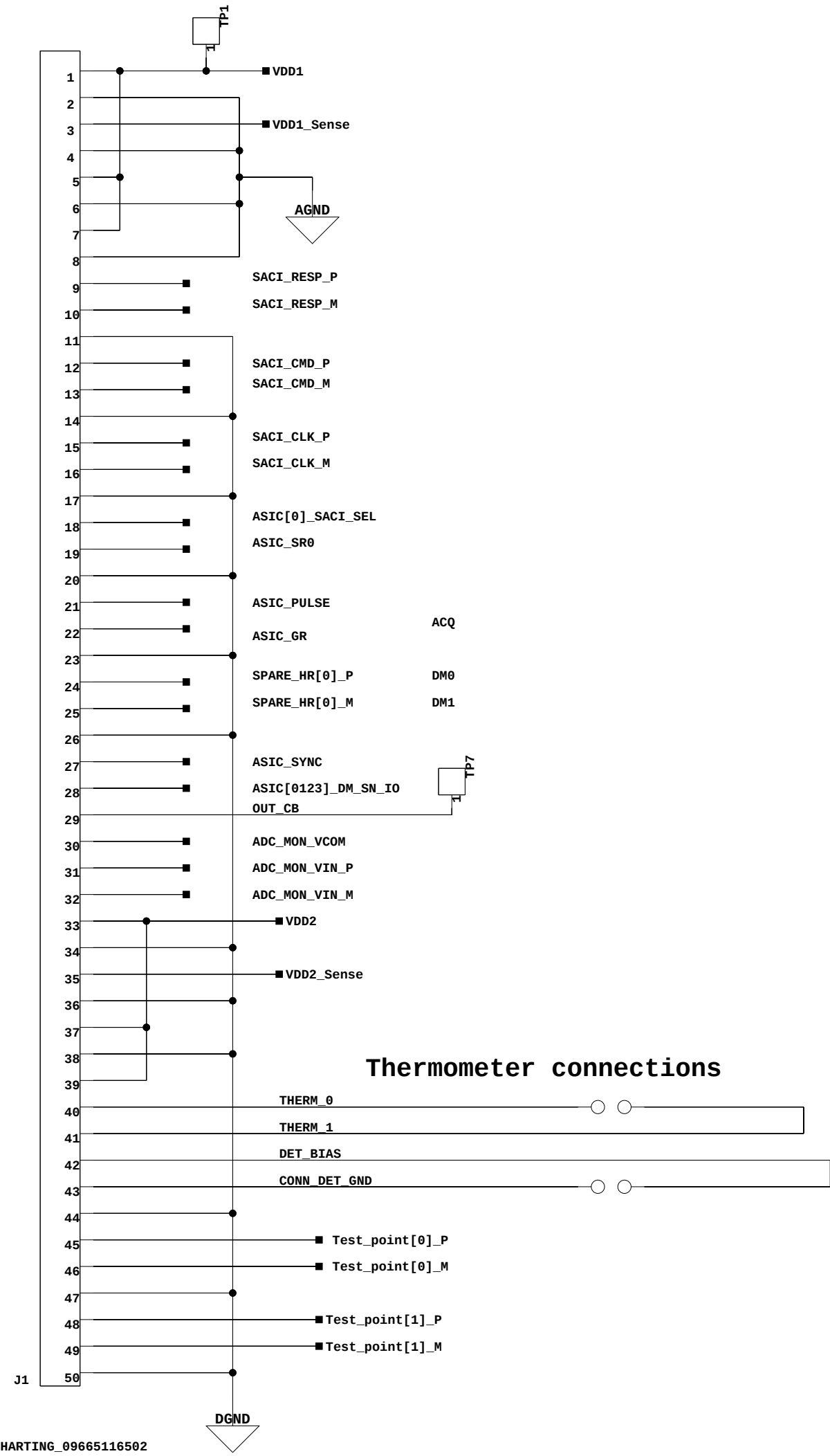
High speed interface



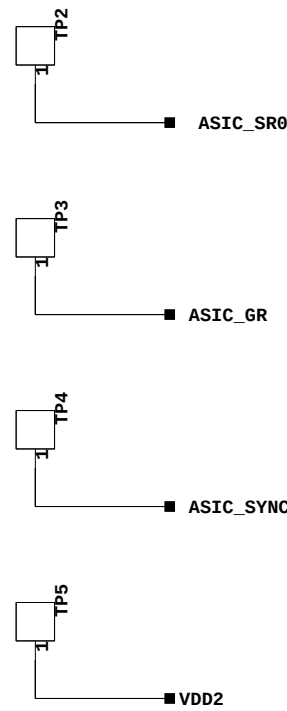
SHEET=2



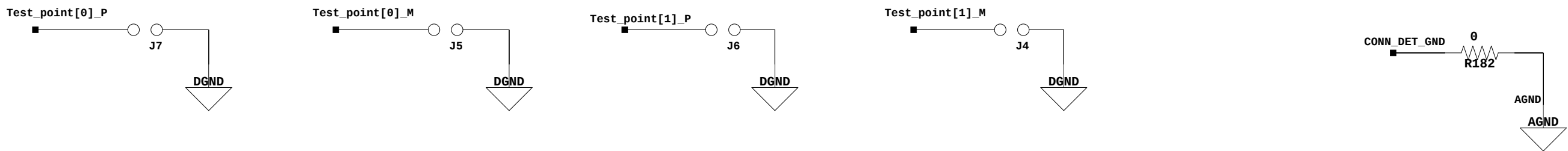
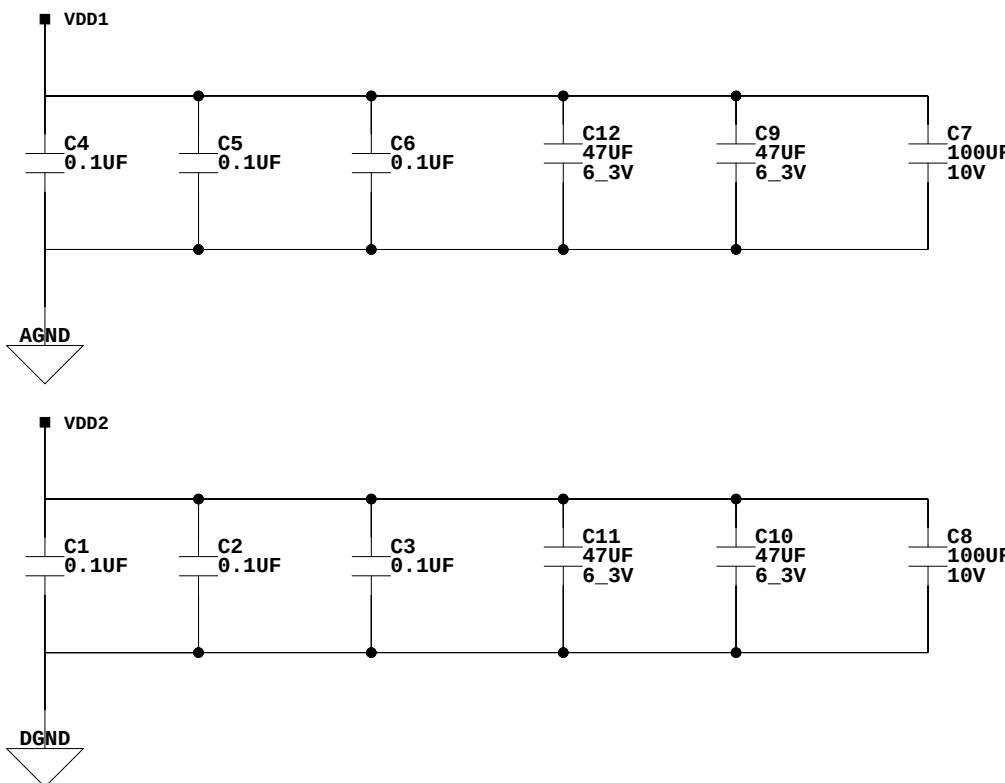
Slow signals and power connector



SHEET=3

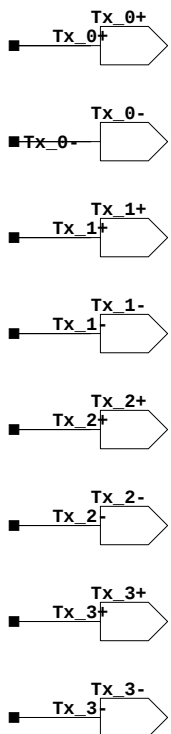
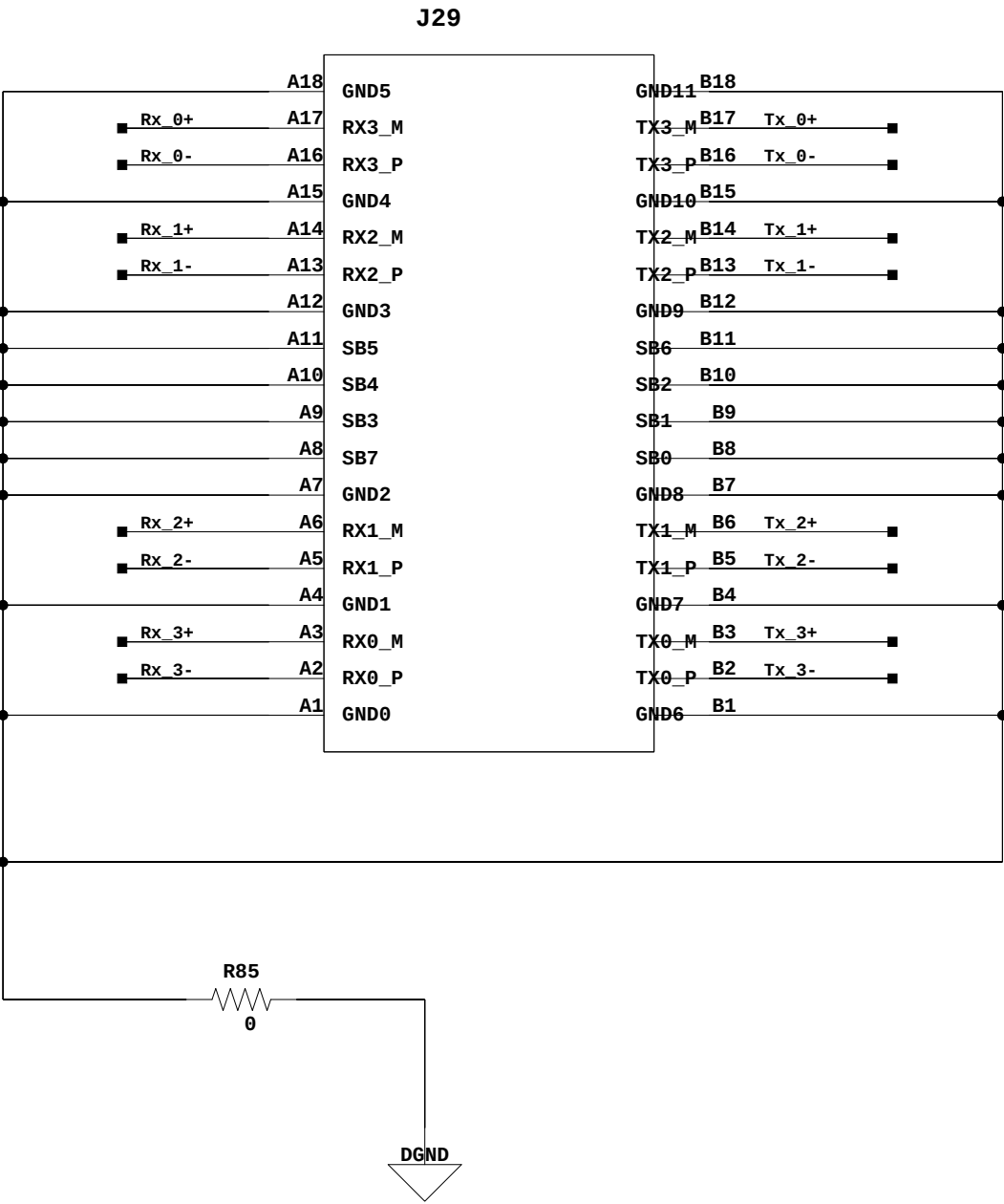
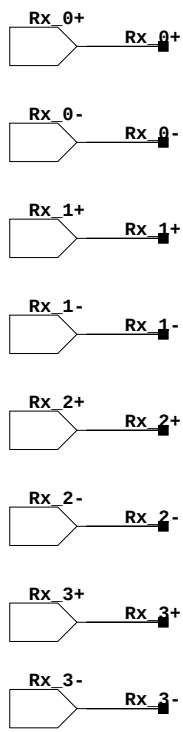


Power Supply decoupling caps

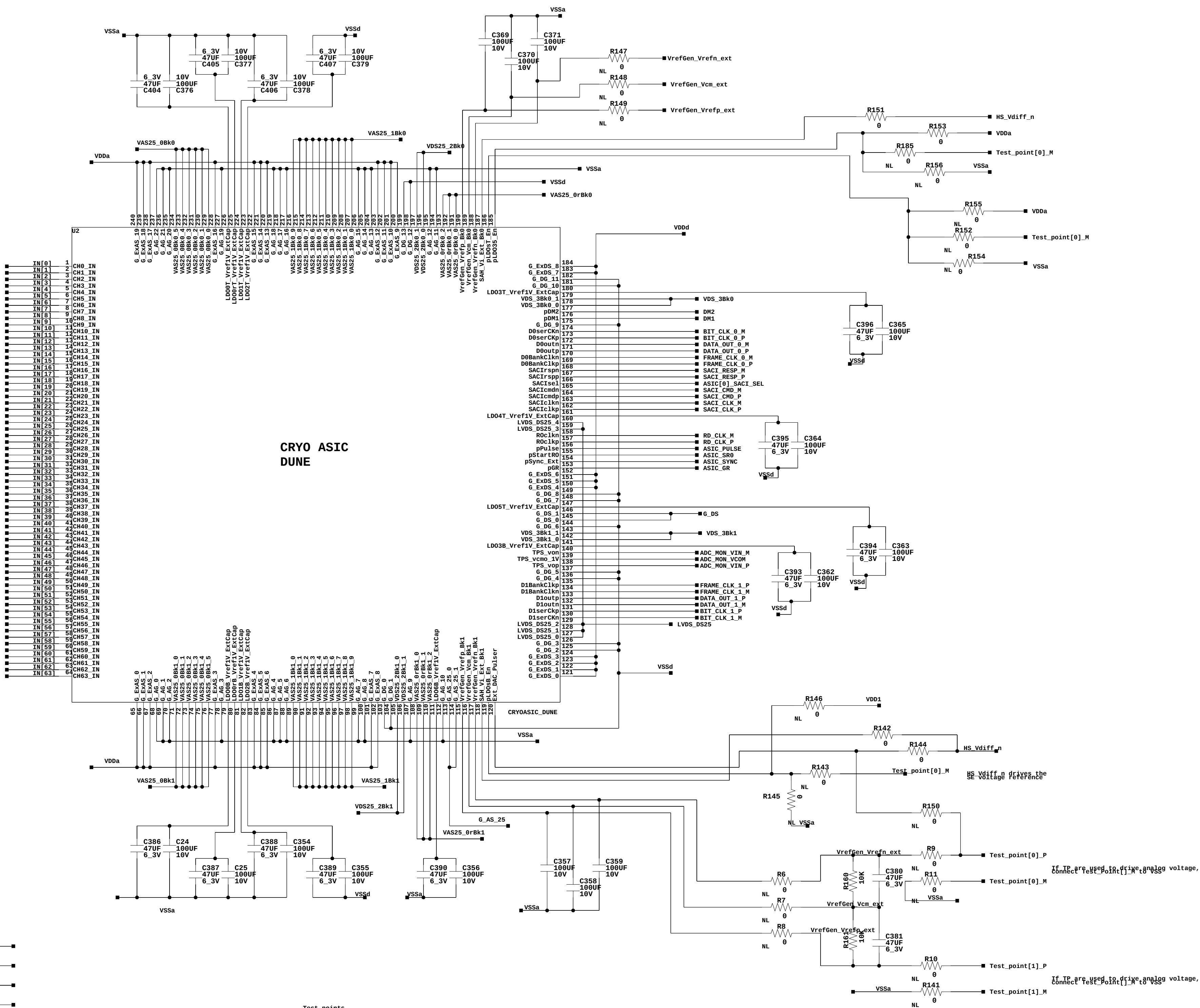
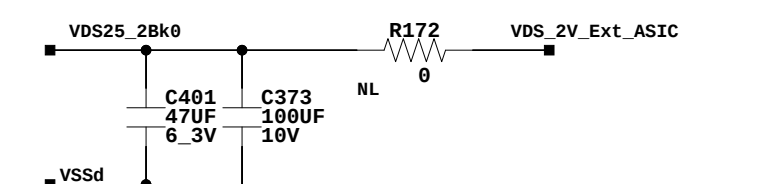
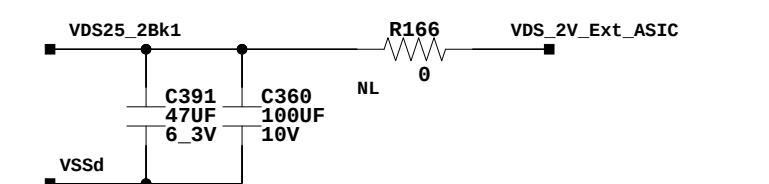
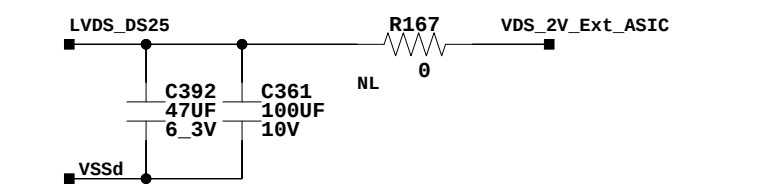
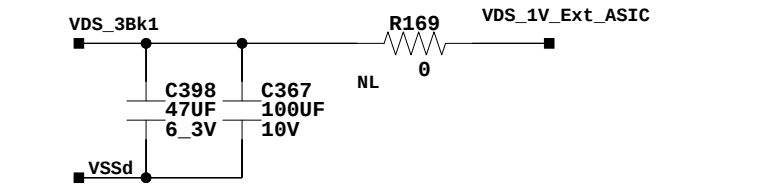
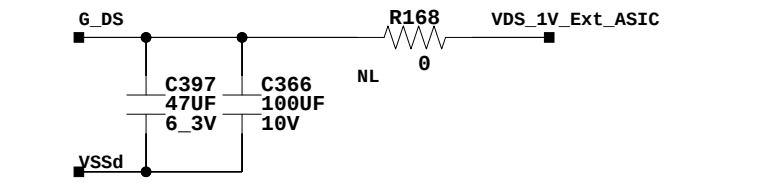
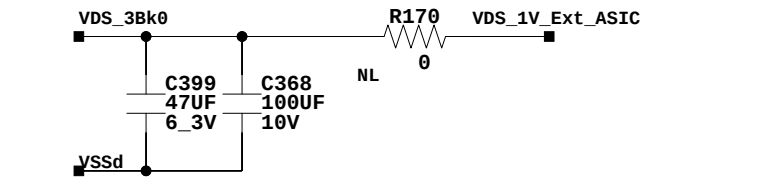
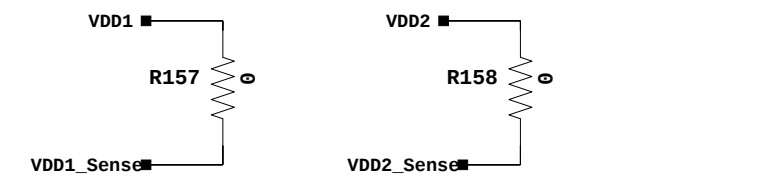
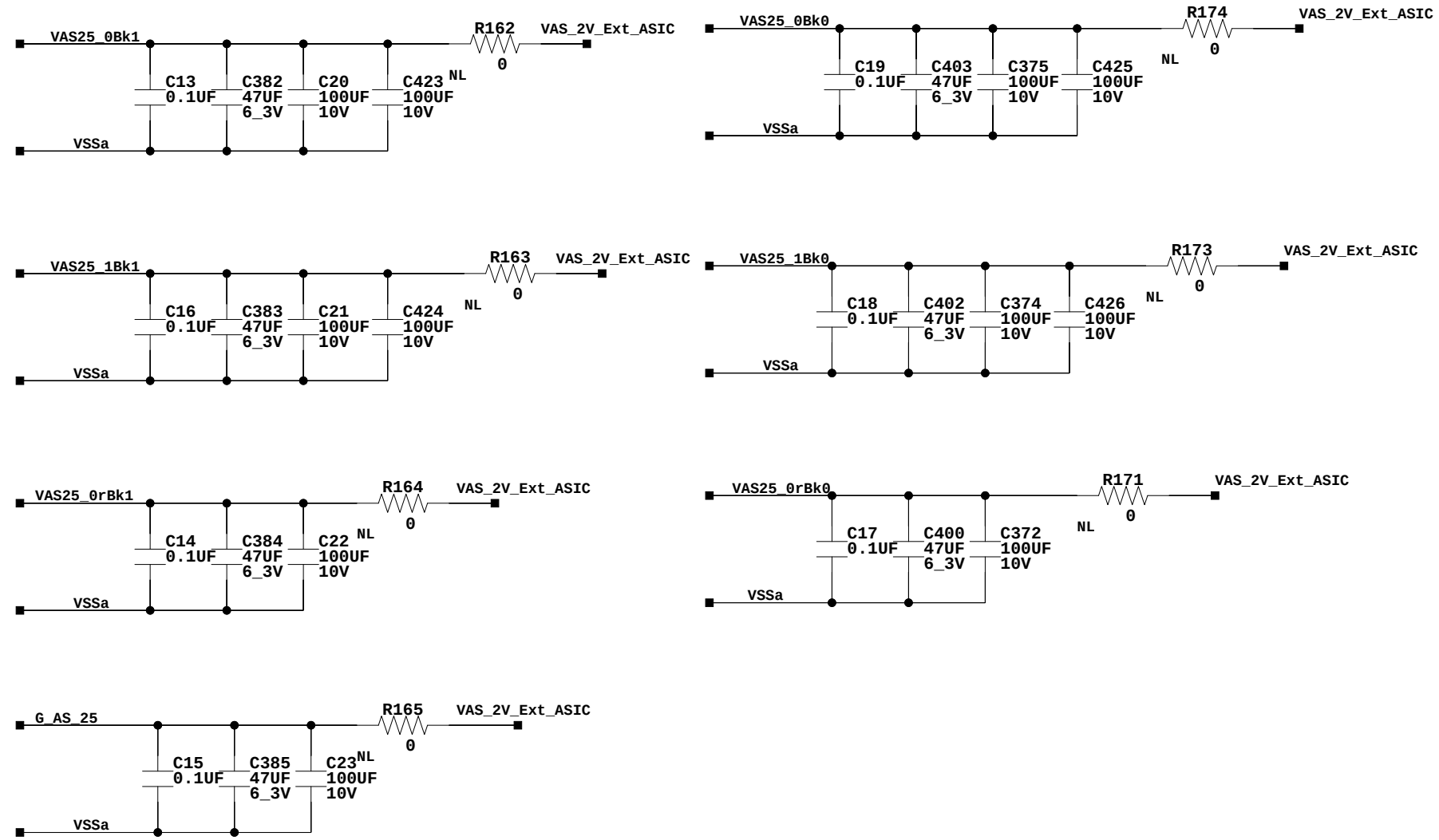
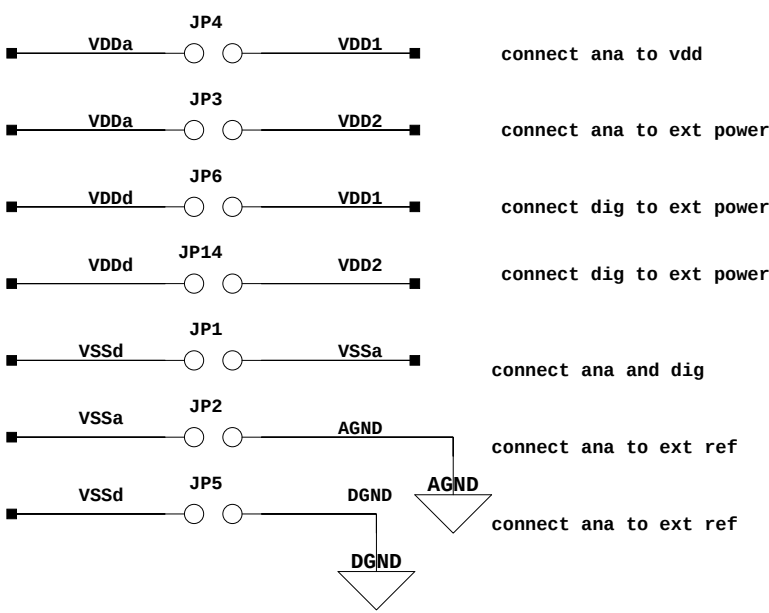
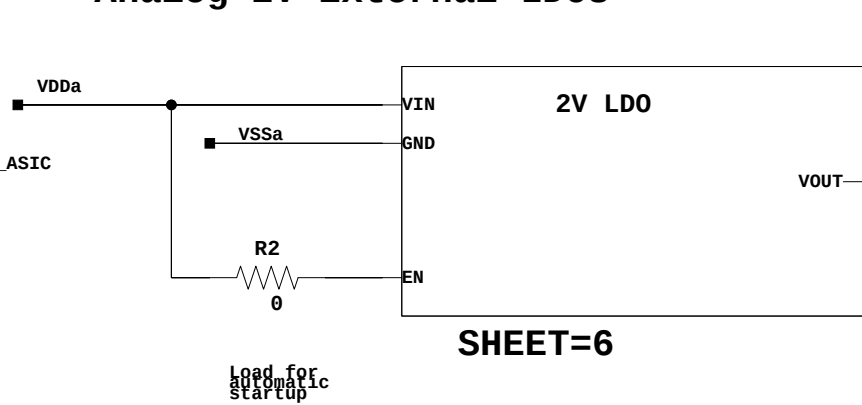


14/01/2019:15:58

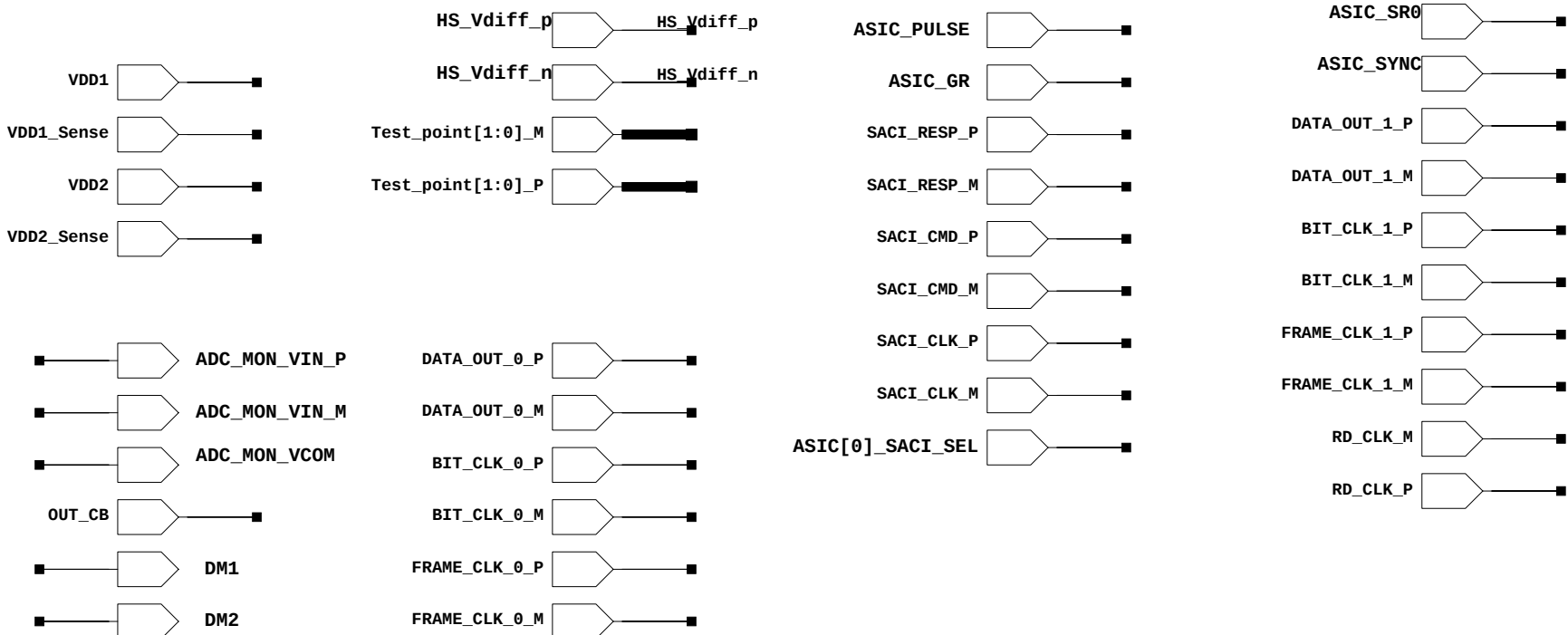
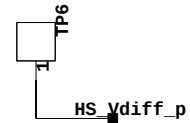
High-speed connector



REV	DESCRIPTION	DFTR	CHKR	ENGR APPV	DATE
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Test points



STANFORD LINEAR ACCELERATOR CENTER U. S. DEPARTMENT OF ENERGY		
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ENGR	Dionisio Doering	DATE
DFTR		2018
CMR		APPROVALS

SHEET 3 OF 19

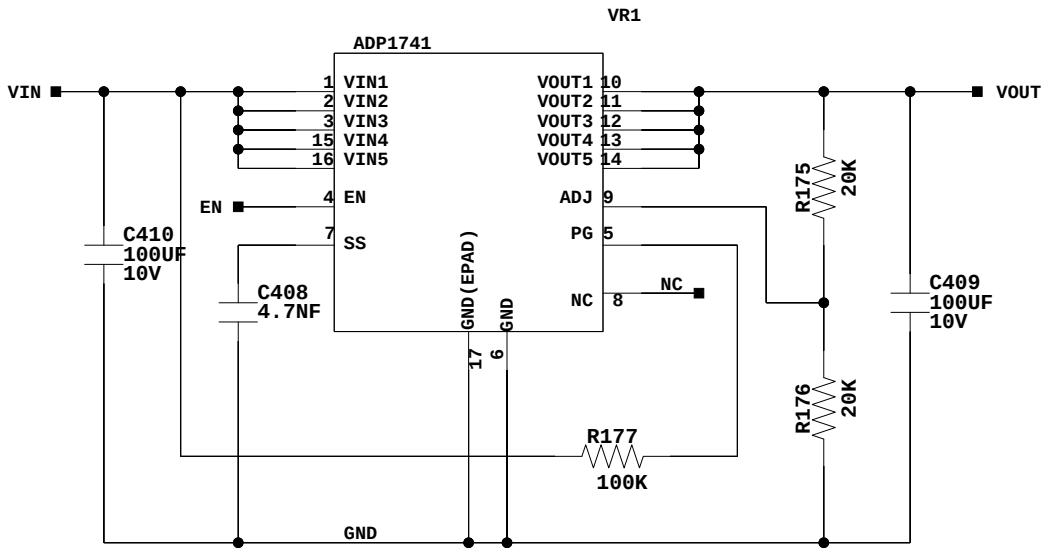
DUNE Cold Board

LOCATED AT SHEET 1

SD-264-810-06-C00

D

DIGITAL 1.0V



Input to external LDO

VIN

positive

GND

negative

EN

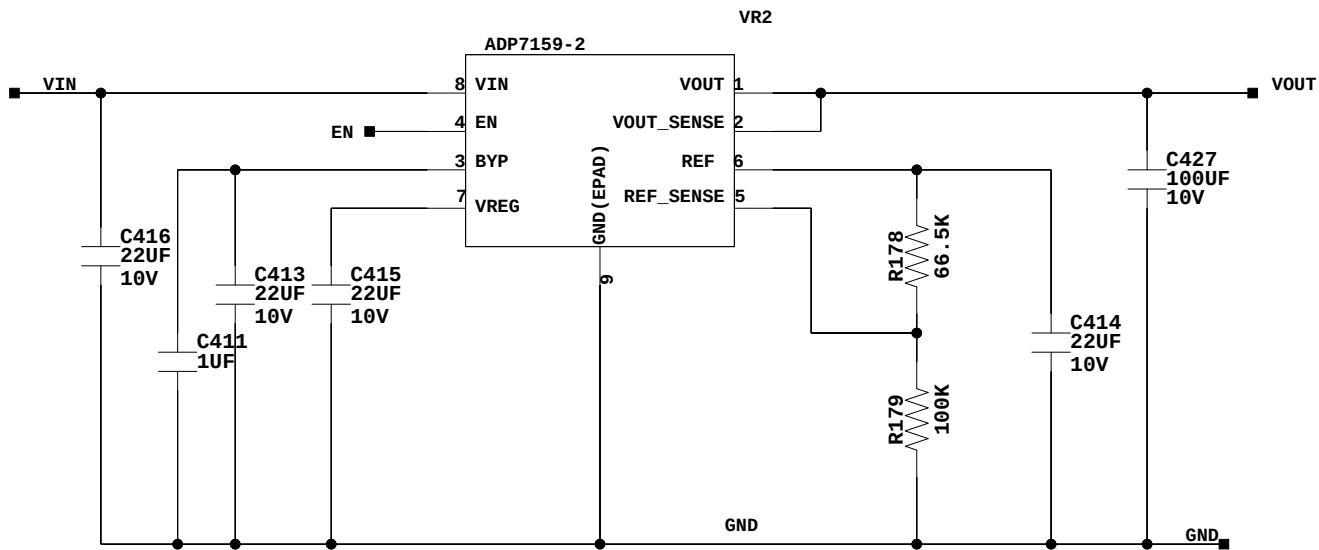
Enable dig LDO by tying to VDD

Output voltages from external LDO

VOUT

10/01/2019:10:12

2.0V OUTPUT



Input to external LDO

VIN

GND

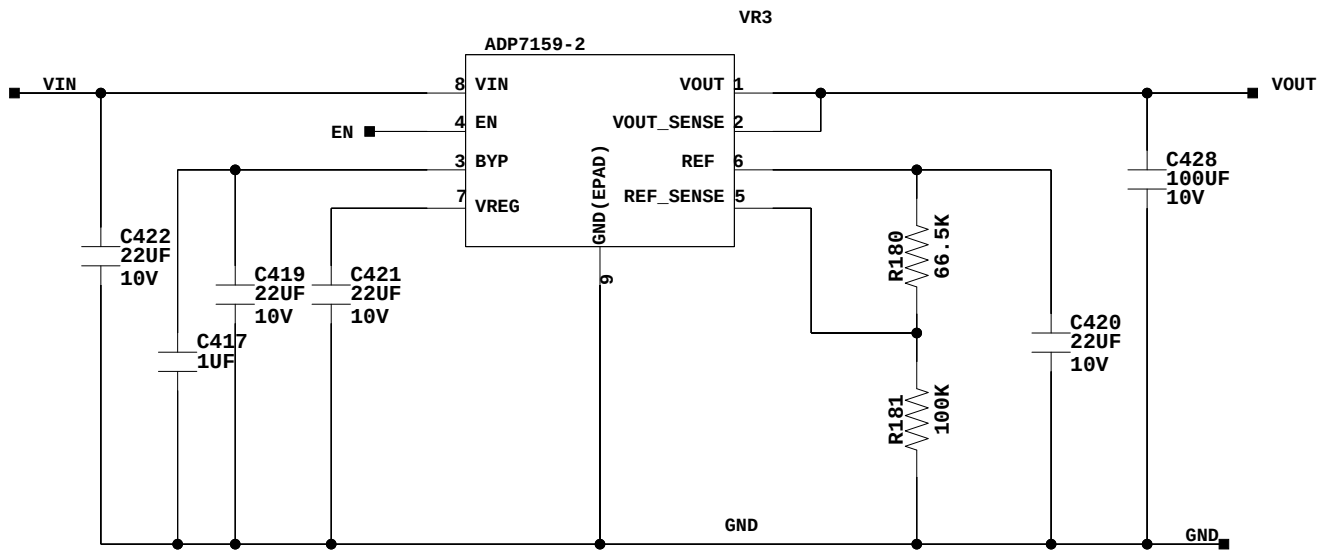
EN

Enable by tying to VIN
in LDO by

Output voltages from external LDO

VOUT

2.0V OUTPUT



Input to external LDO

VIN

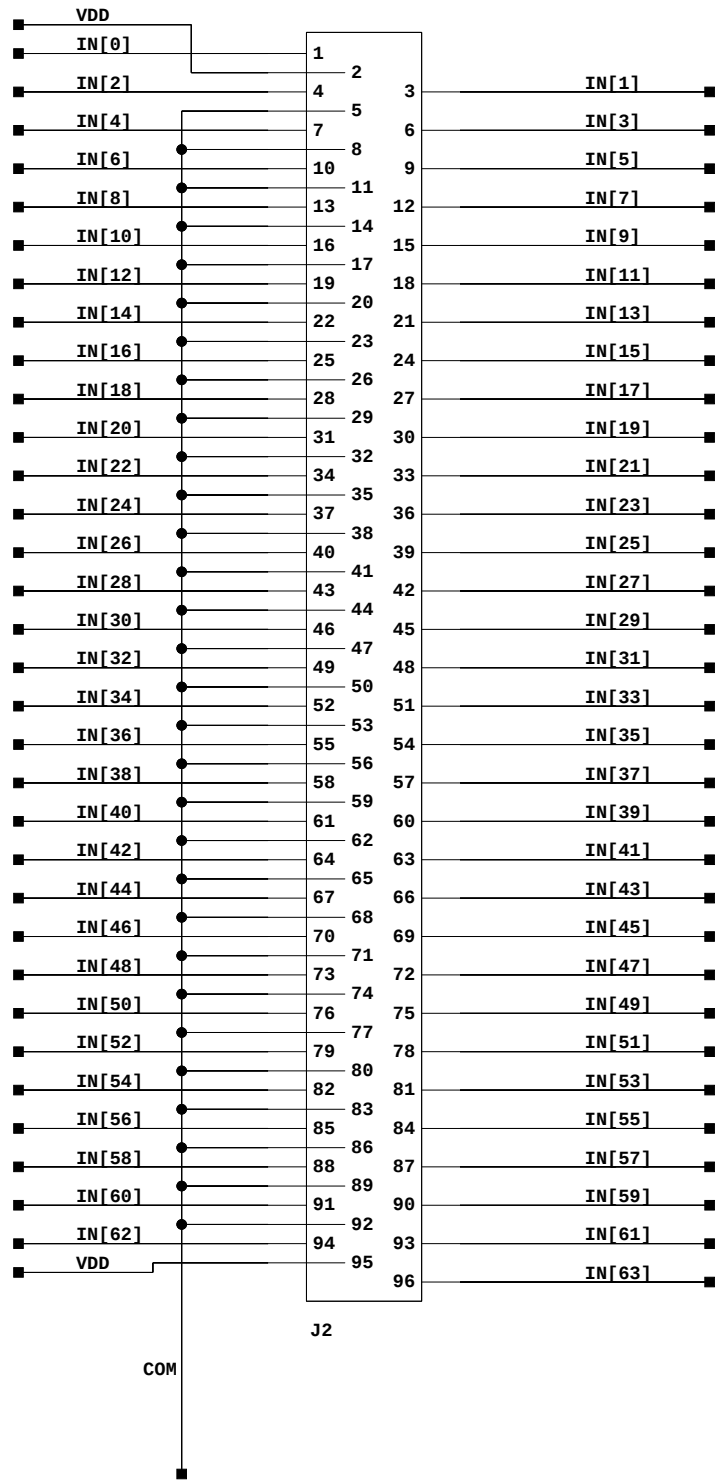
GND

EN

Enable by tying to VIN
in LDO by

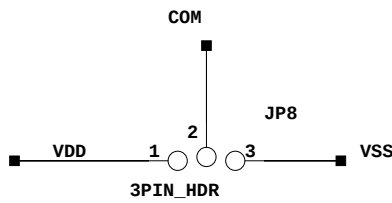
Output voltages from external LDO

VOUT

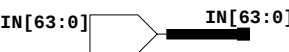


COM is a common reference voltage representing e.g. other wire plane.
VDD is the positive power reference voltage
VSS is the negative power reference voltage

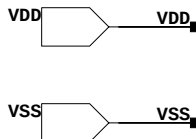
Reference voltage selection



Input signals to ASIC



Reference voltages



14/01/2019:08:48

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DTFR			D	
CHKR				