DUNE FRONT END MOTHERBOARD - REVISION B
University of Hawaii at Manoa IDL
Adapted from Brookhaven Design and SLAC Cold Board

POWER RAW

LDO 2.5V_D

LDO 2.5V_A

Default Op Conditions

LVDS data buffer

DATA out to WIB
WIB clk to CRYO
WIB SACI to CRYO

(all LDOs and power options have enable pins and jumpers to load and unload)

128 data channels

54x64

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DUNE FRONT END MOTHER BOARD
UNIVERSITY OF HAWAII MANOA INSTRUMENT DEVELOPMENT LAB
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8pin 10pin

default unloaded
sense lines. Keep resistors close toasic. in between both
Testpoints

Input protection diode load options
load R266,267 for VDD
load R46,49,200,202 for VSS

internal LDO testpoints

Ext. Monitor
Select raw power in or ldo 2.5 out

load R128 for LDO, R129 for raw PWR

load R130 for LDO, R131 for raw PWR
Select raw power in or ldo 2.5 out

load R159 for LDO, R160 for raw PWR

load R161 for LDO, R162 for raw PWR
Input Signal Connectors
Tied to VSS and either VSS/VDD determined by loads, see page 3.
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Input Protection channels

Resistors are not loaded, values of 1G

Note: Inductors are instead loaded by 0ohm R using same footprint
REGR_BIAS to 3.3V

LVDS Drivers

Load R3, 4, 7, 8, 9, 10, 11, 12 and C398, 399, 400, 401, 402, 403, 404, 405 to use drivers

Instead load R253, 254, 255, 256, 258, 259, 260, 261 to bypass drivers