DUNE FRONT END MOTHERBOARD - REVISION B
University of Hawaii at Manoa IDL
Adapted from Brookhaven Design and SLAC Cold Board

Default Op Conditions

8pin
10pin

8pin
10pin

LDO 2.5V_D
LDO 2.5V_A

LVDS data buffer

CRYO Left

WIB
WIB clk to CRYO
WIB SACI to CRYO

128 data channels

(out all LDOs and power options have
enable pins and jumpers to load a)
sense lines. Keep resistors close to asic. in between both
Testpoints

Input protection diode load options:
- Load R266,267 for VDD
- Load R46,49,200,202 for VSS

internal LDO testpoints
Select raw power in or LDO 2.5 out

load R128 for LDO, R129 for raw PWR

load R130 for LDO, R131 for raw PWR
**Left Digital 2.5V**

Select raw power in or ldo 2.5 out

- Load R159 for LDO, R160 for raw PWR
- Load R161 for LDO, R162 for raw PWR
Input Signal Connectors
Tied to VSS and either VSS/VDD determined by loads, see page 3
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Input Protection channels

Resistors are not loaded, values of 1G

Note: Inductors are instead loaded by 0ohm R using same footprint
LVDS Drivers

Load R3, 4, 7, 8, 9, 10, 11, 12 and C398, 399, 400, 401, 402, 403, 404, 405 to use drivers
Instead load R253, 254, 255, 256, 258, 259, 260, 261 to bypass drivers