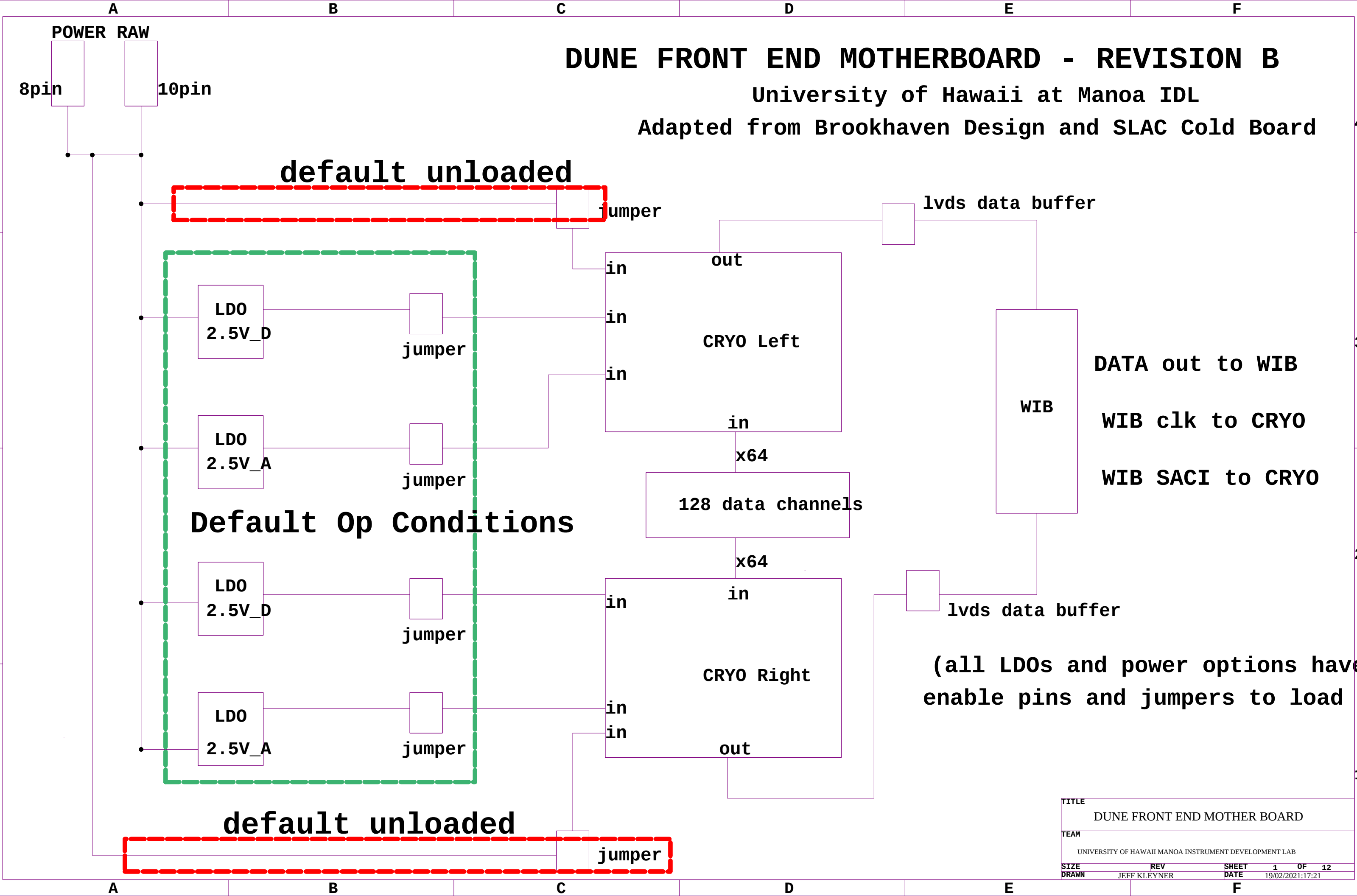
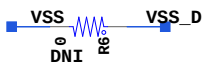
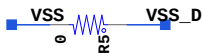
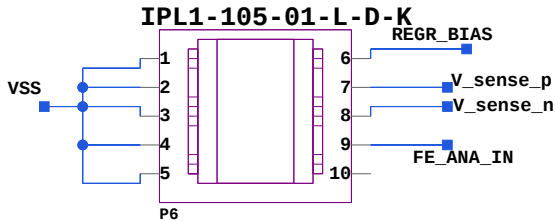
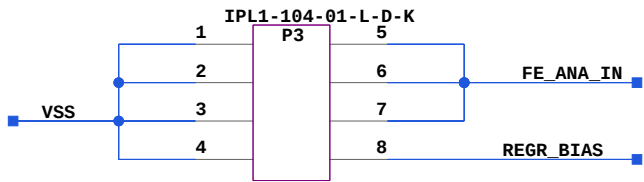


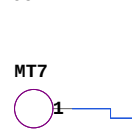
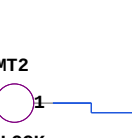
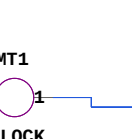
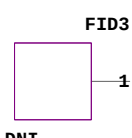
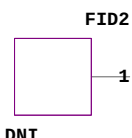
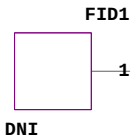
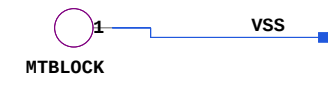
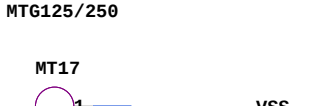
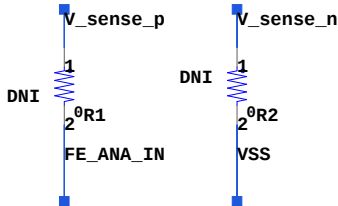


TITLE				
DUNE FRONT END MOTHER BOARD				
TEAM				
UNIVERSITY OF HAWAII MANOA INSTRUMENT DEVELOPMENT LAB				
SIZE	REV	SHEET	1	OF 12
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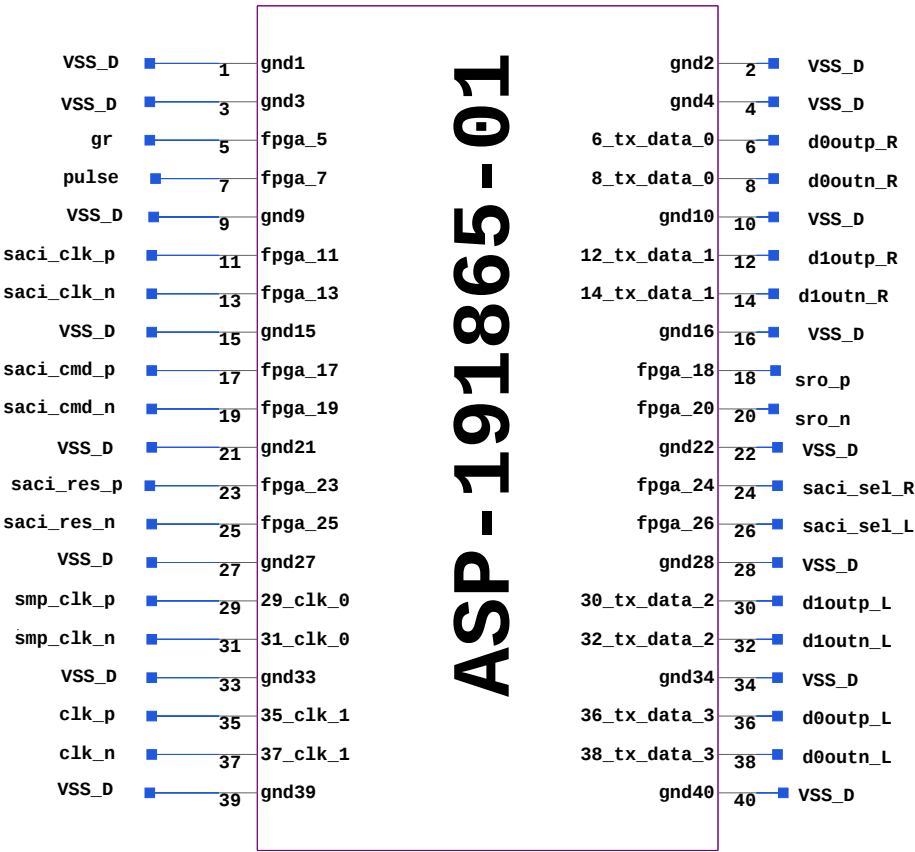
Raw Pwr



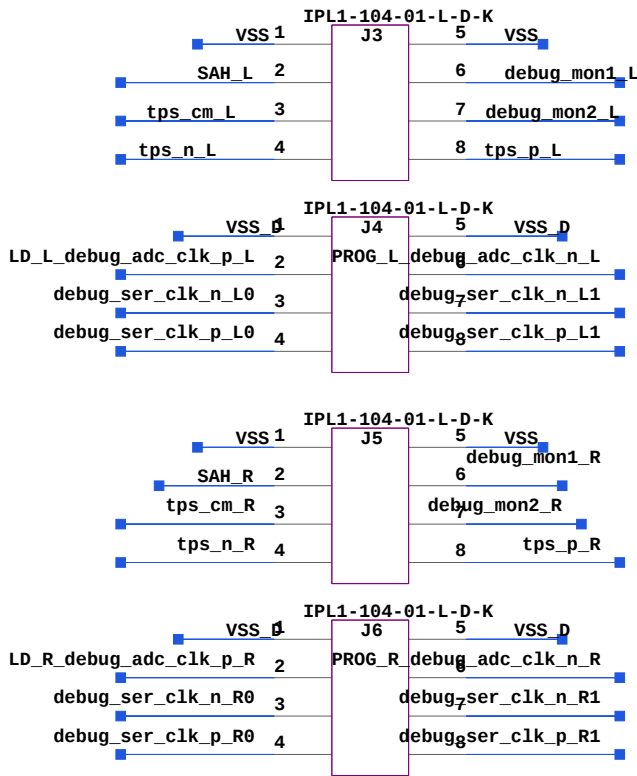
sense lines. Keep resistors close to asic. in between both



WIB DATA Connector

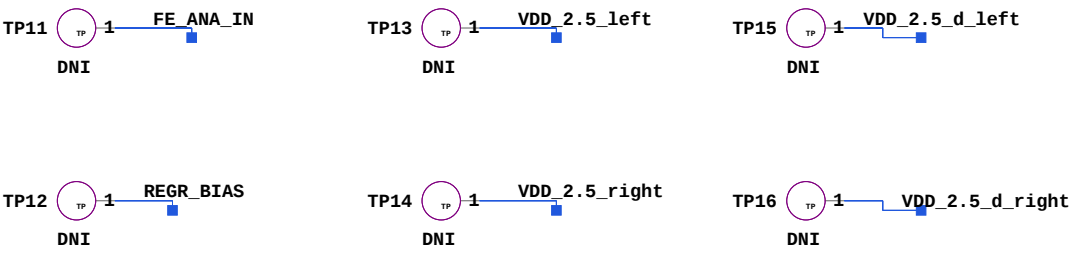


Debug connectors

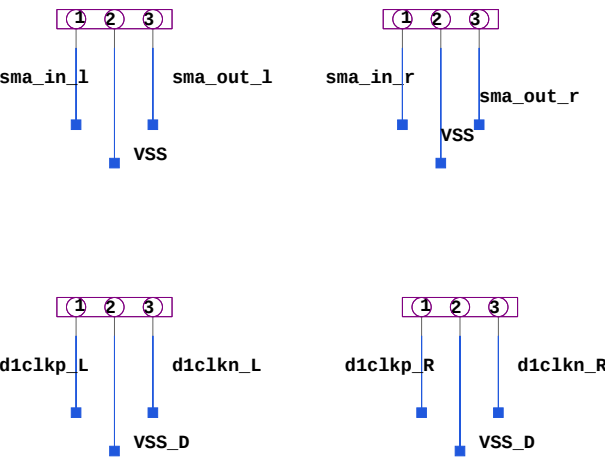


TITLE				
DUNE FRONT END MOTHER BOARD				
TEAM				
UNIVERSITY OF HAWAII MANOA INSTRUMENT DEVELOPMENT LAB				
SIZE	REV	SHEET	2	OF 12
DRAWN	JEFF KLEYNER	DATE	02/03/2021:17:23	

Testpoints

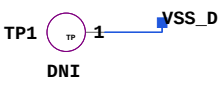
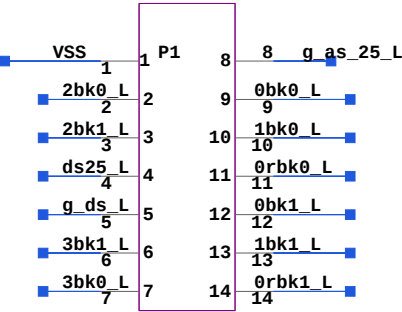
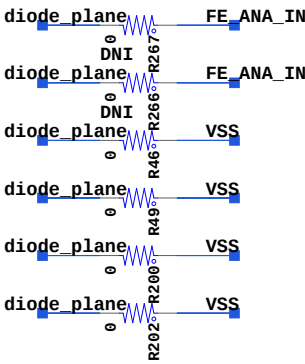


Ext. Monitor

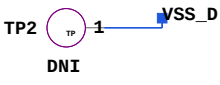
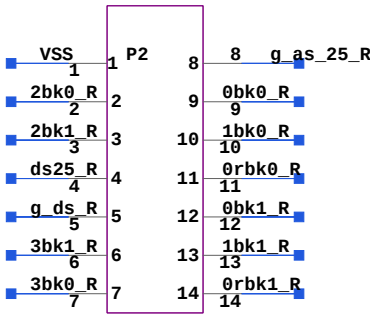


Input protection diode load options

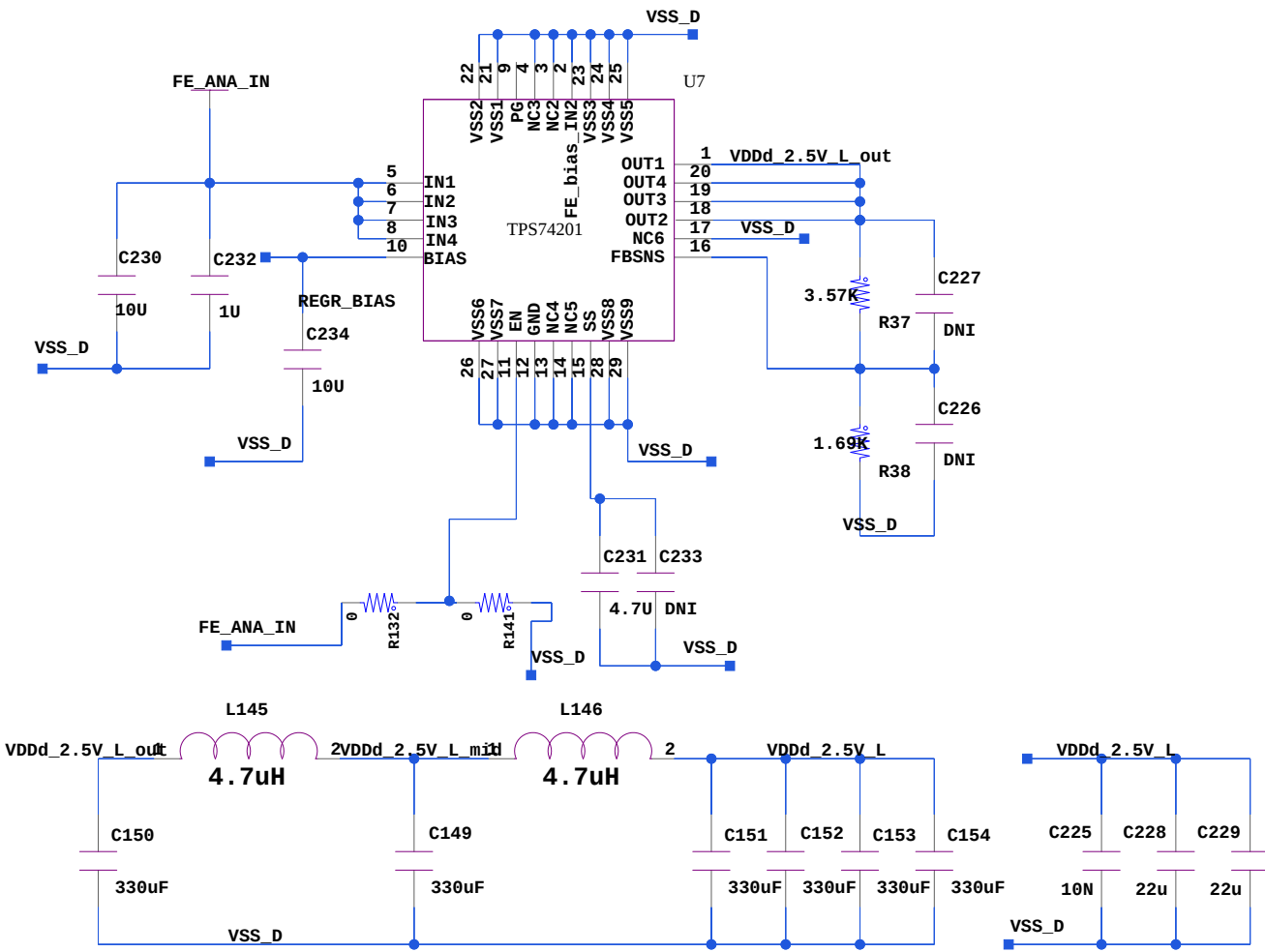
load R266,267 for VDD
load R46,49,200,202 for VSS



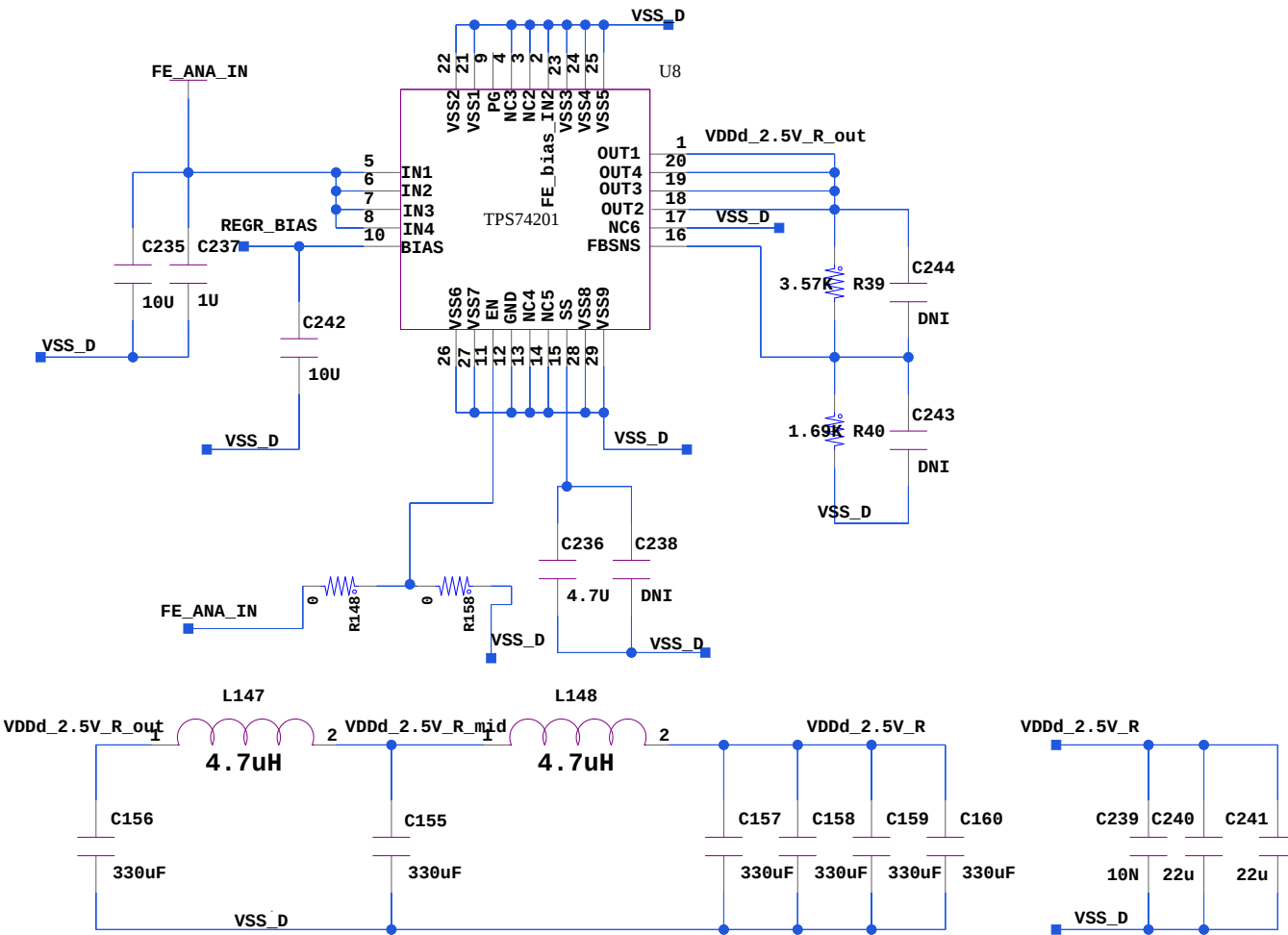
internal LDO testpoints



Left Digital 2.5V



Right Digital 2.5V



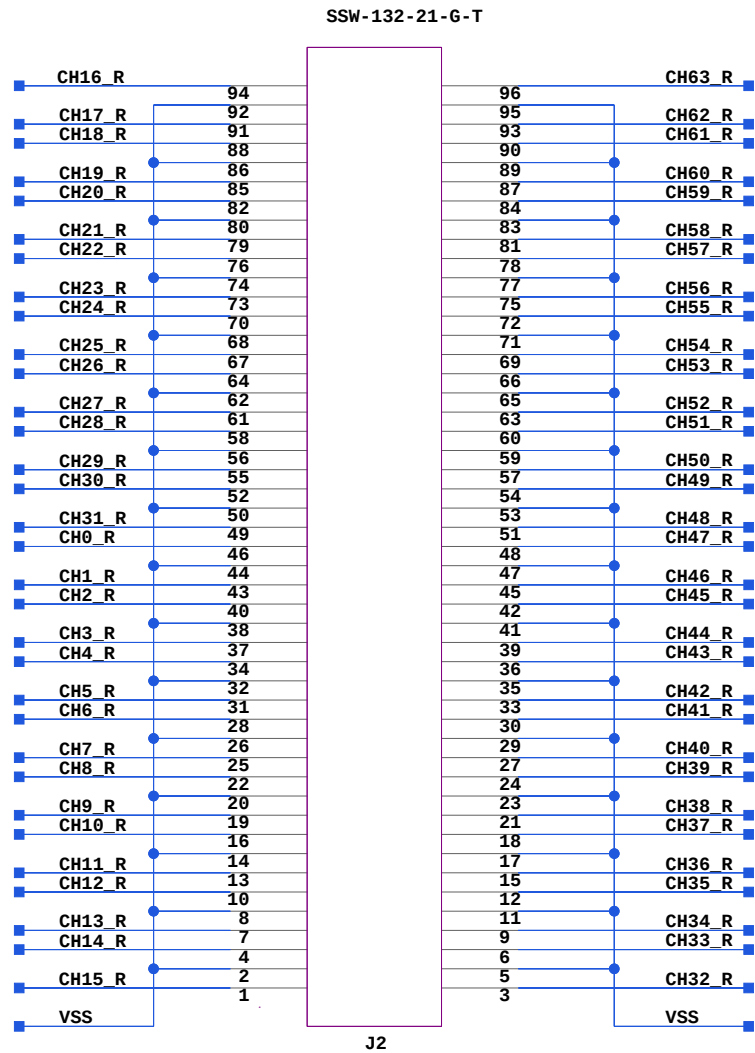
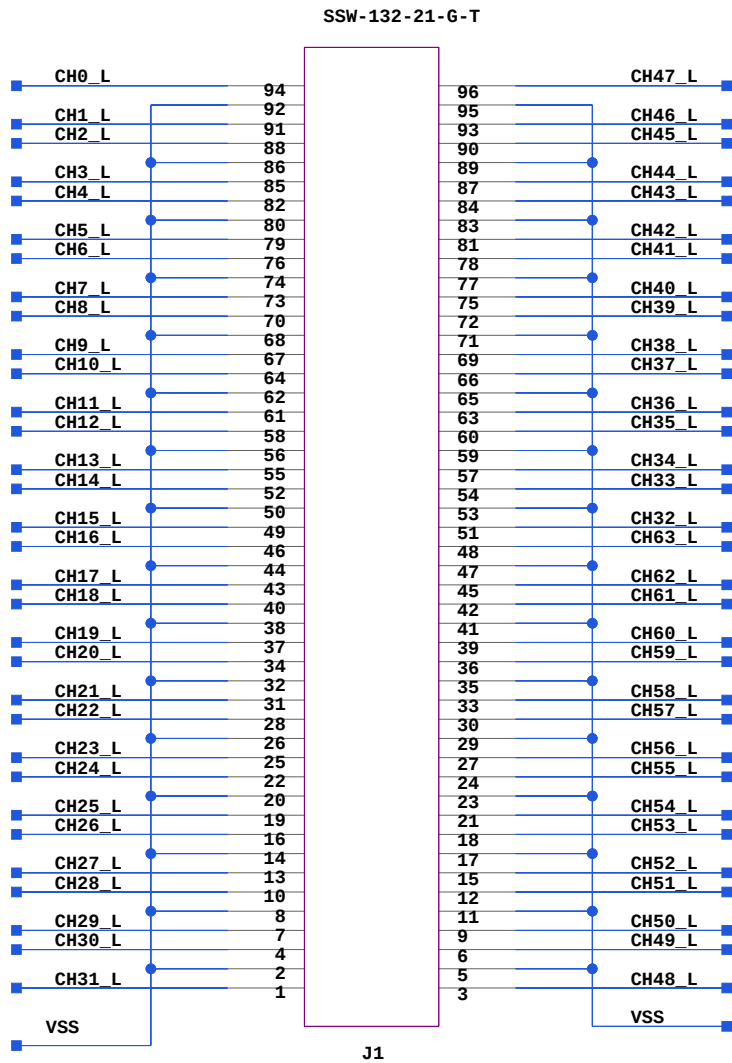
Select raw power in or ldo 2.5 out



load R159 for LD0, R160 for raw PWR

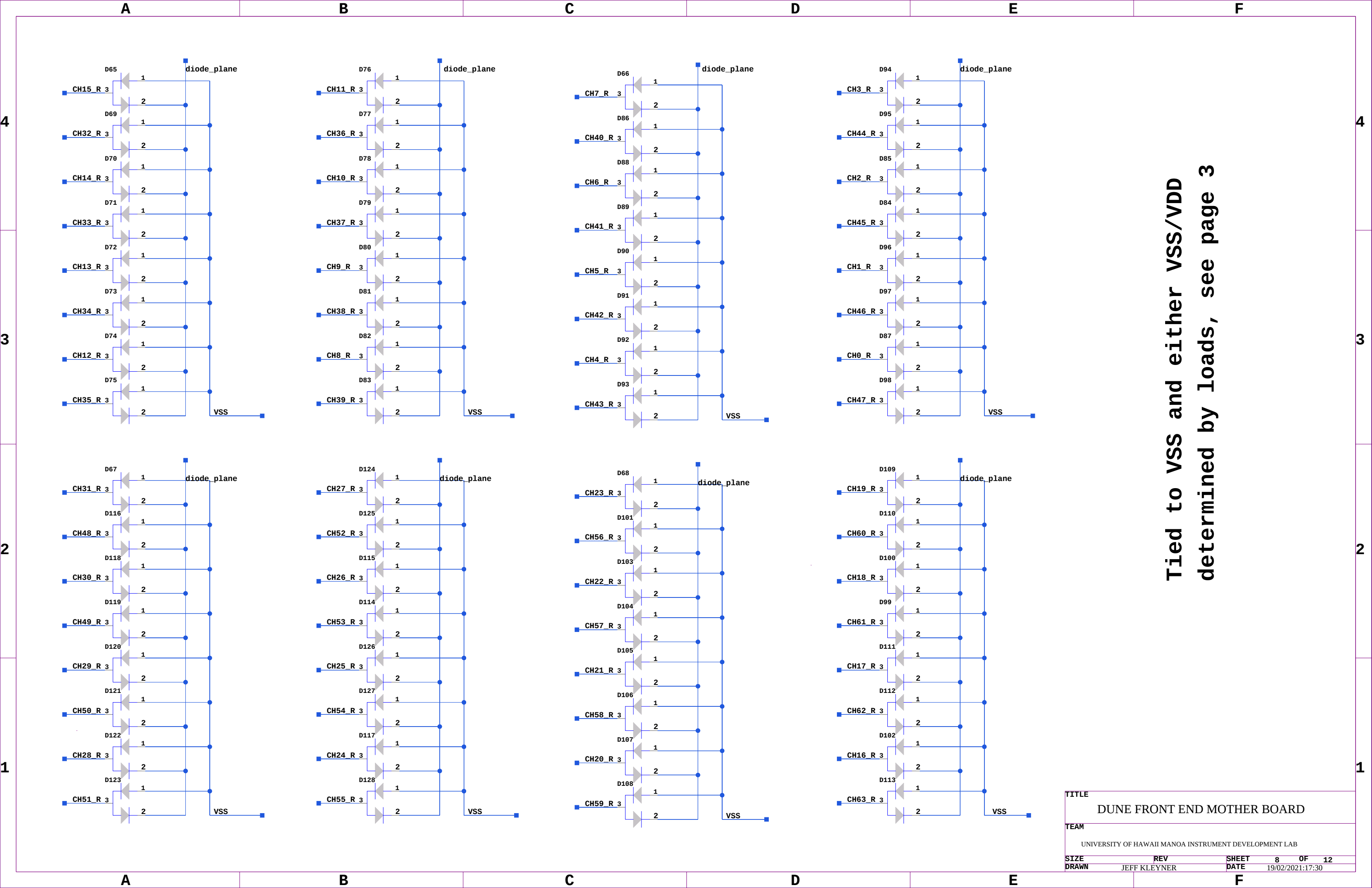
load R161 for LD0, R162 for raw PWR

TITLE					
DUNE FRONT END MOTHER BOARD					
TEAM					
UNIVERSITY OF HAWAII MANOA INSTRUMENT DEVELOPMENT LAB					
SIZE	REV	SHEET	6	OF	12
DRAWN	JEFF KLEYNER	DATE	02/03/2021:16:38		



Input Signal Connectors

TITLE				
DUNE FRONT END MOTHER BOARD				
TEAM				
UNIVERSITY OF HAWAII MANOA INSTRUMENT DEVELOPMENT LAB				
SIZE	REV	SHEET	7	OF 12
DRAWN	JEFF KLEYNER	DATE	18/02/2021:23:03	



4

3

2

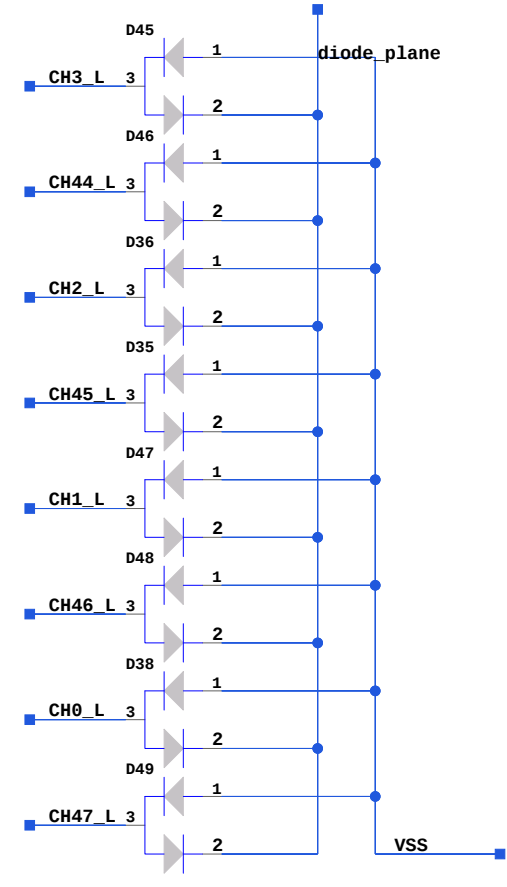
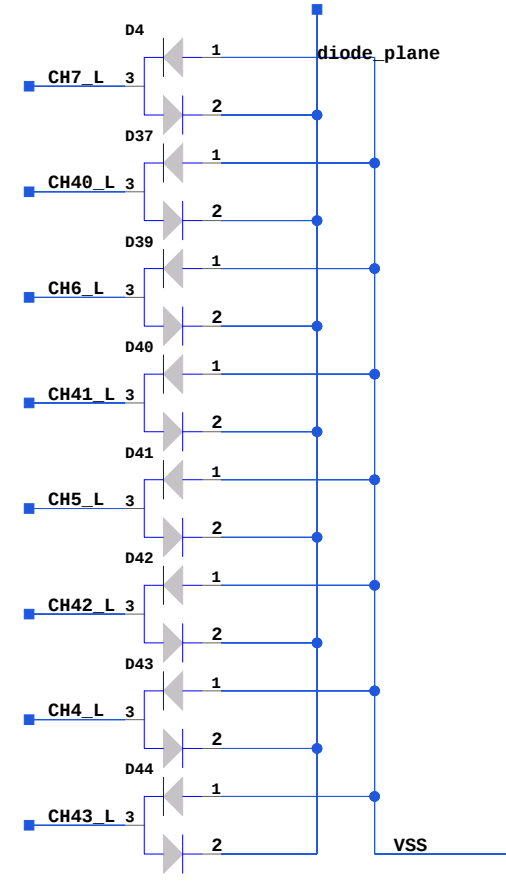
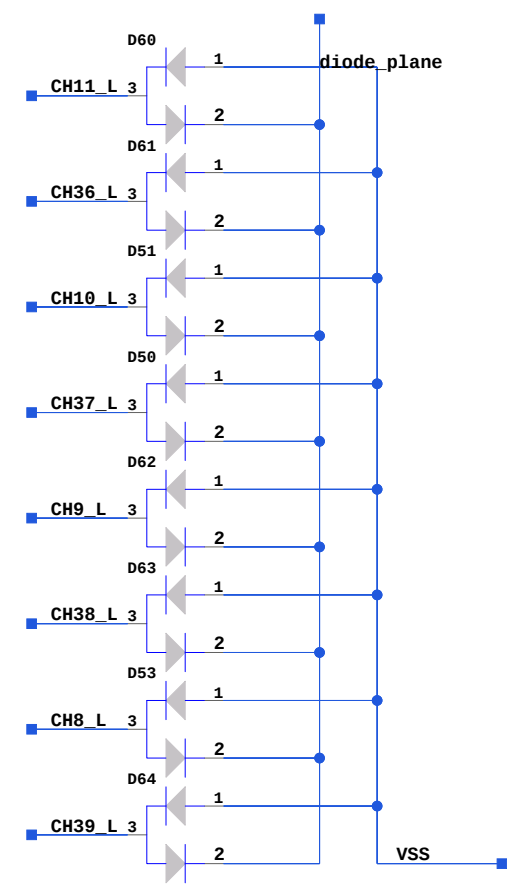
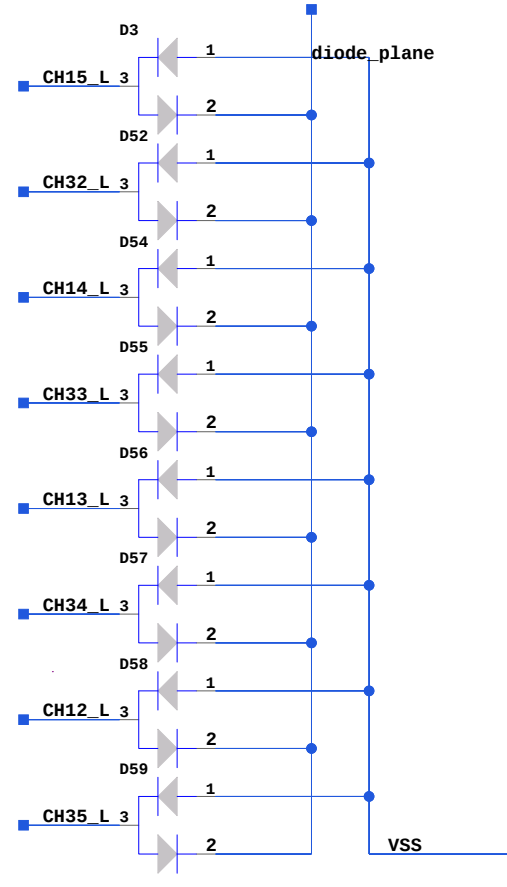
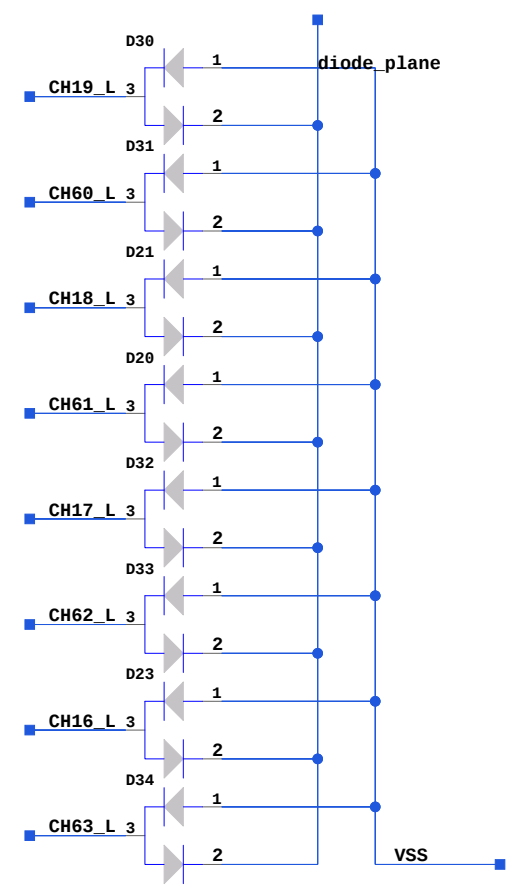
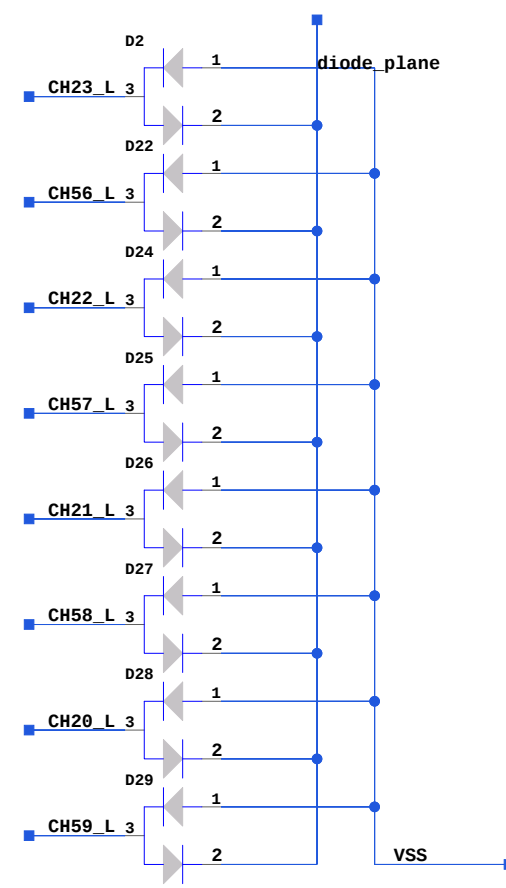
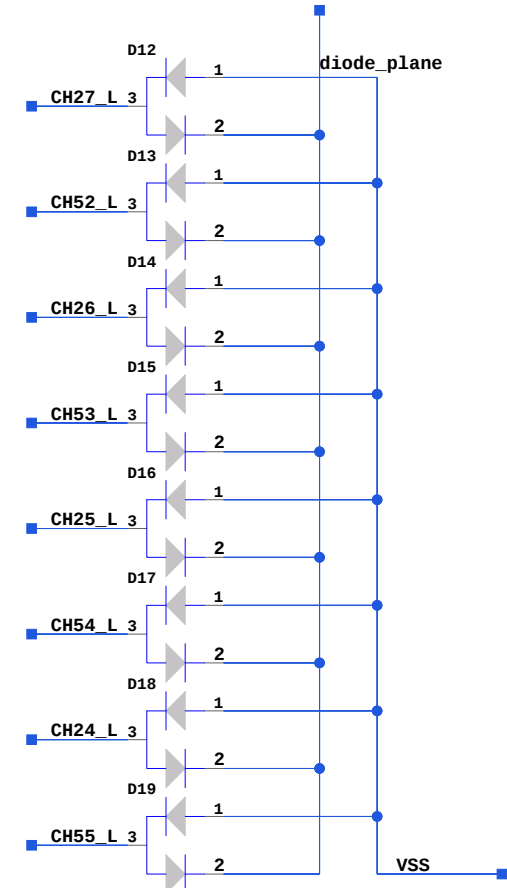
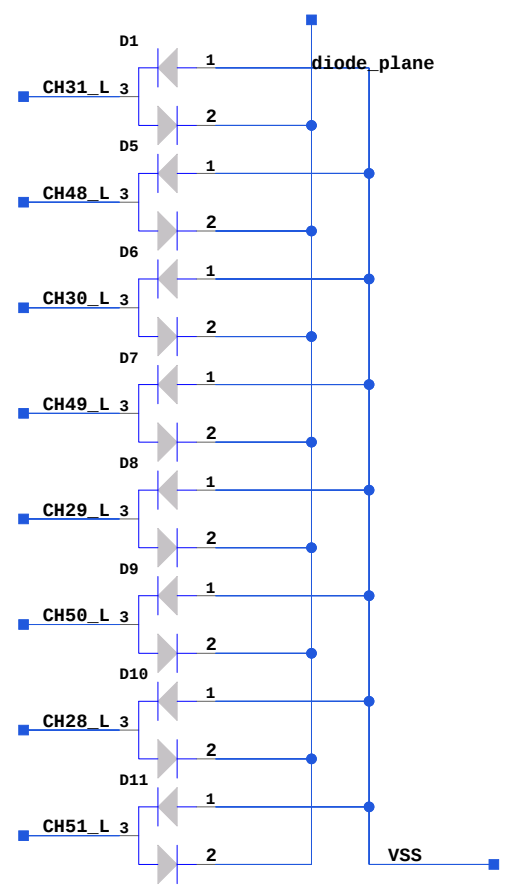
1

4

3

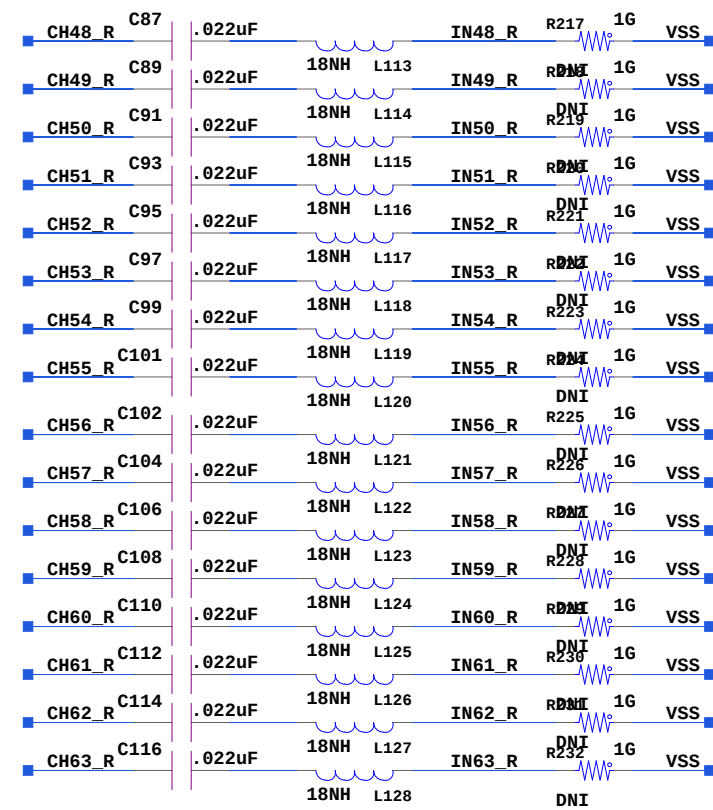
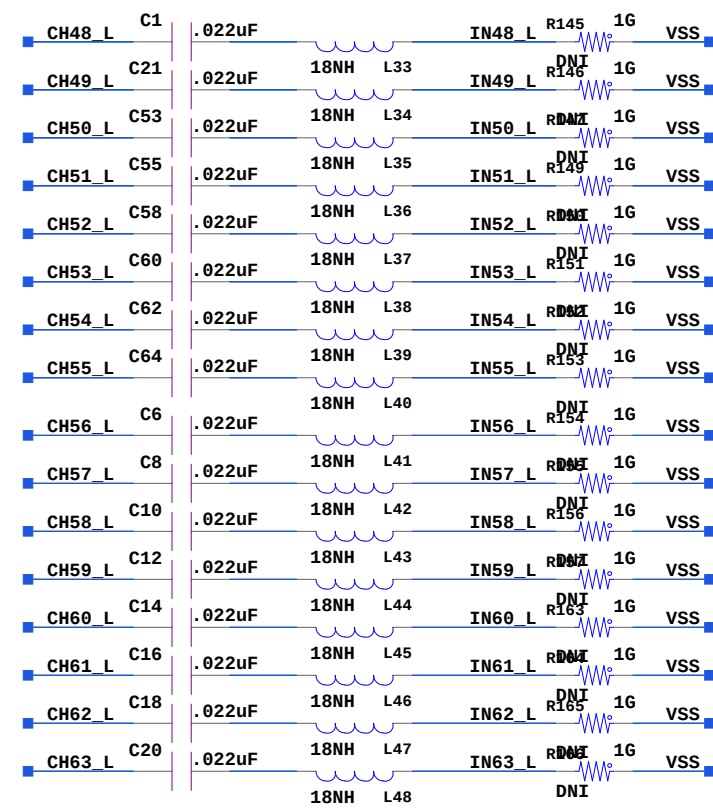
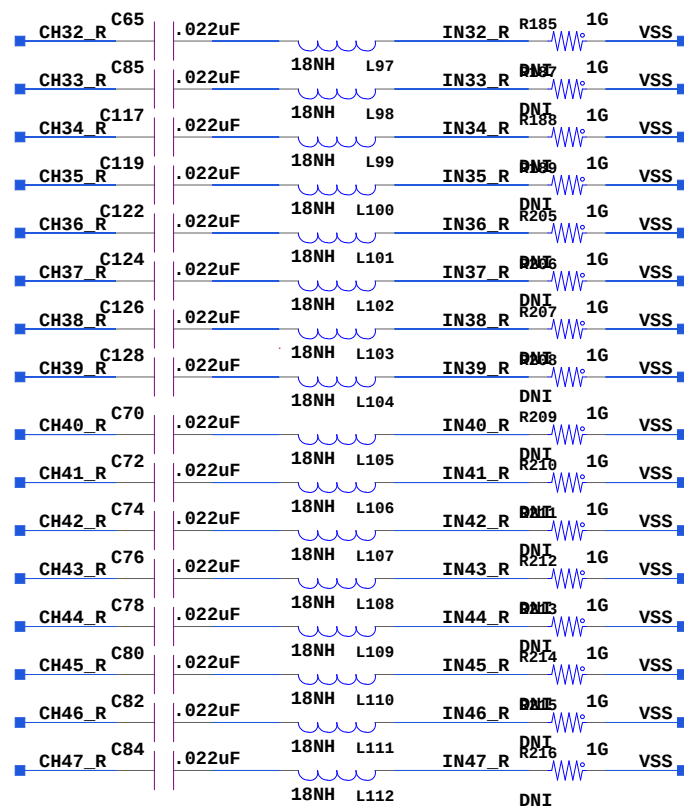
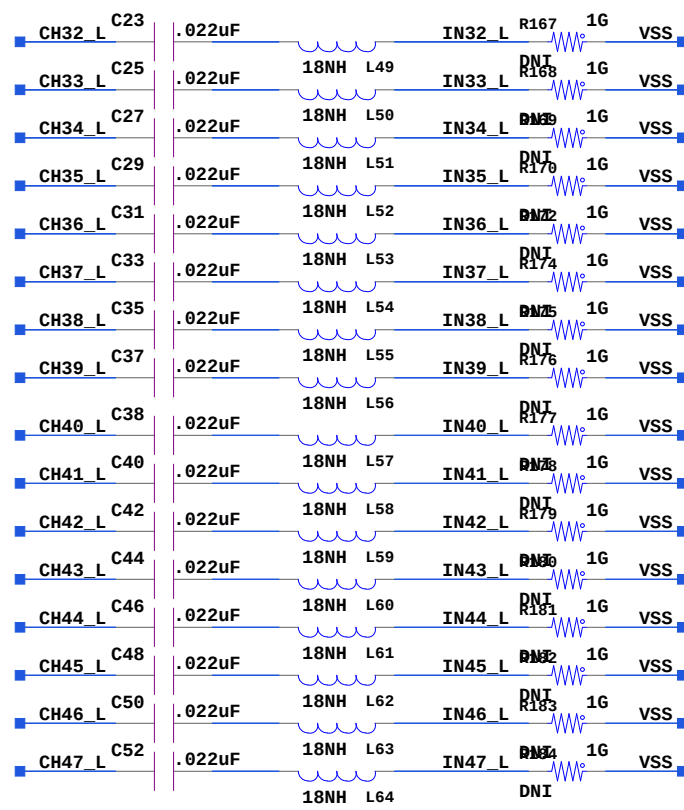
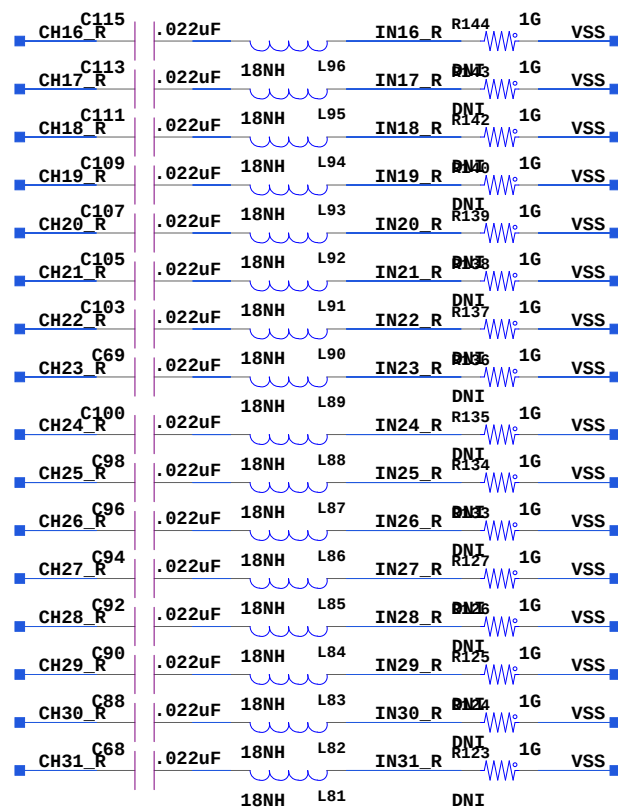
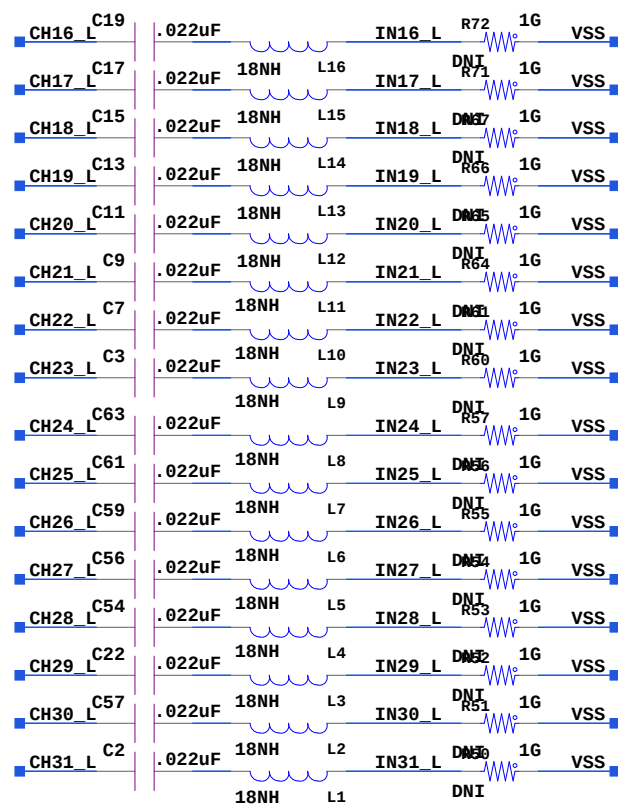
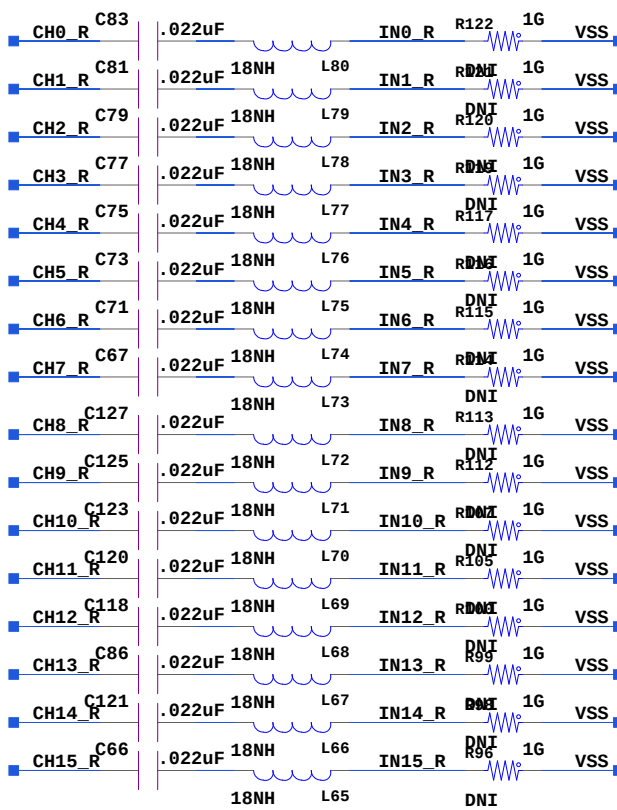
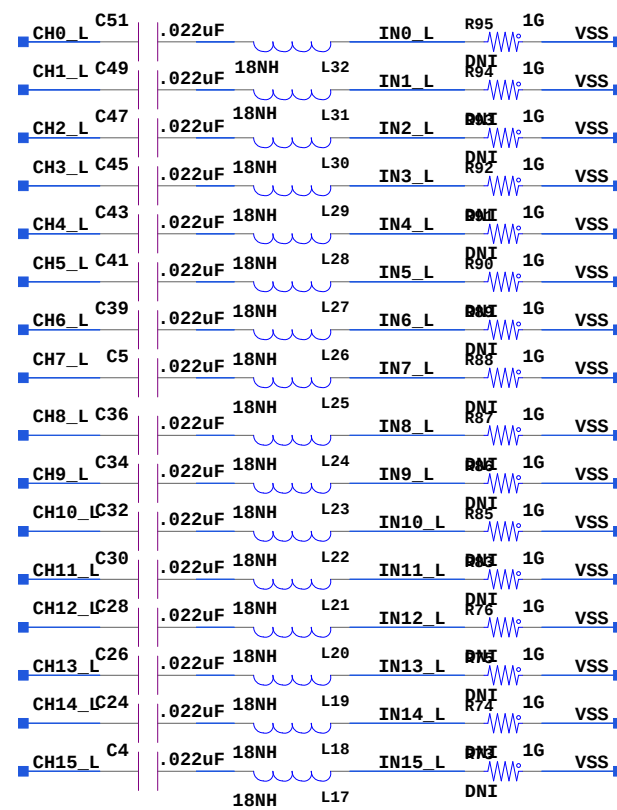
2

1



Tied to VSS and either VSS/VDD
determined by loads, see page 3

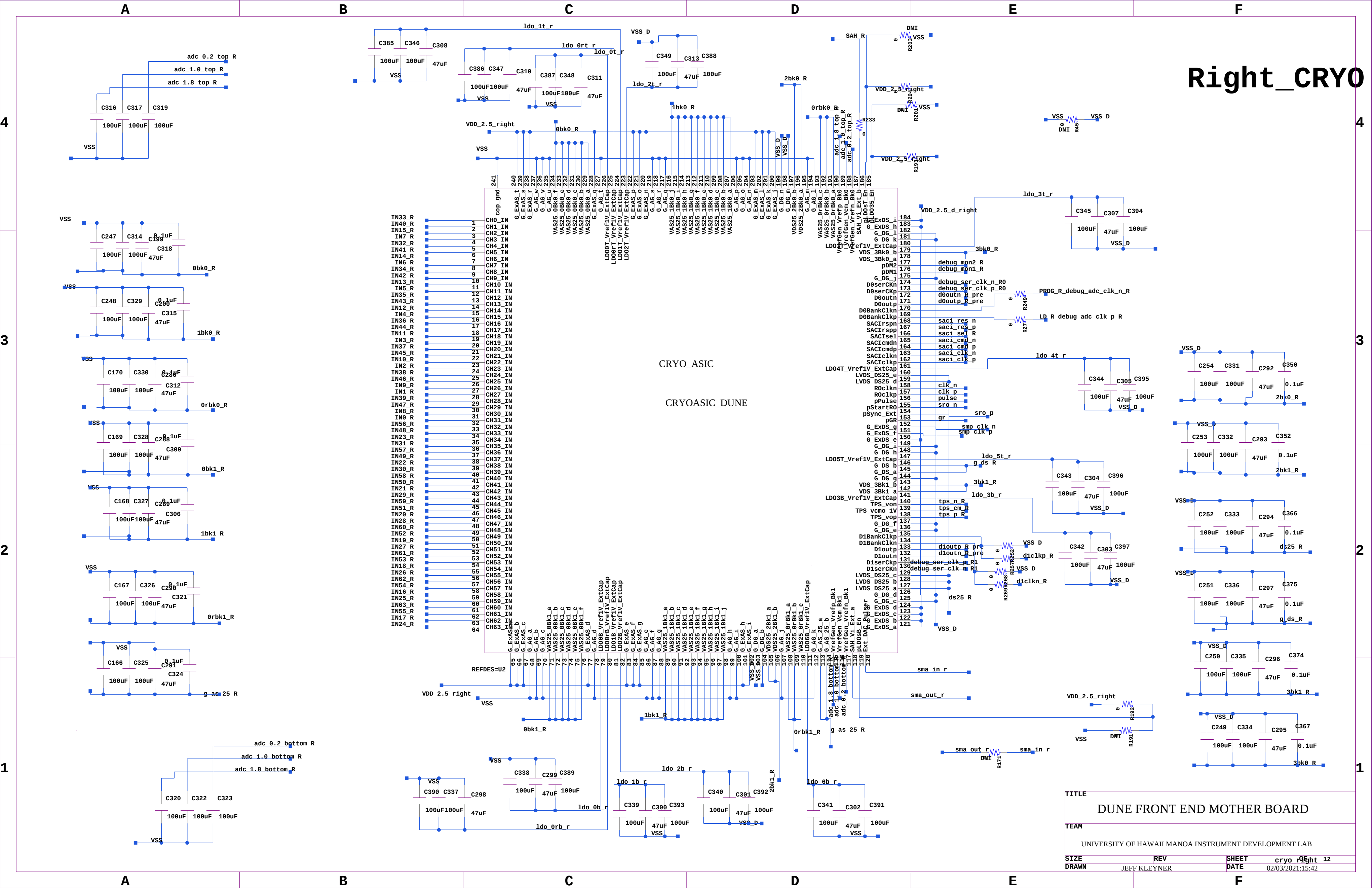
TITLE				
DUNE FRONT END MOTHER BOARD				
TEAM				
UNIVERSITY OF HAWAII MANOA INSTRUMENT DEVELOPMENT LAB				
SIZE	REV	SHEET	9	OF 12
DRAWN	JEFF KLEYNER	DATE	19/02/2021:17:30	



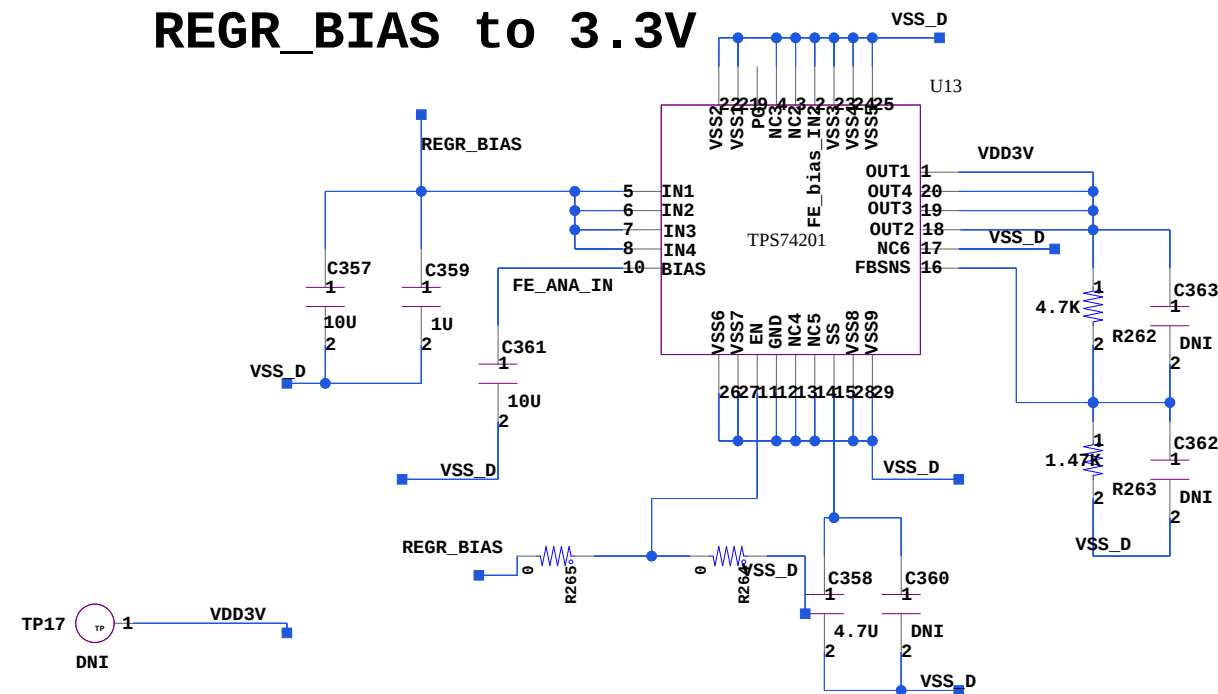
Input Protection channels

Resistors are not loaded, values of 1G

Note: Inductors are instead loaded by 0ohm R using same footprint

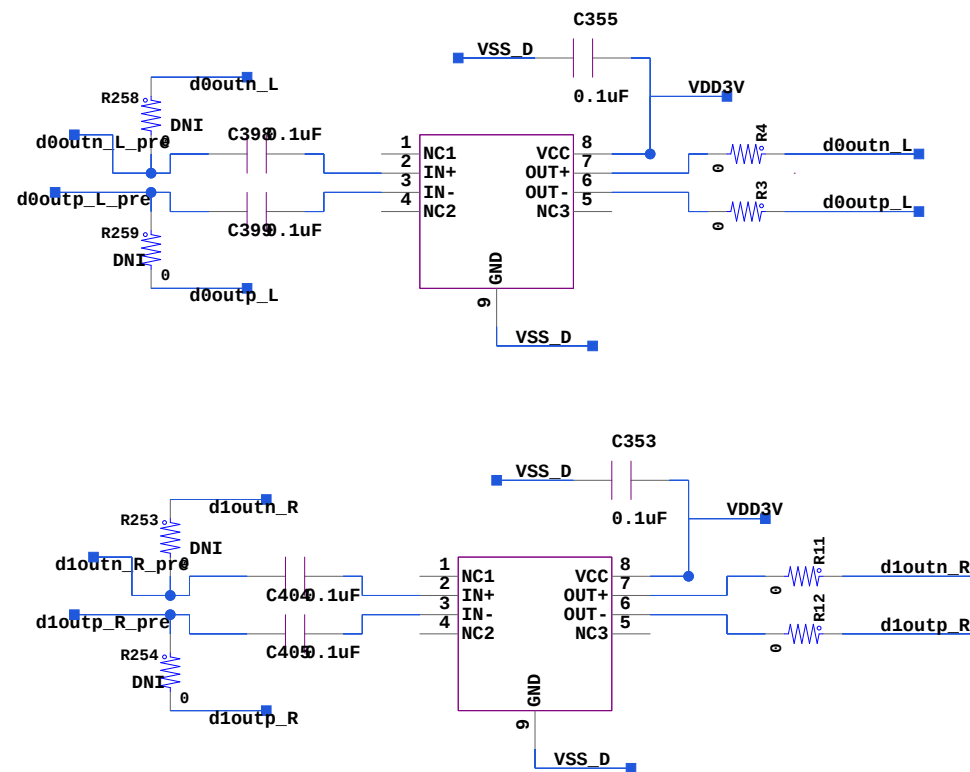
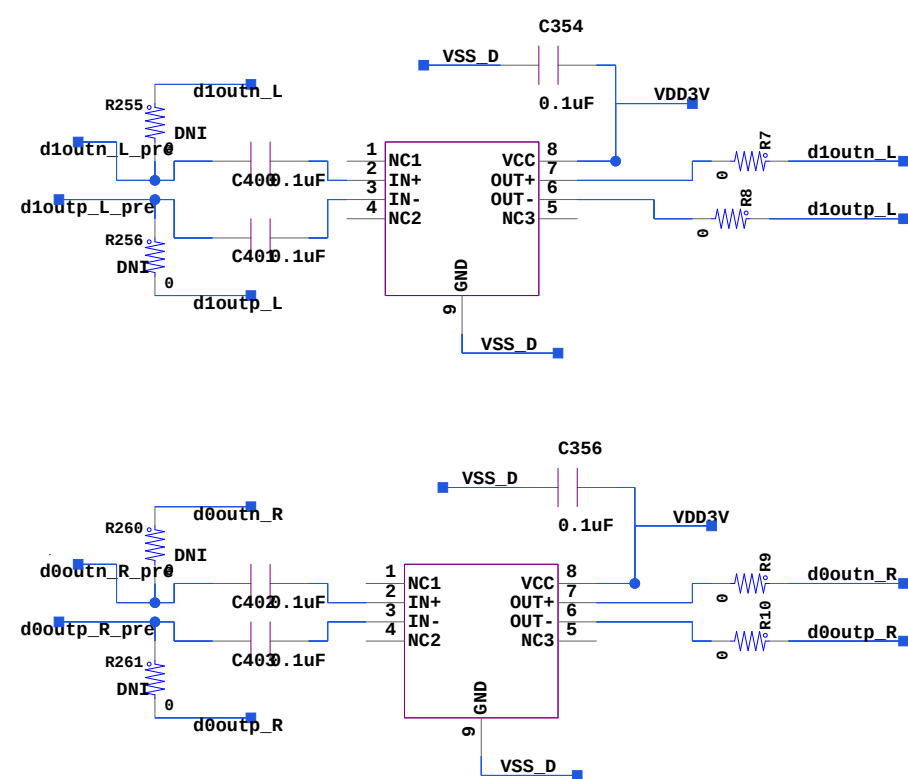


REGR_BIAS to 3.3V



LVDS Drivers

**Load R3,4,7,8,9,10,11,12 and C398,399,400,401,402,403,404,405 to use drivers
Instead load R253,254,255,256,258,259,260,261 to bypass drivers**



TITLE				
DUNE FRONT END MOTHER BOARD				
TEAM				
UNIVERSITY OF HAWAII MANOA INSTRUMENT DEVELOPMENT LAB				
SIZE	REV	SHEET	13	OF 12
DRAWN	JEFF KLEYNER	DATE	02/03/2021:16:42	