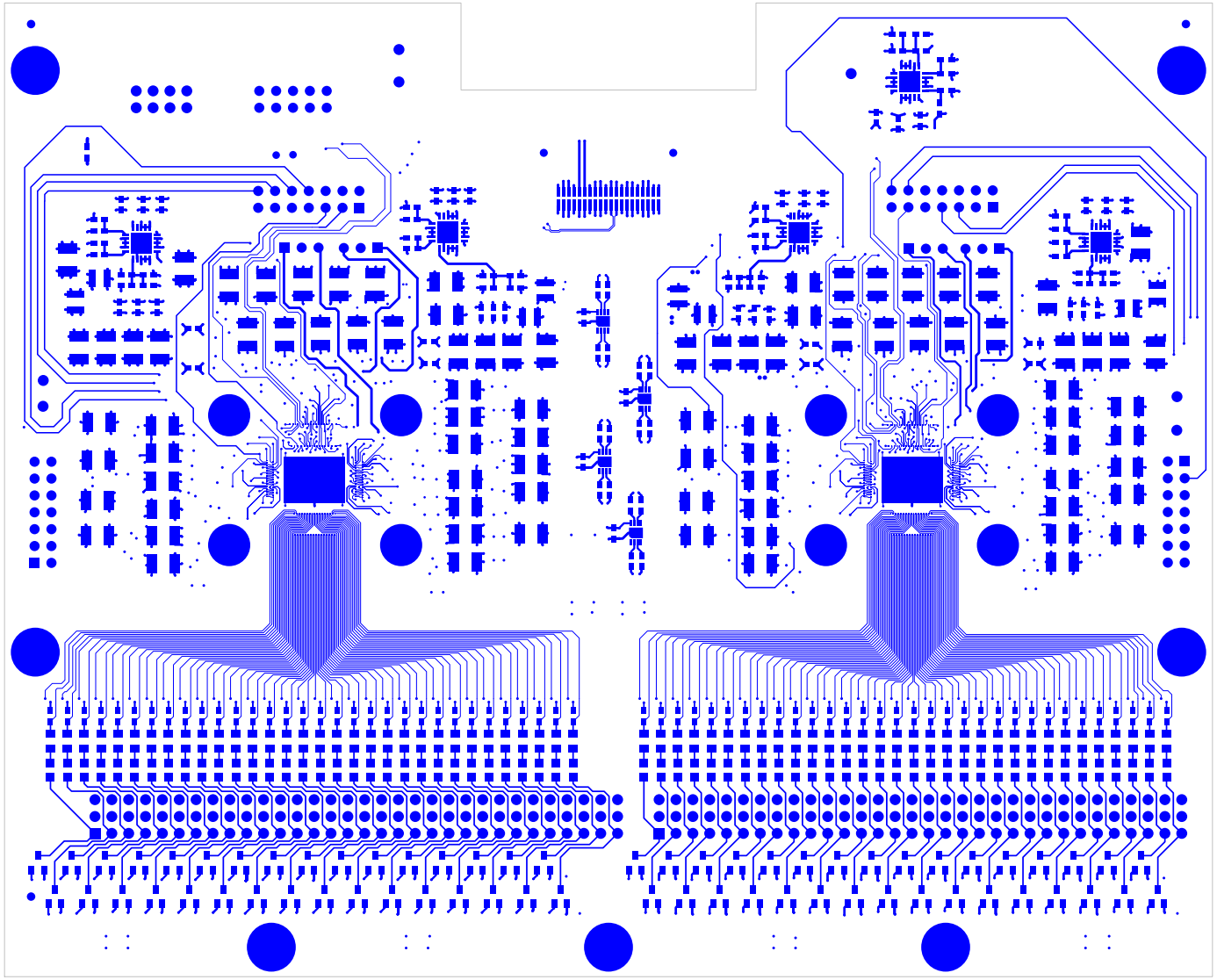
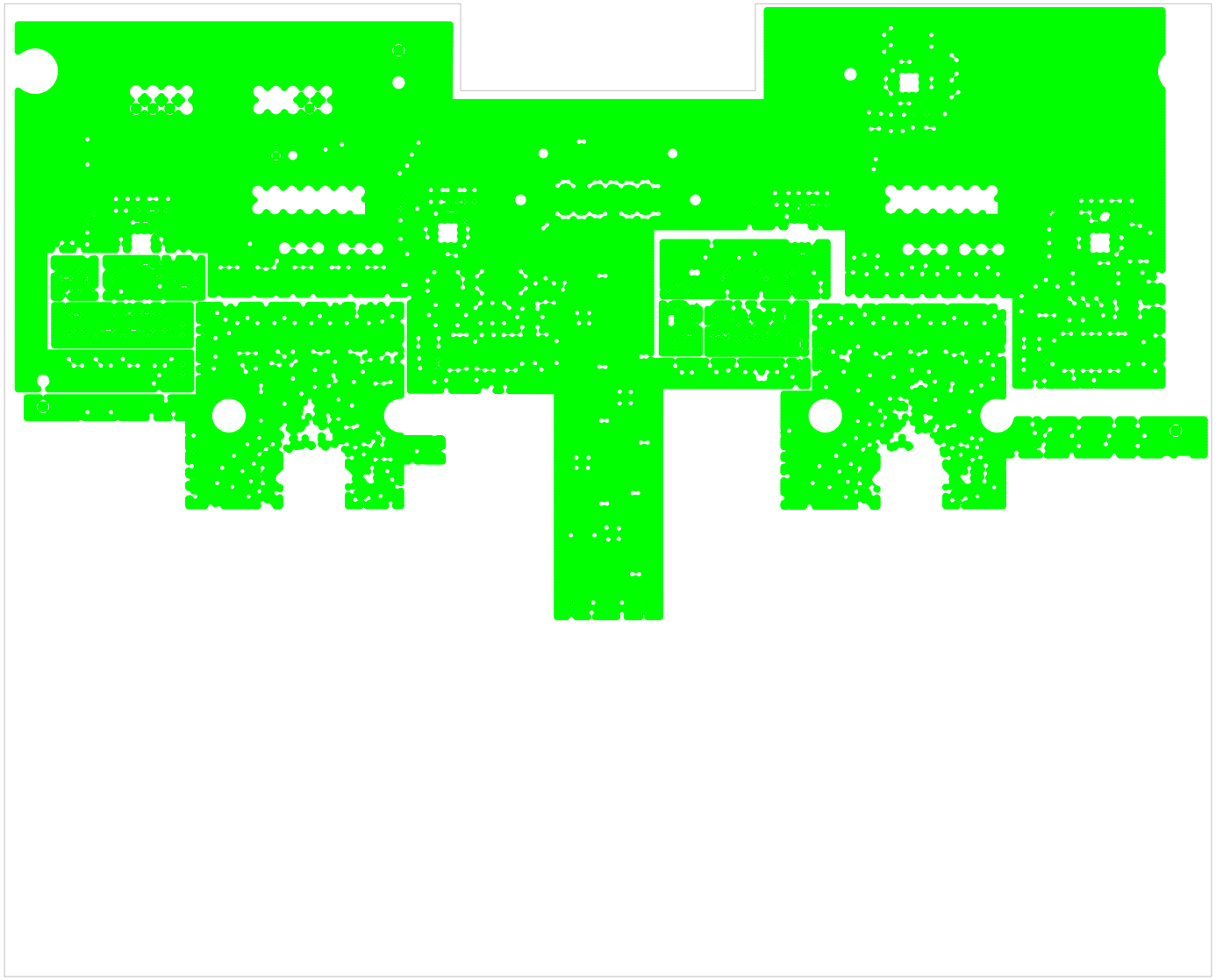
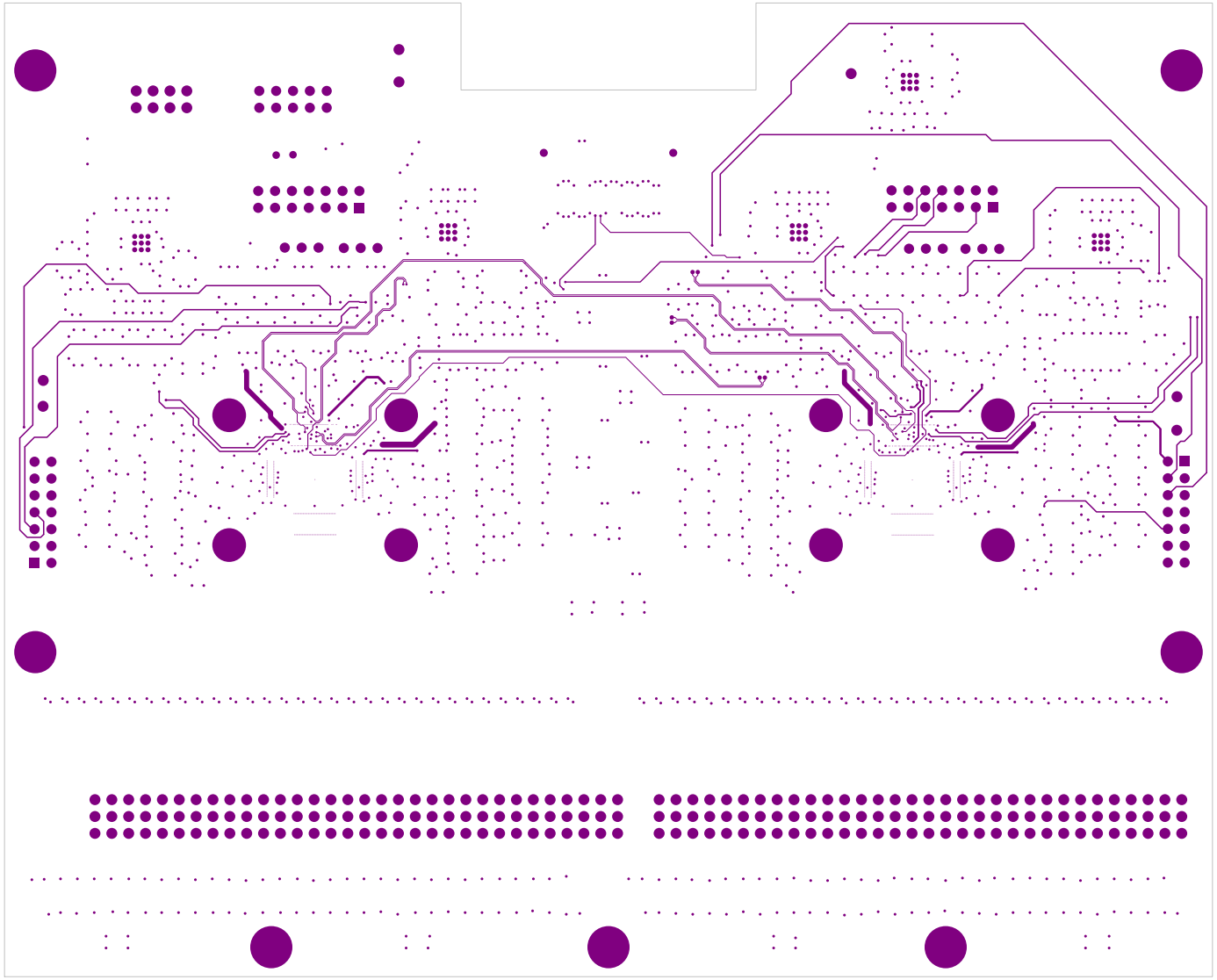
LAYER 1 – TOP COMPONENTS



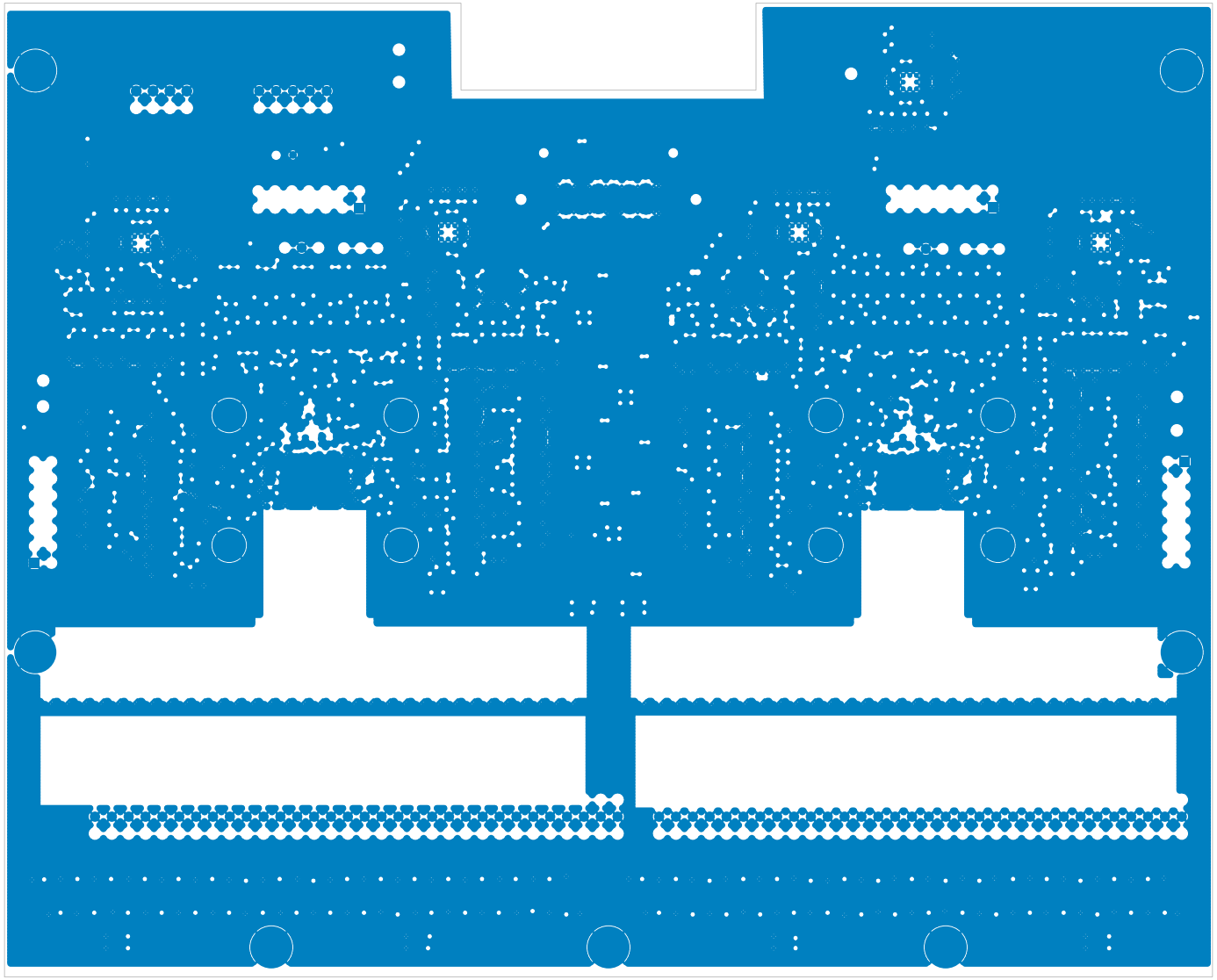
LAYER 2 – RAW POWER & ANALOG 2.5V PLANES



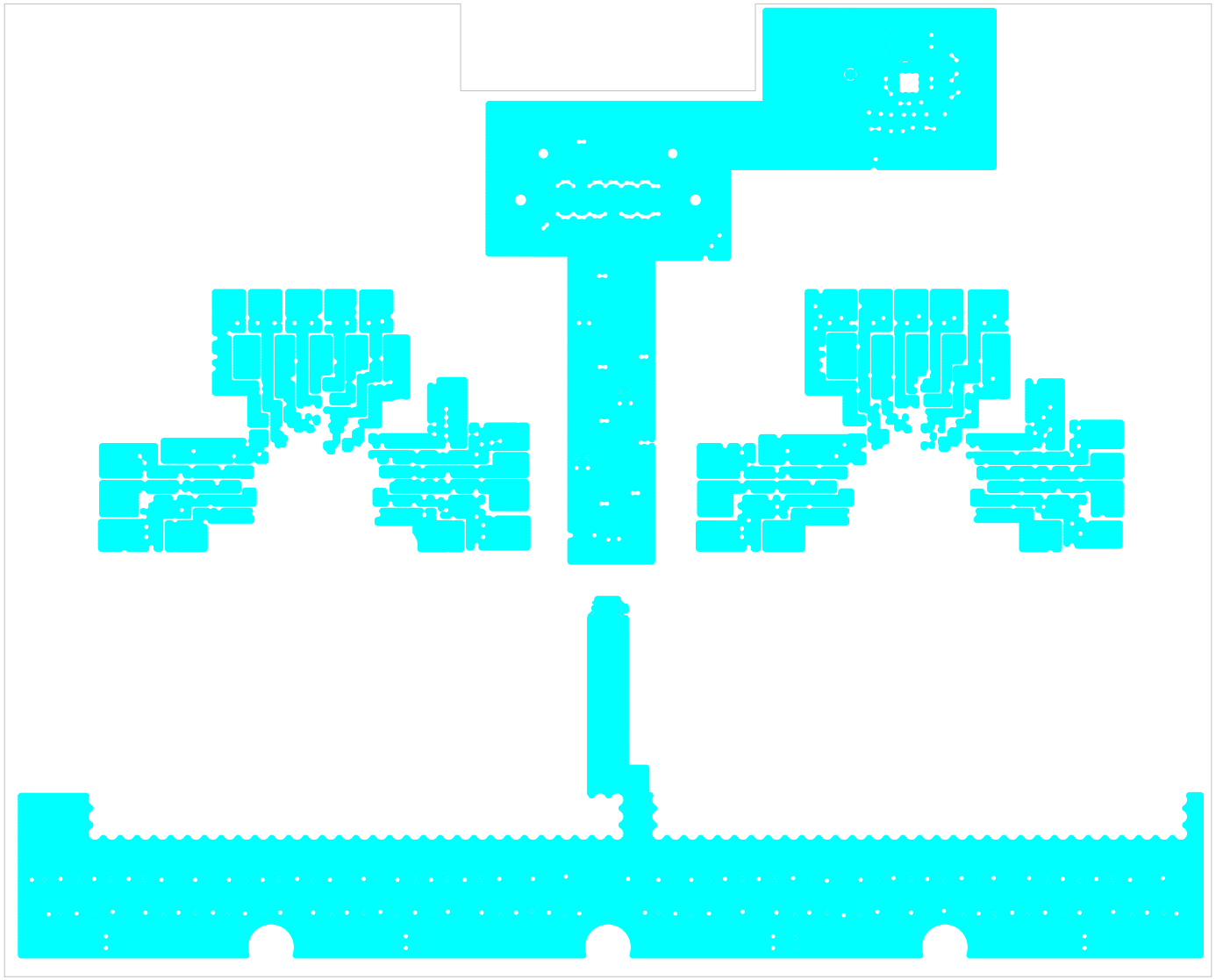
LAYER 3 – SIGNALS (100 OHM DIFF PAIRS)



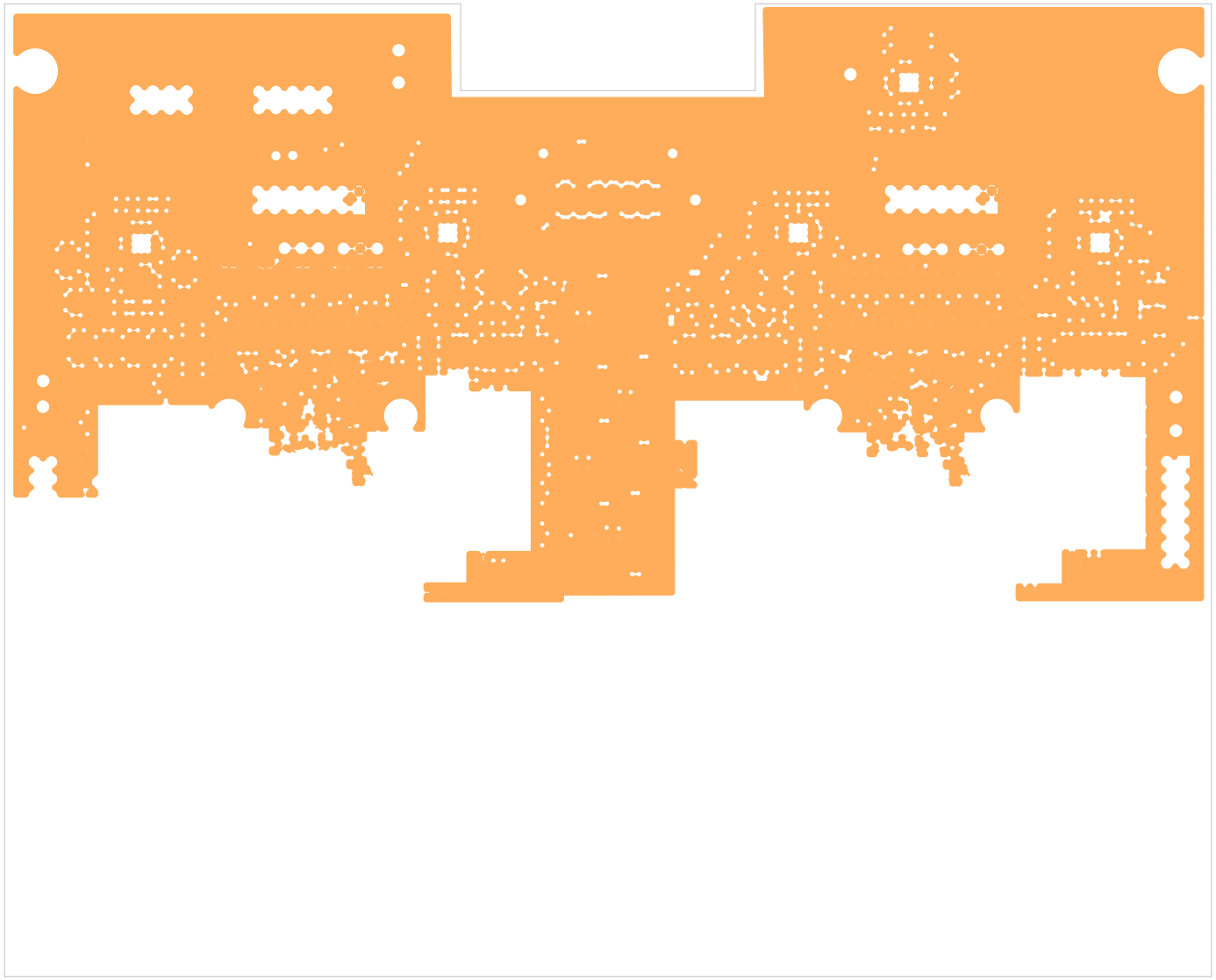
LAYER 4 – ANALOG GROUND PLANE



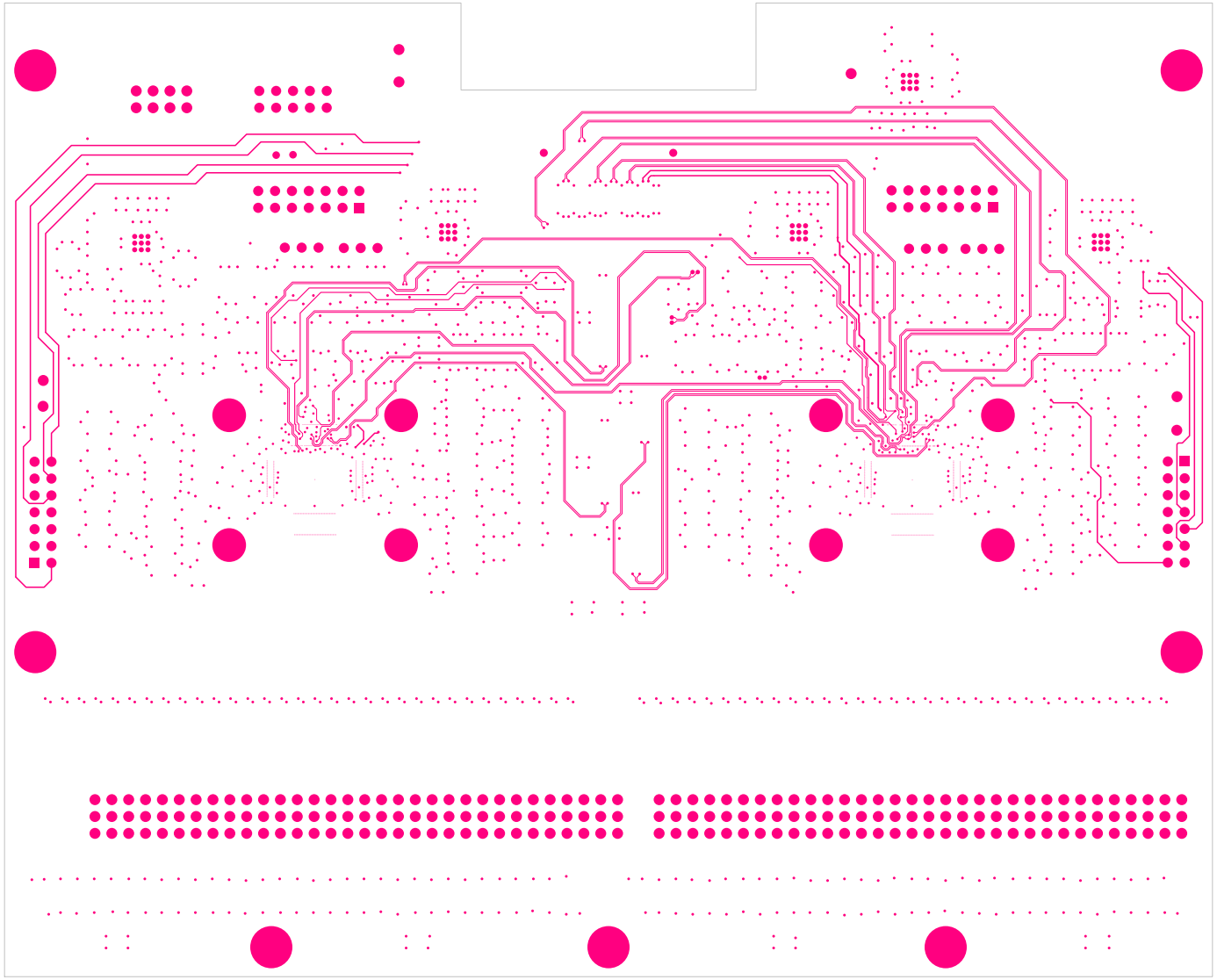
LAYER 5 – DIGITAL 3.3V & LDO FILTERING



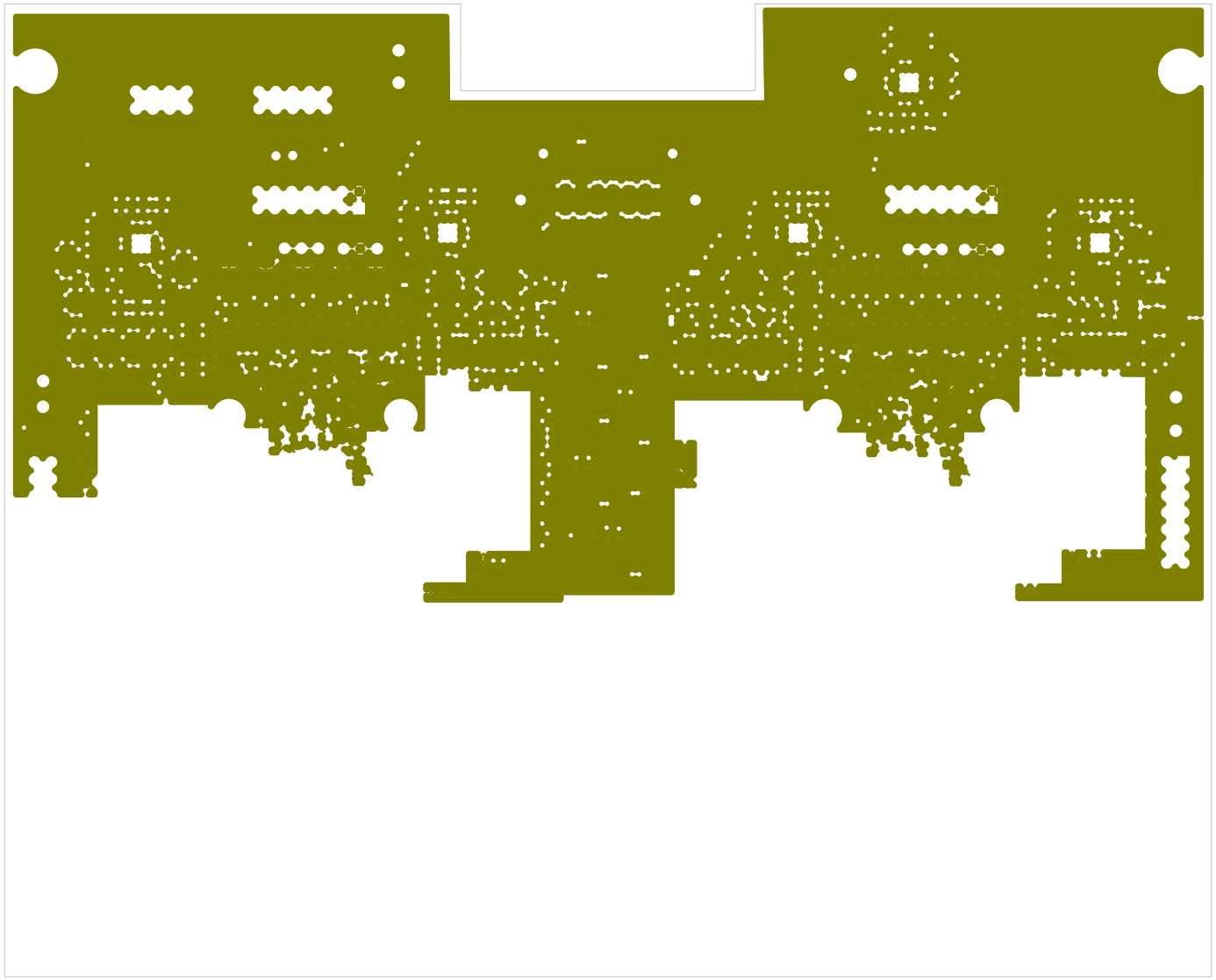
LAYER 6 – DIGITAL GROUND PLANE



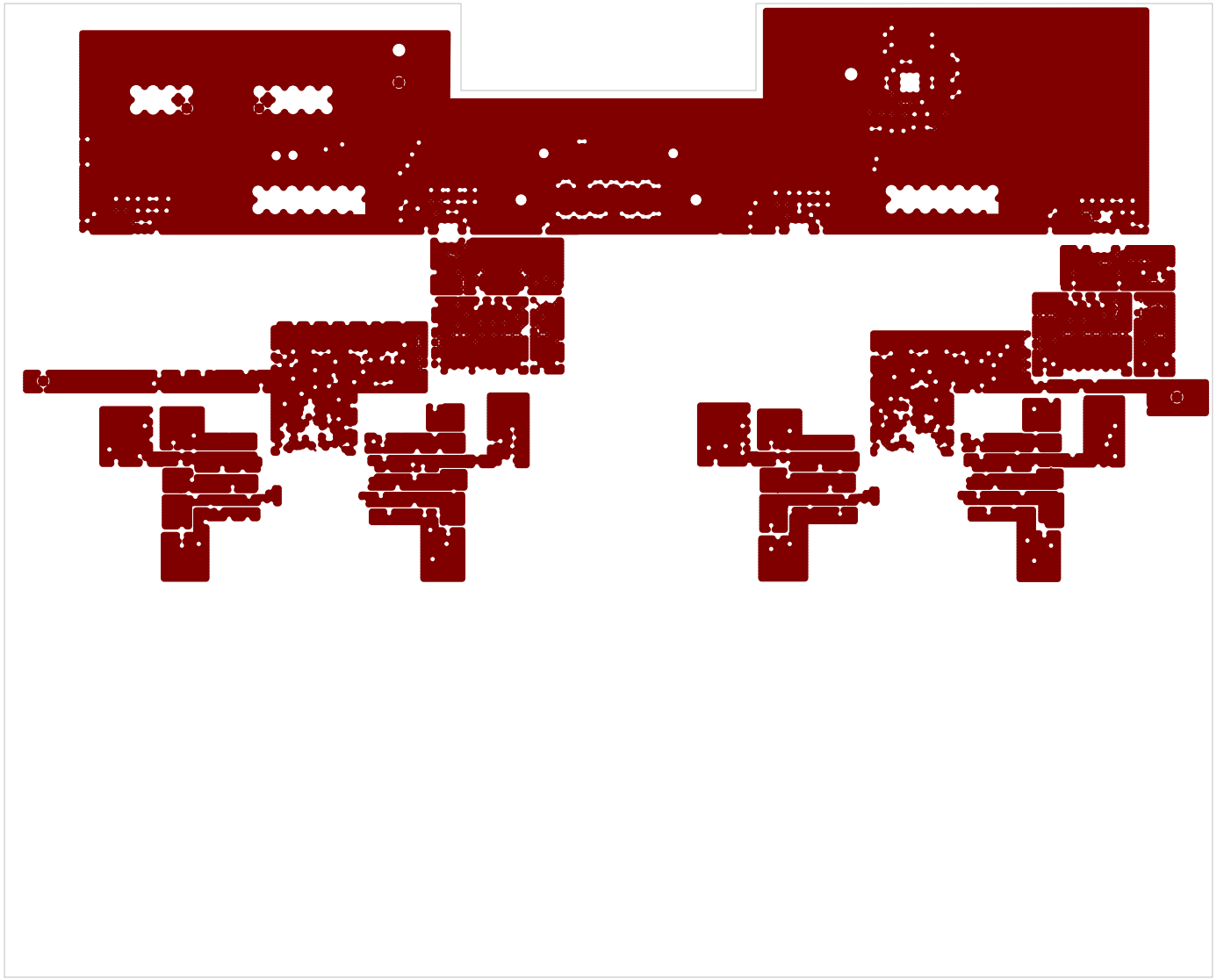
LAYER 7 – SIGNALS (100 OHM DIFF PAIRS)



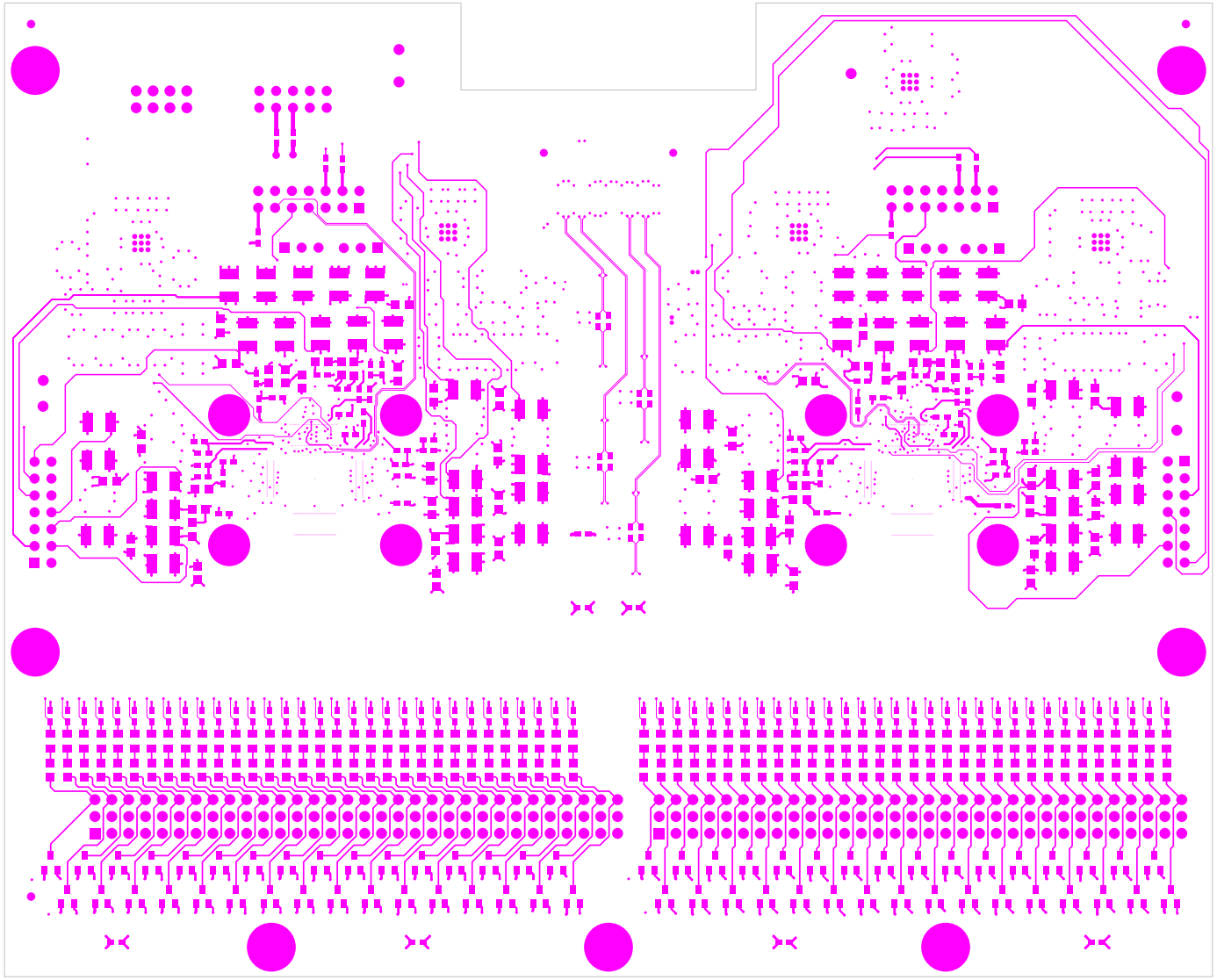
LAYER 8 – DIGITAL GROUND PLANE



LAYER 9 – DIGITAL 2.5V POWER & 5V REG BIAS & LDO FILTERING

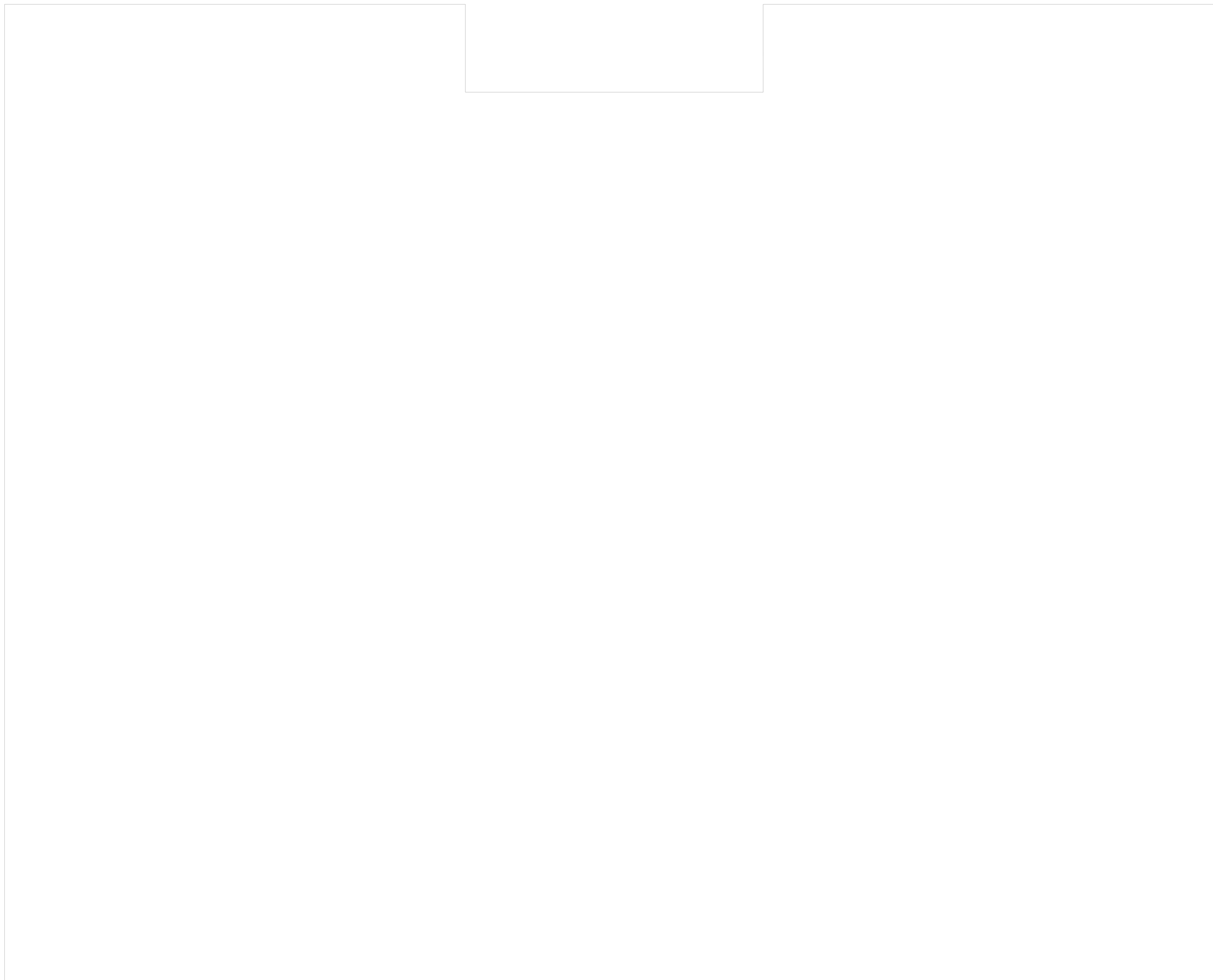


LAYER 10 – BOTTOM COMPONENTS



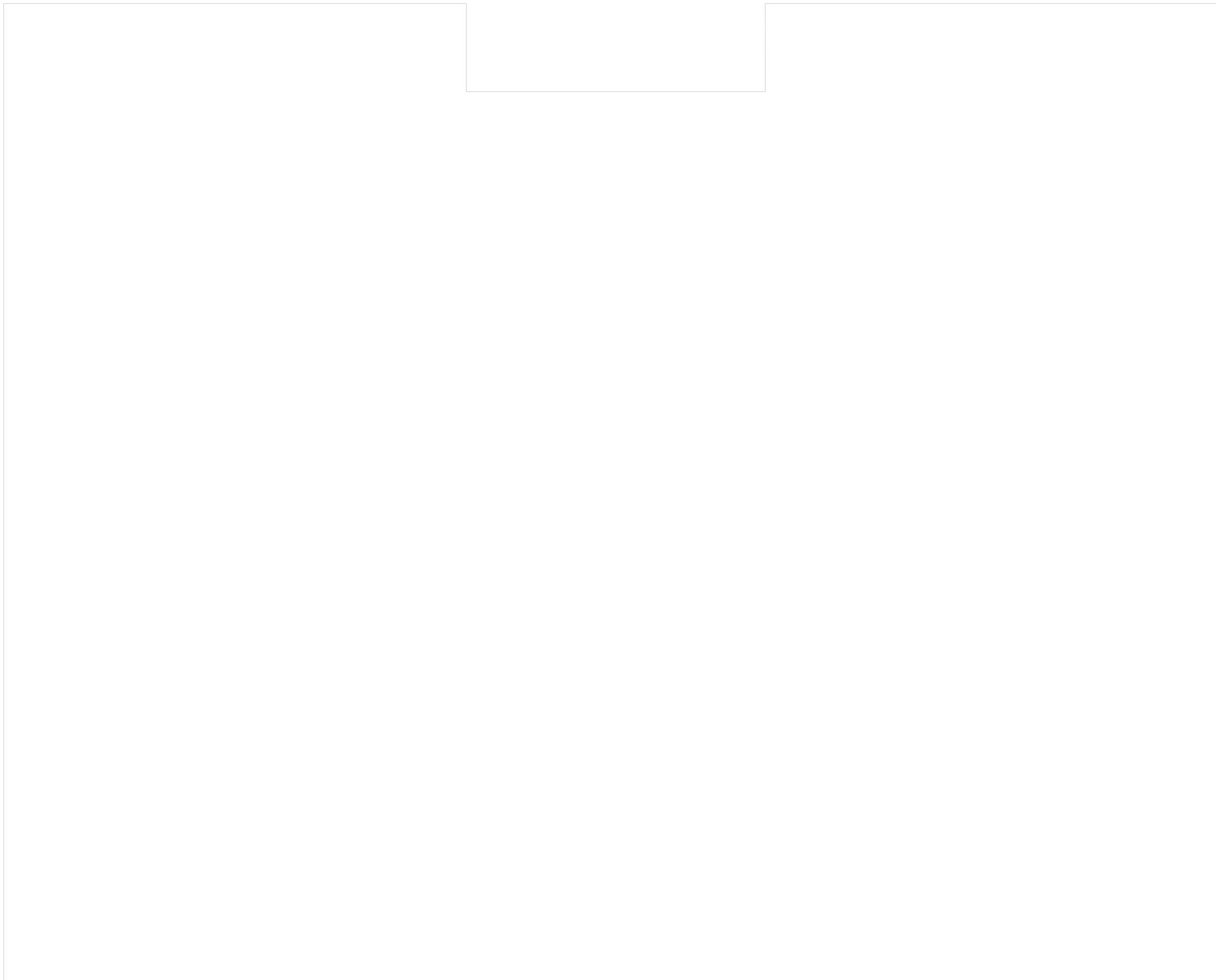
LAYER 1 - TOP COMPONENTS

ASSEMBLY - TOP



LAYER 10 - BOTTOM COMPONENTS

ASSEMBLY - BOTTOM



NES)

AYER)

NES)

NES)

SIDE)

(LAYER 6) 1 OZ. COPPER

(LAYER 7) 1/2 OZ. COPPER

(LAYER 8) 1 OZ. COPPER

(LAYER 9) 1 OZ. COPPER

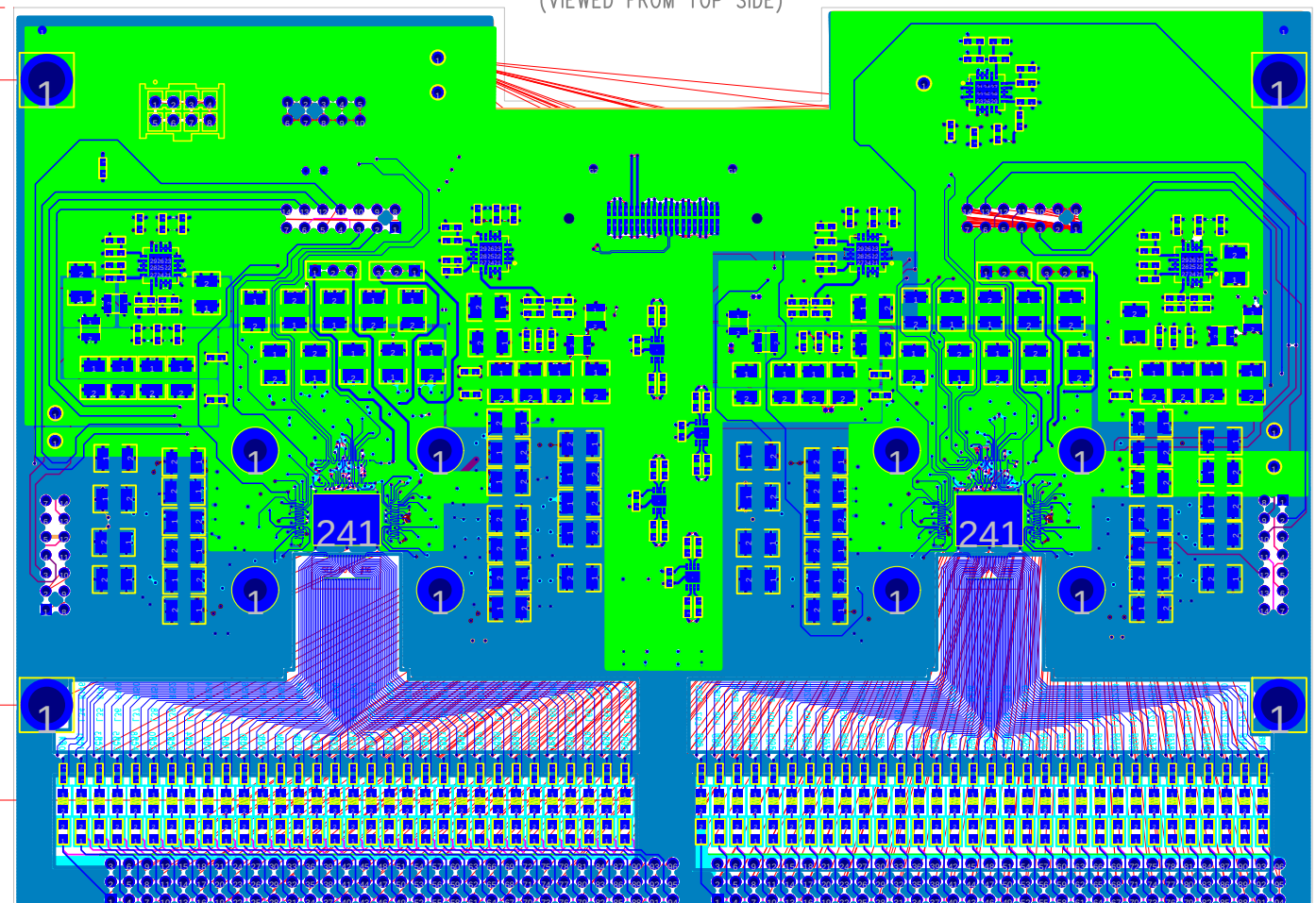
(LAYER 10) 1/2 OZ. STARTING COPPER

SOLDERMASK (BOTTOM SIDE)

SILKSCREEN (BOTTOM SIDE)

LAYER 9 [illegible] FILTERING

(VIEWED FROM TOP SIDE)



11. TOLERANCES:

- BOW AND TWIST SHALL NOT EXCEED 0.5% .
- CONDUCTOR WIDTH AND SPACING SHALL BE WITHIN 0.001 INCH OF GERBE
- FINAL PWB THICKNESS SHALL BE AS SHOWN IN STACK-UP DETAIL.
- SURFACE MOUNT PADS SHALL BE FLAT AND SHALL NOT EXTEND MORE T

12. THROUGH HOLES:

- HOLE SIZES IN DRILL CHART ARE IN MILS AND SPECIFY FINISHED DIAMETE
- LAYER TO LAYER REGISTRATION SHALL BE WITHIN 0.003 INCH.
- HOLE LOCATION SHALL BE WITHIN 0.004 RADIUS OF TRUE POSITION (RT
- ALL HOLES SHALL BE ON FIRST DRILL. SECOND DRILL IS NOT PERMITTE
- TOLERANCE FOR COMPONENT LEAD HOLES IS +/- 0.003 INCH.
- TOLERANCE FOR UNPLATED HOLES IS +0.002 /- 0.002 INCH.
- TOLERANCE FOR VIA HOLES IS +0.002 / -0.010 INCH.

13. CONTROLLED IMPEDANCE : 100 OHMS +/- 10% ON

14. FILL ALL VIAS.

15. CROSS SECTION CUT REQUIRED.

16. PLATE 5-10 MICROINCH OF SOFT GOLD OVER 15