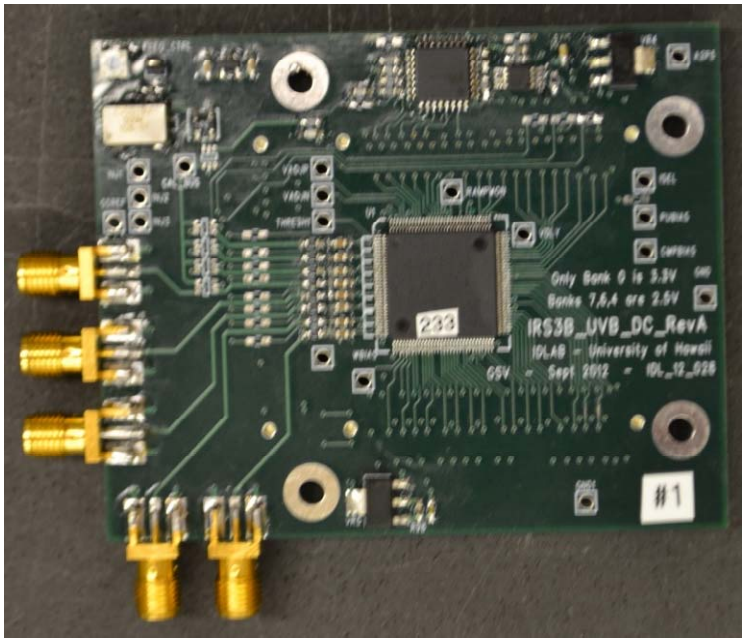
Some thoughts on TARGET7 specs

1. Trigger testing with IRS3B
2. Peremptory thoughts on what can/cannot be done “easily:
3. Apologies… couldn’t prepare further: though can capture and promise a follow-up later

21-FEB-2013 CHEC meeting

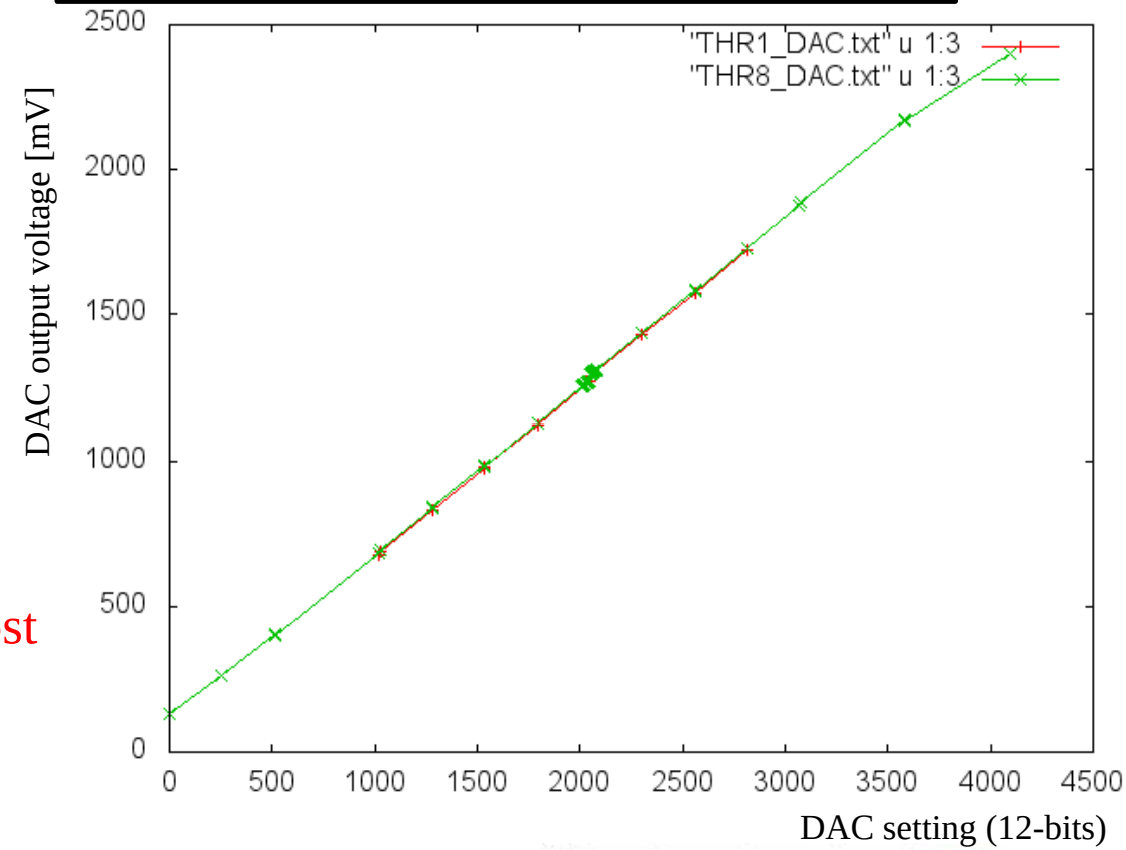
G. Varner

IRS3B Trigger Studies

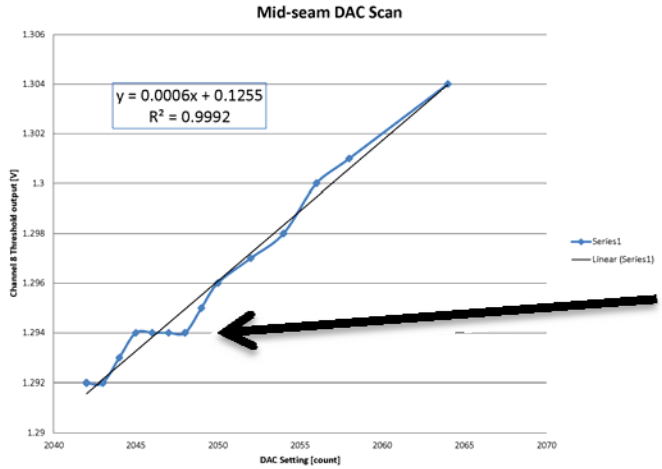


Again, using the “Universal Eval”, as test platform

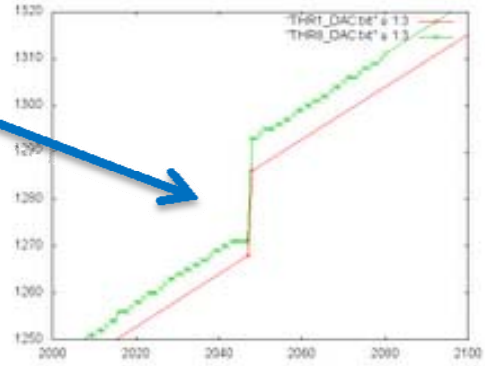
Now have access to a number of DAC channels, can study



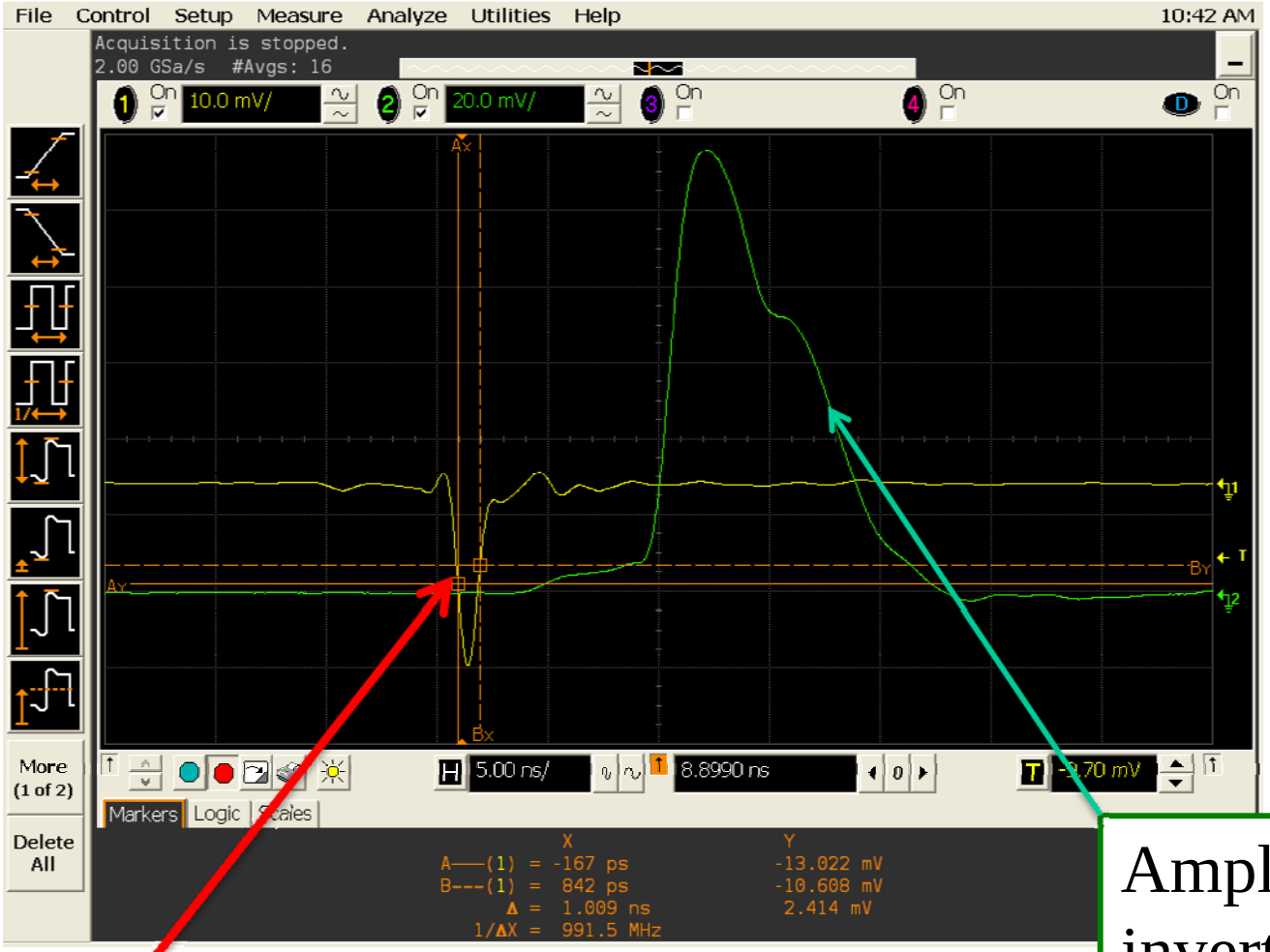
Some Resistance offset in DACs – most prevalent at the “mid seam” of R-2R ladder

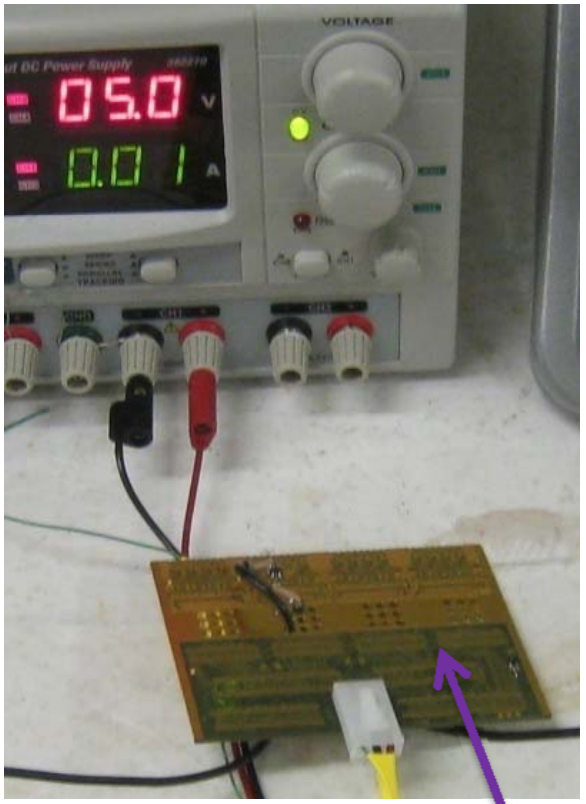


“worst case” **~20mV**, many almost seamless



Including new Pre-amp



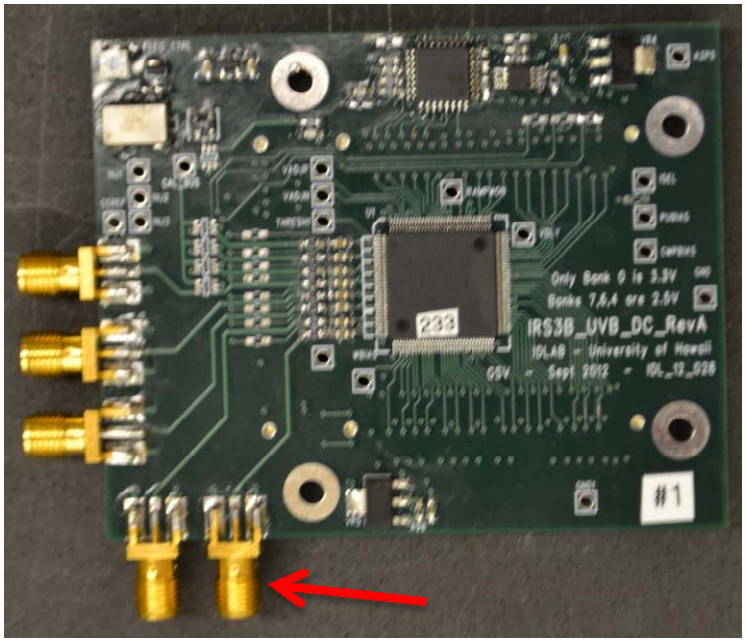


Clip fast signal from Avtech pulser to obtain MCP-PMT like input

Amplified signal using the inverting/shaping circuit prototyped on **Carrier 1 eval** – to be used on future carriers

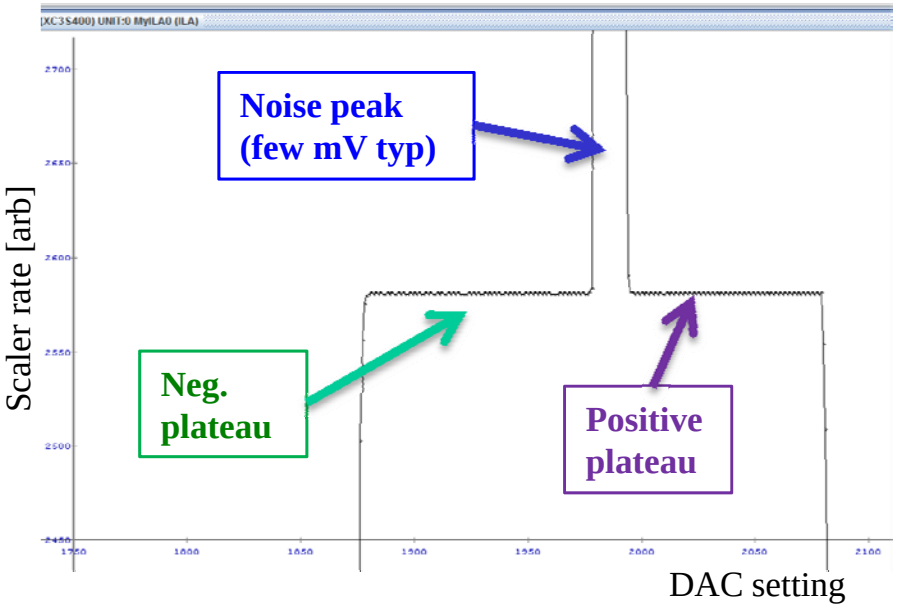
- FWHM ~ 1ns

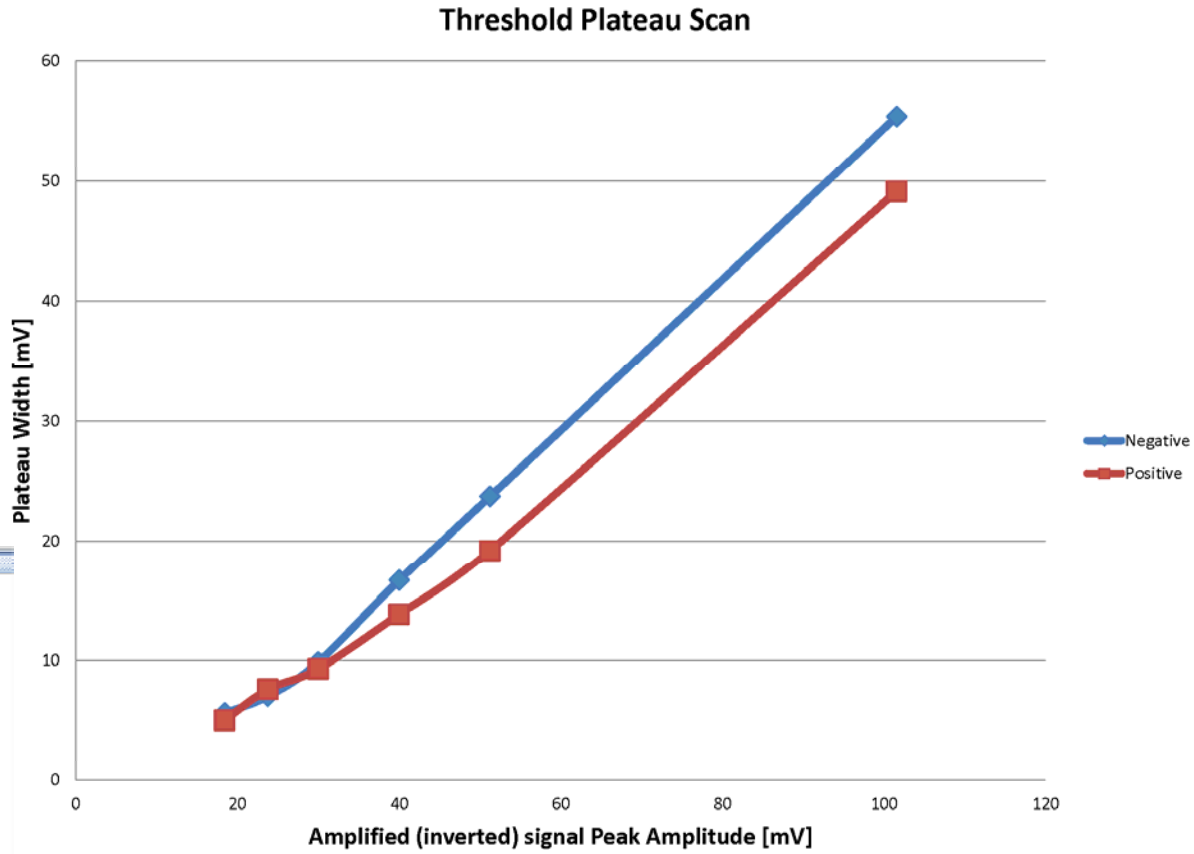
Trigger Threshold Result (1)



Initial test Threshold scan:
Ch8

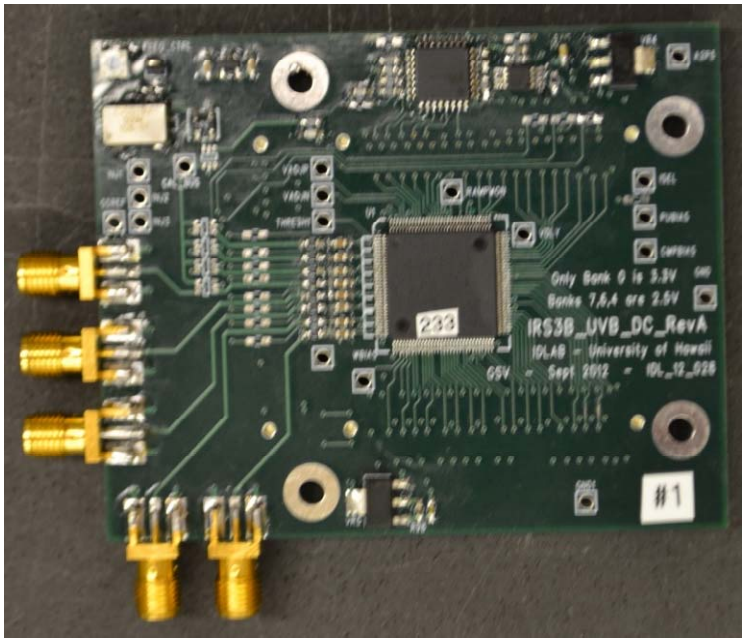
Inject signal and scan count-rate versus threshold



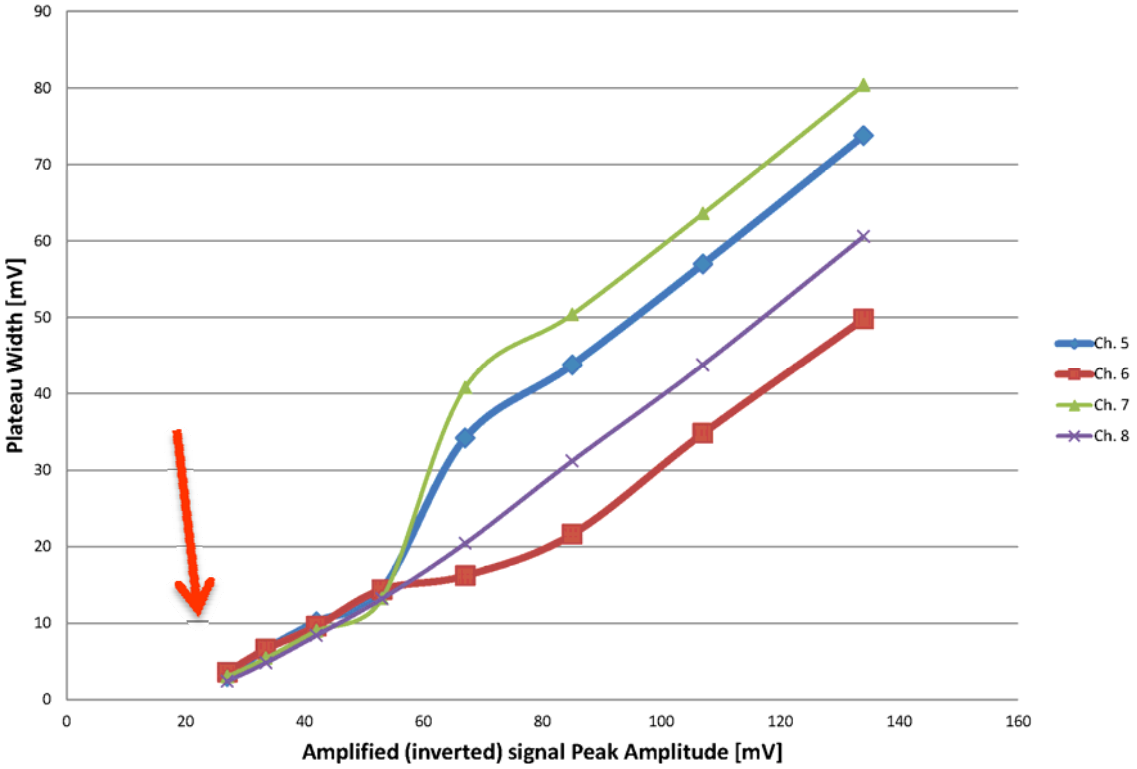


Based upon this – estimated should be able to trigger reliably down to 20-30mV amplified, shaped output peak voltage (~ 5×10^5 gain)

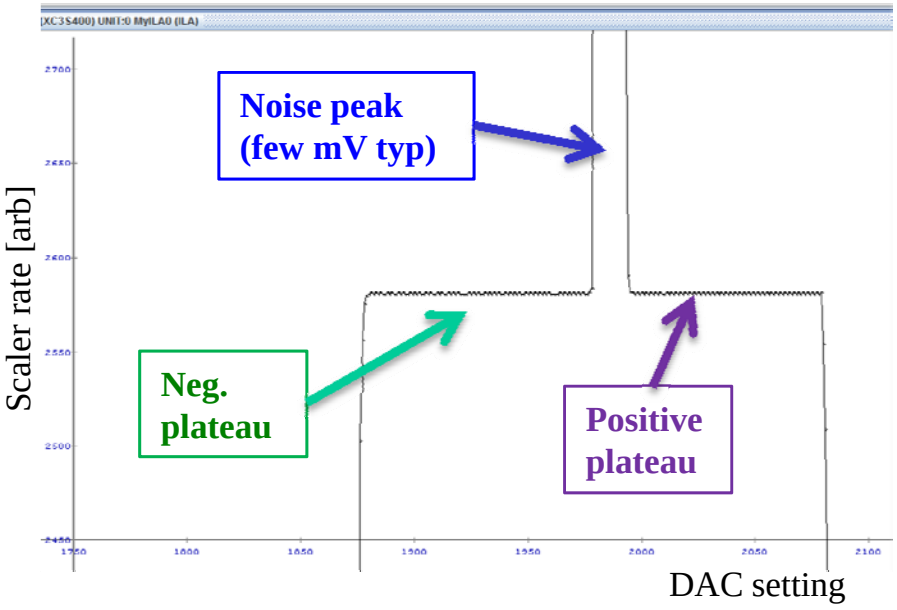
Trigger Plateau Comparison



Comparison of plateaus:
Ch5-8 (positive plateaus)

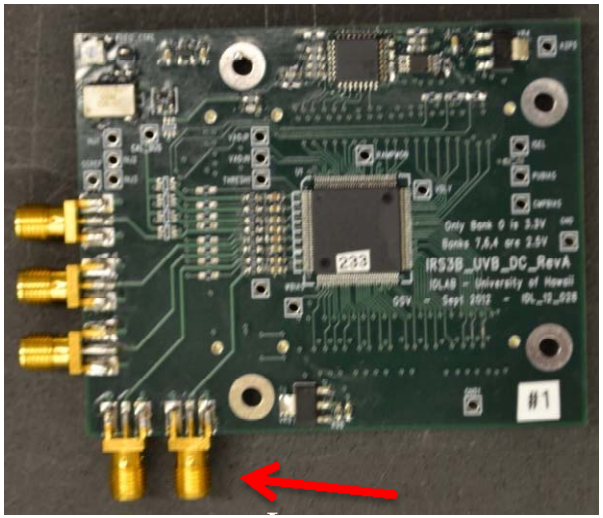


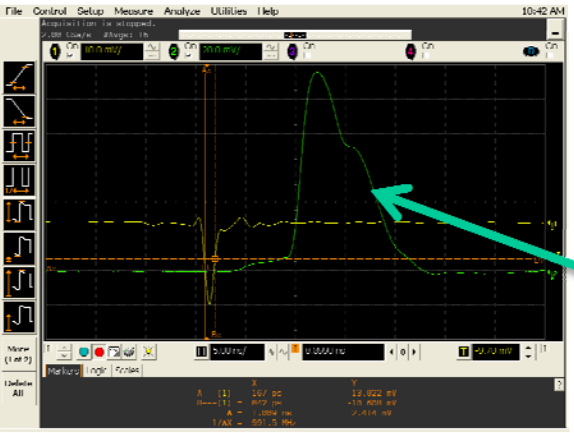
Inject signal and scan count-rate versus threshold

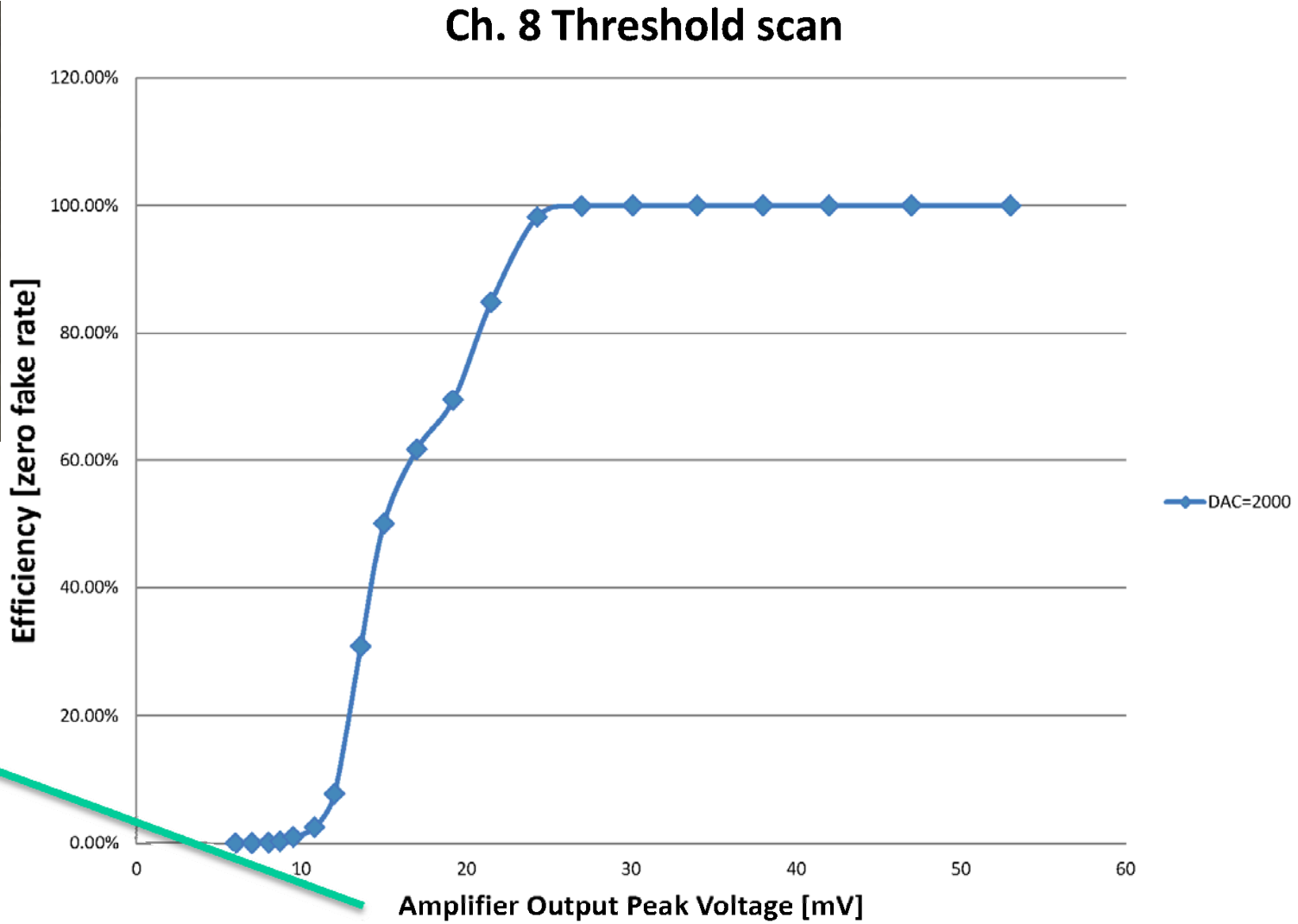


Splitting due to crossing the DAC mid-seam; Arrow indicates the planned operating range

Trigger Threshold Result (2)



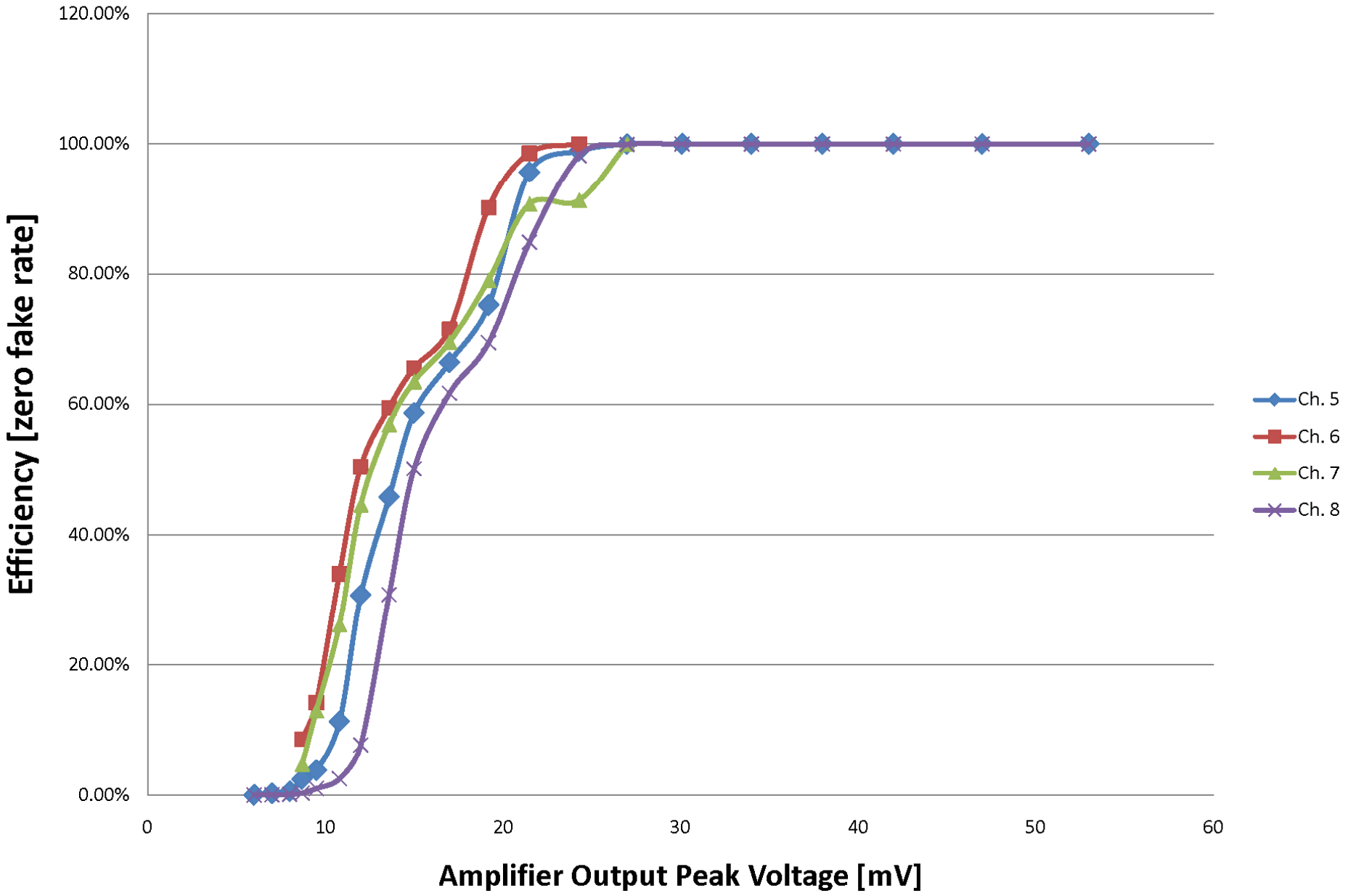




~50% efficiency for 15mV peak pulses (near 100% for 24mV peak). Need to confirm this is shaped output peak voltage range for lower gain (~ 5×10^5 gain) operation

Initial test Threshold scan:
Ch8

Trigger Threshold Comparison



Channel 8 actually worst of those checked, more statistics needed.

Initial thoughts (1)

From Jim H.:

** The basic operational plan for TARGET in CHEC:
- Baseline 1 pe amplitude post-pre-amp was 1.2 mV peak to give saturation at ~800 pe in a 1 V TARGET range and signal/noise ~2 in ~5 (~independent) samples. This would require triggering at ~12 mV on the 4-channel sum to meet goal performance.

Already fairly close – issue is gain-bandwidth in the analog sum

- Revised plan: 1 pe -> 2 mV peak into ~1.3 V TARGET range -> ~20 mV trigger (increased TARGET range helps with everything from our perspective - but would probably require >5V delivered to the pre-amp.)

Don’t understand, let’s discuss…

Initial thoughts (2)

From Jim H.:

** TARGET-7 wish-list (in priority order):

-- trigger possibility at 15-20 mV on the 4-pixel sum - OR - a 16-pixel sum (ideally with clipping pre-sum)

As shown earlier, trigger itself can work on amplitudes of this size – the issues are upon summed signals, clipping

-- somewhat larger input range + (electronic noise on readout channel kept down to ~0.5 mV)

The input range is set by the power rails of the process chosen. Noise is ideally set by the ASIC, though from extensive experience, in "real world systems", with FPGAs and loads of single-ended, asynchronous digital lines flapping in the breeze, going well sub-mV is difficult/impossible (bumping up so that this board-level noise is limit can work).

-- a few bit gain adjustment (factor 1-3 adjustment) ideally for both trigger and for digitised waveform.

Trim DAC adjusts on trigger parameters is viable. Not likely for the sampling itself.

Initial thoughts (3)

From Jim H.:
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and things we could live with:
-- lower bandwidth (I believe that this is also the case for SCTs --- by the way what is the status of the SCT pre-amplifier design Jim?)

Bandwidth, sampling rate, or temporal resolution. This statement needs refinement.

-- smaller range of digitisation speeds (0.5-1 GS/s as nominal)

The way these samplers achieve their sampling rates has limited agility. Multi-ranging is often the only way to ensure versus process parameter spread and uncertainty.

-- a bit more deadtime

??? Please explain/quantify?

Initial thoughts (4)

From Jim B.:

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1) Improve rise/fall time/ drivers at the trigger outputs to allow trigger output pulses with a minimum width of 4nsec (programmable with some resolution) - This is my only really high priority suggestion!

Achieving faster leading edges on such single-ended output signals is in direct conflict with the noise "desirements" stated earlier. Already the output drivers significantly stress the analog regime of the design. The obvious thing to do would be to go to balanced (e.g. LVDS) outputs for the trigger signals. However that would require more output pins (and there is a desire not to significantly alter the TARGET5 pinout(?))

2) Decrease noise allowing lower threshold triggering (see Jim's notes). Perhaps explore ways of canceling noise with better isolation of comparators, or proximity cancelation with differential signals.

On an ASIC, which has no proper ground planes for the active elements, this is very difficult to realize. Not impossible, but conflicting goals come into play.

3) Add a programmable offset as well as threshold to the trigger (I don't think this is there, let me know if I am wrong)

Completely wrong. Offsets and thresholds are already 12-bit DAC adjustable (modulo comment regarding R-2R and basic R uniformity). However it is not a panacea, for reasons I can explain.

Initial thoughts (5)

From Jim B.:

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4) It might be good to consider additional methods to suppress afterpulsing and cross-talk (in SiPMs), I don't have all of the answers on this but it might be good to ask David Williams and Nepomuk about there ideas for this. Jim's suggestion about a hit sum, with clipping might be a good way to go. Perhaps this information could be used to "qualify" the baseline analog-sum-of-4 trigger. Again, I hope for additional wisdom from others who have done simulations!

Without analog level encoding of some form, “thresholding” is very difficult/expensive to do at full signal bandwidth in real time.

As usual, there may be alternative methods to skin this cat. However, in the truly analog regime, “clipping” at a fixed amplitude offset is not at all trivial (CF: the diode is NOWHERE near a threshold device – merely exponential dependence, which is far ideal in many circumstances)

Initial thoughts (6)

From Justin, Leonid and myself (Stefan):

- The AC noise: is there a way to improve the timing in the next version so that the noise might be lower?

At the risk of being pedantic: let's be clear, this is not "noise". All evidence points to this being a synchronization problem with respect to sample transfer/update. In layman's terms "a timing problem".

Leonid suggested that this is what had been done in IRS3b.

Yes, it is well-worth considering the fine timing adjust that can be done inside the ASIC. This both allows for fine timing adjusts, without needing endless, tedious (and lengthy) firmware recompilation cycles, as allowing for scans that can provide optimized parameters for each ASIC controlled from a common FPGA, in a way that is difficult, if not impossible.

-The issue with the serial output that Leonid described in his earlier message

This issue is raised earlier. If I can get the rise/fall time down to 1ns, but this means 5mV of noise injected into the front-end, is that progress? LVDS outputs are clearly the best alternative, though we'll need to consider what to trade off for the bonding pads to provide.

- The sample 31 problem.

It will be interesting to compare TARGET6. IRS3B has no clear dependence on last sample, but TARGET6 is closer (due back March 3rd)