

Design and Performance of the TeV Array with GSa/s sampling and Experimental Trigger (TARGET) ASIC

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Abstract

Next generation detector proposals for TeV γ astronomy envision arrays of order 100 telescopes each having 100×100 photo-sensor image planes. To be affordable, instrumentation of these mega-channels of sensor require event recording technologies that are highly integrated. We present a first-generation device targeted to this application. This 16-channel ASIC has adjustable input termination, 4k sample depth per channel, prototype self-trigger functionality, and tight window-selected readout. Results on sampling rate, power, dynamic range, current-mode gain and cross-talk are reported. While TARGET is specific to this application, its basic performance is generally useful for a number of applications, as will be presented.

Key words: TeV γ astronomy, CMOS, low-power GSa/s waveform sampling

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1. Background

AGIS, a next-generation atmospheric Cherenkov telescope array, aims to achieve 10 times better sensitivity level of the current Cherenkov telescopes for gamma-ray observations in the energy band of 40 GeV to 200 TeV. Achieving this level of performance will require on the order of 50 telescopes with perhaps as many as 1M total electronics channels. Producing this affordably will require individual components with lower cost and higher reliability than are used in the current generation of telescopes. We are exploring several design

concepts to reduce the cost of camera electronics while improving their performance. Systems based on multi-channel waveform sampling ASIC are leading candidates for such low cost electronics system. We have developed TARGET (TeV Array with GSa/s sampling and Experimental Trigger) ASIC optimized for the AGIS requirements.

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The ASIC design presented in this paper is the natural evolution of a series of ASICs that have been developed for radio neutrino detection [1,2], precision timing recording [3] photodetector, and ...

To meet the challenges of a next generation, much larger collection area telescope array for TeV γ -ray astronomy,

From scientific requirements and budget constraints, specifications of camera electronics can be summarized as the following:

- ADC sampling time: $> 1\text{Gsps}$,
- Readout time: $< 30\mu\text{s}$,
- Trigger latency tolerance: $> 2\mu\text{s}$,
- Dynamic range: > 8 bits
- Target cost: \$15 per pixel.

2. Architectural Details

The Photodetector Read Out version 1 (PRO1) ASIC was developed to evaluate the use of waveform sampling in conjunction with edge determination and

go back and look at original proposal for PROMPT in terms of description of ASIC and its intended purposes.

Table 1

Design specifications of the TARGET ASIC.

<i>Parameter</i>	<i>Value</i>	<i>Unit</i>
Storage samples	4096	per channel
Number channels	16	per TARGET
Dynamic range	~ 9	bits
Sample window	32	samples
Nominal sampling	~ 1	GSa/s
Readout time	$16\mu\text{s}$	all window samples
Event rate	50	kHz sustained

The primary components of this circuit are shown in the

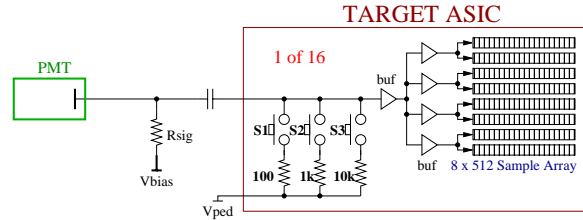


Fig. 1. A block diagram of the TARGET readout ASIC, with the input coupling and termination for a single channel shown.

3. Readout Test System

Evaluation of the TARGET ASIC has been performed using the test circuit board configuration shown in Fig. 2. At left is a test board that permits the insertion of high-frequency signals via SMA input connectors. The basic evaluation board consists of a couple of ...

Fig. 2. Photograph of the TARGET evaluation circuit board (right) and RF input test board (left). The 2mm pitch, dual-row connector is designed for direct interconnect to a 64-channel multi-anode photomultiplier.

The three main components on this circuit board are a wire bonded PRO1 chip, an FPGA, and a Universal Serial Bus (USB) interface. The external communication interface is via USB 2.0. A USB microcontroller on the circuit board interprets the USB 2.0 protocol. The USB microcontroller used was a Cypress CY7C68013-56PVC. The USB microcontroller controls the data being sent and received from the FPGA to a computer interface. The FPGA controls the digital logic and timing for the PRO1 readout. The FPGA used was a Xilinx XC3S200. The internal FPGA RAM buffers the data while the data is being dumped into the USB data stream. Basic software was developed to send commands FPGA and record the PRO1 data with the USB 2.0 interface.

4. Test Results

Employing the test system described in the previous section and its variants, a number of the basic performance parameters of the TARGET have been evaluated.

4.1. Sampling speed

This is the result for TARGET??

Determination of the sampling speed is made by measuring the time interval between insertion of the timing strobe and appearance of the output pulse from the last cell of the row, minus pad buffer delays. The sampling speed is calculated by taking the number of cells in a row and dividing it by the propagation time for a given control voltage setting. A plot of the sampling speed versus control voltage (ROVDD) is shown in Fig. 3, where it is seen that sampling rates from below 0.3 GSa/s to above 3.5 GSa/s are possible.

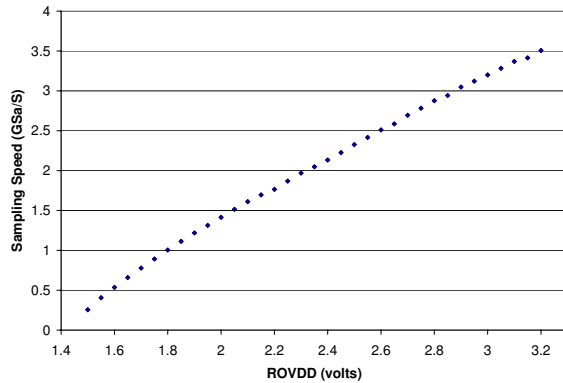


Fig. 3. Sampling rate as a function of the ROVDD control voltage, where extended operation (< 2.5V) is possible.

4.2. Linearity Performance

While a linearity correction can be applied, a good first cut at the ... is seen in Fig. 4

Fig. 4. Determined output code as a function of DC input voltage.

Need to show residual for TARGET, this is from PRO1

4.3. Triggering Performance

The TARGET triggering performance was evaluated using the test setup ...

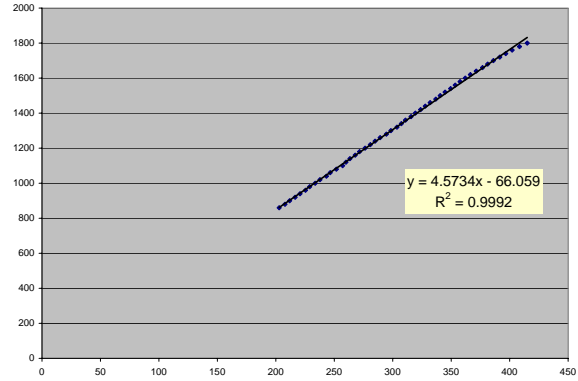


Fig. 5. Determined output code as a function of DC input voltage.

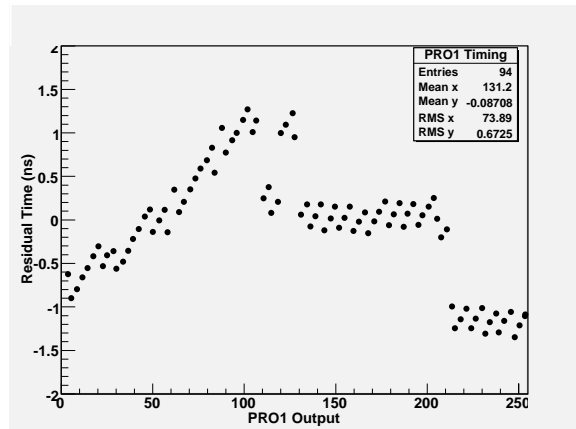


Fig. 6. Plot of the residual data structure from subtracting the linear fit to the data points.

Results of measurements are compared with SPICE simulation in Fig. 7.

shown in Fig. 8. This TDC performance, after applying the calibration corrections, is fairly close to the ideal binary interpolation $\frac{1}{\sqrt{12}}$ limit, as reported previously [??? - insert refer here].

4.4. Analog Bandwidth and Crosstalk

An important aspect of the performance of such a device is to know

where the results are shown for 100Ω, 1kΩ and 10kΩ in Figs. 8, 9 and 10, respectively.

Actually need to measure 10k ohm value

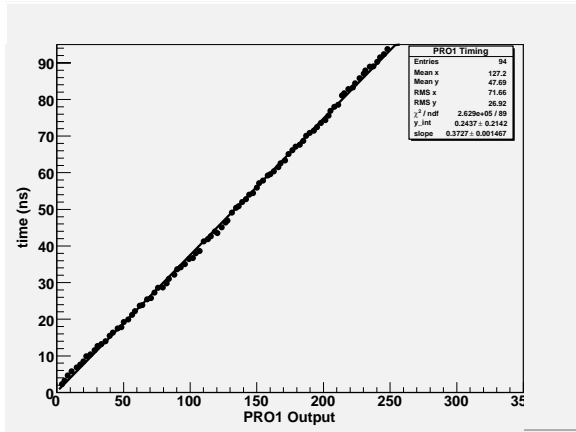


Fig. 7. A comparison of simulated and other data....

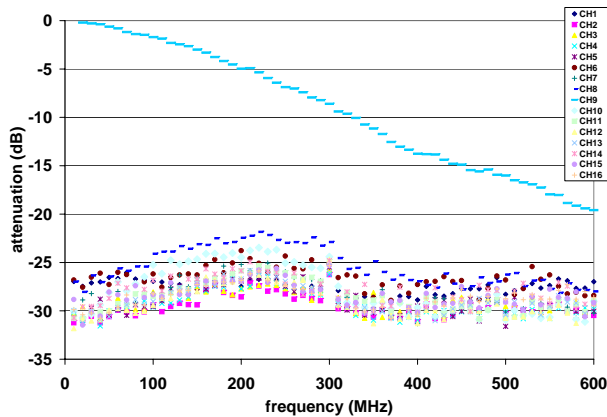


Fig. 8. Measured amplitude and crosstalk with signal injected into Channel 9 and 100Ω input termination.

5. Other Applications

A chip capable of continuous digitization ...

5.1. Drift Chamber Readout

5.2. K_L and Muon System

5.3. Focal Plane Arrays

6. Future Directions

The basic performance of the TARGET to the TeV γ application has been demonstrated. Toward a larger deployment

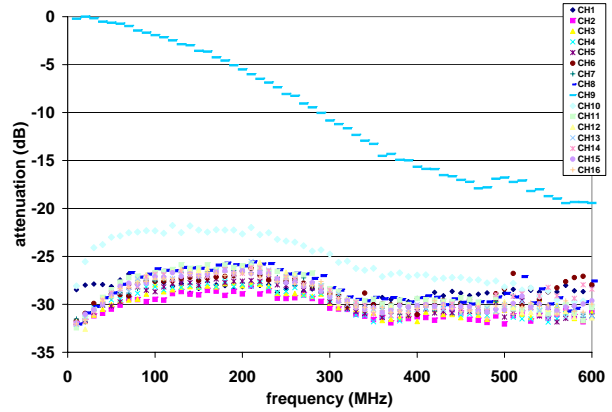


Fig. 9. Measured amplitude and crosstalk with signal injected into Channel 9 and 1kΩ input termination.

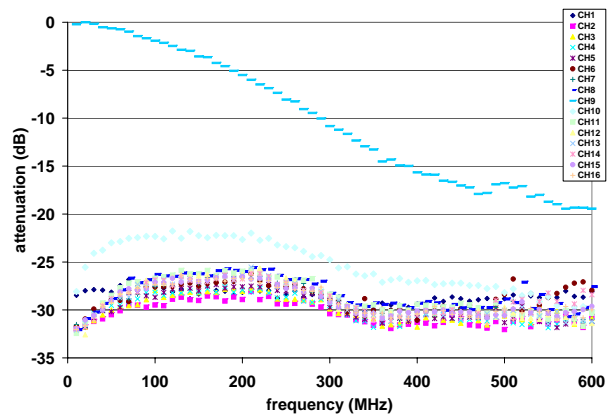


Fig. 10. Measured amplitude and crosstalk with signal injected into Channel 9 and 10kΩ input termination.

- Internal threshold DACs
- TIA amplifier
- Discriminator output DACs

7. Summary

We have described the architecture of an ASIC tailored to the low-cost, high-performance acquisition of the photonic signal from atmospheric showers. A 16-channel device designated TARGET has been evaluated and meets the requirements for such an application.

8. Acknowledgements

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