University of Hawai'i Manoa
Instrumentation Development Laboratory

Version 0.9 February 2009

TARGET1

16-channel, GSPS Transient Waveform Recorder with Self-Triggering and Fast, Selective Window Readout

General Description

The first-generation TeV Array with GSa/s sampling and Experimental Trigger (TARGET1) ASIC is a 16-channel transient waveform recorder initially designed to monolithically and inexpensively instrument large arrays of photodetectors. However the very general nature of the signal recording, the programmable input termination, the narrow digitization selection window, and fast single conversion make it useful in a number of applications. In order to support large arrays, self-triggering capabilities have been incorporated to permit event-of-interest identification as well as data sparsification.

Intended for detectors needing sampling rates of 1-2 Giga-samples per second (GSPS), triggered readout rates of up to 50kHz are possible, depending upon the resolution and performance of Wilkinson time encoding inside a companion Field Programmable Gate Array. Each channel has 8 rows of 512 storage cells, or 4096 storage samples available.

Features

- → High density (16 channels)
- → Good timing performance
- → 9-10 bits of resolution
- → Fast conversion (<0.5us/32 samples)
- → Random access to groups of 16 samples
- → Flexible operating modes
- → 100Ω, 1k and 10k programmable terminators

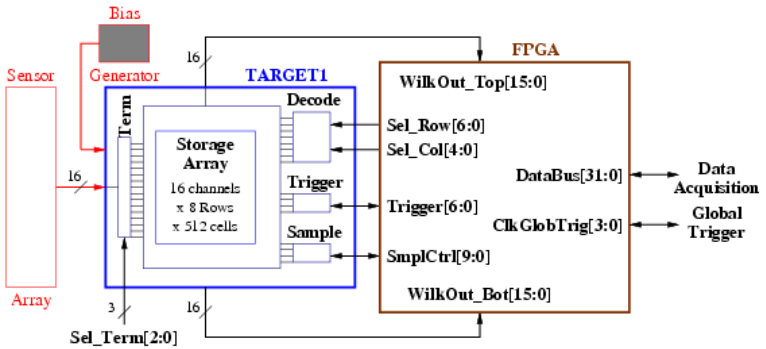
Key Specifications

- → Low power (<10mW/channel)
- → Giga-sample per second recording
- → Selective (windowed) readout
- → 4,096 storage samples/channel

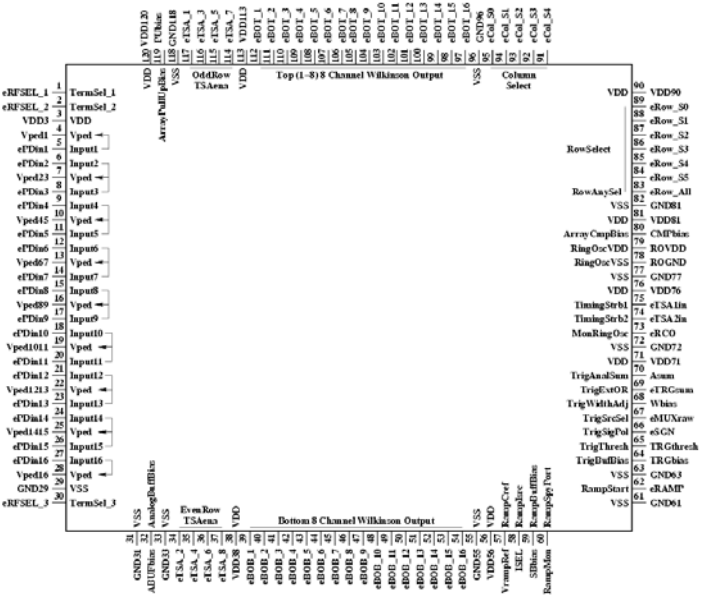
Applications

- ➔ Next generation TeV gamma readout
- ➔ Low-cost, highly integrated systems
- ➔ Collider Detector instrumentation
- ➔ Portable/pocket oscilloscope

Block Diagram



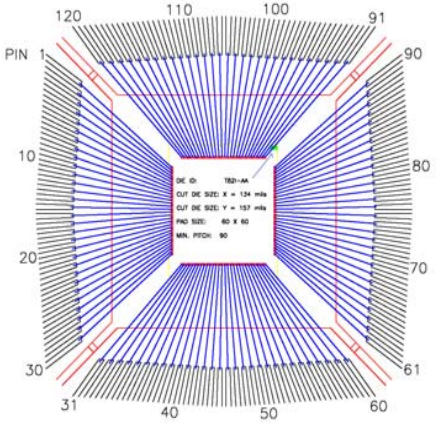
Connection Diagram



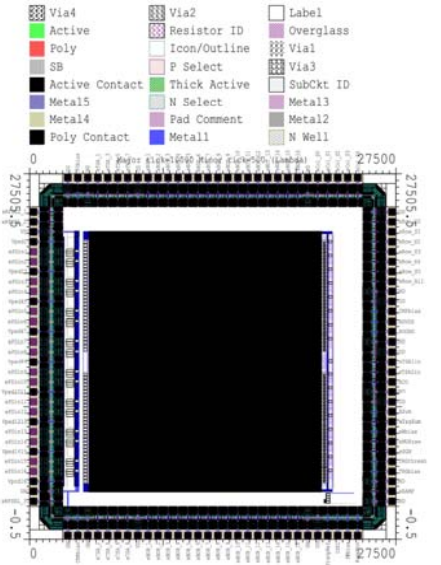
Available Packaging

The currently available TARGET1 devices are available in a standard TQFP-120 package. Different packages or die can be ordered (5months ARO).

Bonding Diagram



Die Overview



Pin-out Functional Listing

A detailed list of pin numbers corresponding to the symbol on the preceding page. Color coding has been used to clarify signal type and group by functionality. Additional comments are provided to indicate relationships, function, or suggested interconnect values. All purple signals correspond to analog signals and are set either by pull-up resistor or voltage regulator, except for VrampRef (optional external capacitor) and Asum (can discriminate to require number triggers active).

= VDD
= GND
= Digital from FPGA
= Digital to FPGA
= Analog/bias value
= Sample speed CTRL V
= Signal input
= Pedestal voltage
= Test point

Pin #	Pin Name	Connection type	Comments
1	eRFSEL_1	Termination Select bit 1	100 Ohm (1=active)
2	eRFSEL_2	Termination Select bit 2	1k Ohm (1=active)
3	VDD3	2.5V power (VDD)	
4	Vped1	Ped voltage ref PDin1	1.3V nom.
5	ePDin1	PhotoDector input 1	term to Vped1
6	ePDin2	PhotoDector input 2	term to Vped23
7	Vped23	Ped voltage ref PDin2, PDin3	
8	ePDin3	PhotoDector input 3	term to Vped23
9	ePDin4	PhotoDector input 4	term to Vped45
10	Vped45	Ped voltage ref PDin4, PDin5	
11	ePDin5	PhotoDector input 5	term to Vped45
12	ePDin6	PhotoDector input 6	term to Vped67
13	Vped67	Ped voltage ref PDin6, PDin7	
14	ePDin7	PhotoDector input 7	term to Vped67
15	ePDin8	PhotoDector input 8	term to Vped89
16	Vped89	Ped voltage ref PDin8, PDin9	
17	ePDin9	PhotoDector input 9	term to Vped89
18	ePDin10	PhotoDector input 10	term to Vped1011
19	Vped1011	Ped voltage ref PDin10, PDin11	
20	ePDin11	PhotoDector input 11	term to Vped1011
21	ePDin12	PhotoDector input 12	term to Vped1213
22	Vped1213	Ped voltage ref PDin12, PDin13	
23	ePDin13	PhotoDector input 13	term to Vped1213
24	ePDin14	PhotoDector input 14	term to Vped1415
25	Vped1415	Ped voltage ref PDin14, PDin15	
26	ePDin15	PhotoDector input 15	term to Vped1415
27	ePDin16	PhotoDector input 16	term to Vped16
28	Vped16	Ped voltage ref PDin16	
29	GND29	0V power (GND = VSS)	
30	eRFSEL_3	Termination Select bit 3	10k Ohm (1=active)
31	GND31	0V power (GND = VSS)	
32	ABUFbias	Analog input buffer bias	50k Ohm pull-up
33	GND33	0V power (GND = VSS)	
34	eTSA_2	Sample Timing Sel Row 2	enable for TSA2in
35	eTSA_4	Sample Timing Sel Row 4	enable for TSA2in
36	eTSA_6	Sample Timing Sel Row 6	enable for TSA2in
37	eTSA_8	Sample Timing Sel Row 8	enable for TSA2in
38	VDD38	2.5V power (VDD)	
39	eBOB_1	Wilkinson Output Bottom #1	of sel 16, col = 1
40	eBOB_2	Wilkinson Output Bottom #2	of sel 16, col = 2
41	eBOB_3	Wilkinson Output Bottom #3	of sel 16, col = 3
42	eBOB_4	Wilkinson Output Bottom #4	of sel 16, col = 4
43	eBOB_5	Wilkinson Output Bottom #5	of sel 16, col = 5
44	eBOB_6	Wilkinson Output Bottom #6	of sel 16, col = 6
45	eBOB_7	Wilkinson Output Bottom #7	of sel 16, col = 7
46	eBOB_8	Wilkinson Output Bottom #8	of sel 16, col = 8
47	eBOB_9	Wilkinson Output Bottom #9	of sel 16, col = 9
48	eBOB_10	Wilkinson Output Bottom #10	of sel 16, col = 10
49	eBOB_11	Wilkinson Output Bottom #11	of sel 16, col = 11
50	eBOB_12	Wilkinson Output Bottom #12	of sel 16, col = 12
51	eBOB_13	Wilkinson Output Bottom #13	of sel 16, col = 13
52	eBOB_14	Wilkinson Output Bottom #14	of sel 16, col = 14
53	eBOB_15	Wilkinson Output Bottom #15	of sel 16, col = 15
54	eBOB_16	Wilkinson Output Bottom #16	of sel 16, col = 16
55	GND55	0V power (GND = VSS)	
56	VDD56	2.5V power (VDD)	
57	VrampRef	Capacitance node for Vramp	100pF (n.c.)
58	ISEL	Vramp Current bias	68k pull-down
59	SBbias	Super buffer bias	50k pull-up
60	RampMon	monitor Vramp signal	to test point

Pin #	Pin Name	Connection type	Comments
61	GND61	0V power (GND = VSS)	
62	eRAMP	Initiate Vramp	PRO or Raw CMP
63	GND63	0V power (GND = VSS)	
64	TRGbias	bias current for TRG comp.	20k pull-up
65	TRGthresh	threshold for TRG comp.	about 1.3V nom.
66	eSGN	TRG signal polarity	XOR w/comp out
67	eMUXraw	Multiplex of 1-shot or raw out	1= raw comp out
68	Wbias	bias for 1-shot Width adj.	voltage input
69	eTRGsum	Digital sum of all comp. outputs	OR of 16
70	Asum	Analog sum of all comp. outputs	I ~ N(on)
71	VDD71	2.5V power (VDD)	
72	GND72	0V power (GND = VSS)	
73	eRCO	Ripple Carry Out (sample rate)	monitor
74	eTSA2in	sample Timing Strobe #2	even row sample
75	eTSA1in	sample Timing Strobe #1	odd row sample
76	VDD76	2.5V power (VDD)	
77	GND77	0V power (GND = VSS)	
78	ROGND	Ripple Oscillator GND	0V nom.
79	ROVDD	Ripple Oscillator VDD	2.5V (@ ~2GSa/s)
80	CMPbias	Wilkinson Comparator bias	50k pull-up
81	VDD81	2.5V power (VDD)	
82	GND82	0V power (GND = VSS)	
83	eRow_All	Enable a Row for Readout	0 = all output off
84	eRow_S5	Row Select bit 5	
85	eRow_S4	Row Select bit 4	
86	eRow_S3	Row Select bit 3	64 indep rows
87	eRow_S2	Row Select bit 2	(8x per chan,
88	eRow_S1	Row Select bit 1	top + bottom)
89	eRow_S0	Row Select bit 0	
90	VDD81	2.5V power (VDD)	
91	Col_S4	Column Select bit 4	
92	Col_S3	Column Select bit 3	512 samples/16
93	Col_S2	Column Select bit 2	= 32 groups
94	Col_S1	Column Select bit 1	(5-bit addressing)
95	Col_S0	Column Select bit 0	
96	GND96	0V power (GND = VSS)	
97	eBOT_16	Wilkinson Output Top #16	
98	eBOT_15	Wilkinson Output Top #15	
99	eBOT_14	Wilkinson Output Top #14	
100	eBOT_13	Wilkinson Output Top #13	
101	eBOT_12	Wilkinson Output Top #12	
102	eBOT_11	Wilkinson Output Top #11	
103	eBOT_10	Wilkinson Output Top #10	
104	eBOT_9	Wilkinson Output Top #9	
105	eBOT_8	Wilkinson Output Top #8	
106	eBOT_7	Wilkinson Output Top #7	
107	eBOT_6	Wilkinson Output Top #6	
108	eBOT_5	Wilkinson Output Top #5	
109	eBOT_4	Wilkinson Output Top #4	
110	eBOT_3	Wilkinson Output Top #3	
111	eBOT_2	Wilkinson Output Top #2	
112	eBOT_1	Wilkinson Output Top #1	
113	VDD113	2.5V power (VDD)	
114	eTSA_7	Sample Timing Sel Row 7	enable for TSA1in
115	eTSA_5	Sample Timing Sel Row 5	enable for TSA1in
116	eTSA_3	Sample Timing Sel Row 3	enable for TSA1in
117	eTSA_1	Sample Timing Sel Row 1	enable for TSA1in
118	GND118	0V power (GND = VSS)	
119	PUbias	Pull Up bias for readout column	50k pull-down
120	VDD120	2.5V power (VDD)	

Absolute Maximum Ratings

Supply Voltage (VDD)	-0.4V to +3.6V
Voltage Input Digital lines	-0.3V to +3.3V
Voltage Input Signal pins[1]	+0.4 to +2.8V
Voltage any output pin	TBD
Input Current (non-power)	TBD
Package Input Current	TBD
Max Junction Temperature	TBD
Thermal Resistance	TBD
Package Dissipation	TBD
+ Many other specs	TBD
Storage temperature[2]	-65C to +150C

Note 1: Minimal input protection diode structure
Note 2: Soldering process must comply with ASAT Technologies Reflow Temperature Profile Specificaitons

Operating Ratings

Operating Temperature	-0.4V to +3.6V
Supply Voltage	-0.3V to +3.3V
Output Signal Levels	+0.4 to +2.8V
TSA strobe jitter	TBD
RCO Duty Cycle	TBD
Analog Input Pins	TBD
Vped	+0.4V to +2.8V

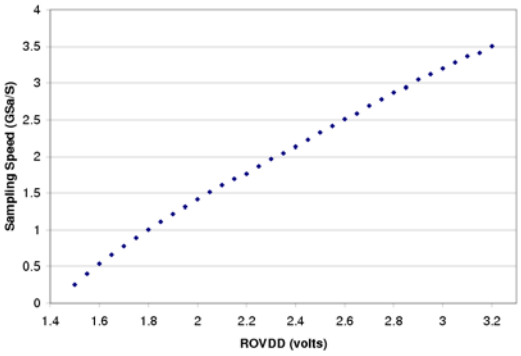
Converter Electrical Characteristics

Stored samples in the TARGET1 are converted into output digital code using a Wilkinson technique, where a ramp converts the analog value into a binary output time. These time intervals, from the beginning of ramp until the count time is latched using a fast Gray code counter, is proportional to the stored analog value. By changing the ISEL (ramp rate) and VrampRef (external capacitor), the conversion ramp time slope can be manipulated. Performance and number of bits of resolution depend upon TDC technique employed inside the FPGA.

Symbol	Parameter	Conditions	Typ.	Limits	Units
INL	Integral Non-linearity	Full scale input	TBD	TBD	Bits (min)
DNL	Differential Non-linearity	Full scale input	TBD	TBD	Bits (min)
Tacq	Conv. Cycle time	32x in parallel	1	0.5	us
ENC	Equivalent Noise	No signal	TBD	TBD	Bits (min)

Sampling Speed Adjustment

The sampling speed of the TARGET is controlled by adjusting the ROGND and ROVDD voltage lines. In general, ROGND is tied to ground, though could also be adjusted to achieve even slower sampling speeds. With ROGND tied to local ground, the sampling speed dependence as a function of applied ROVDD is seen in the Figure at right.

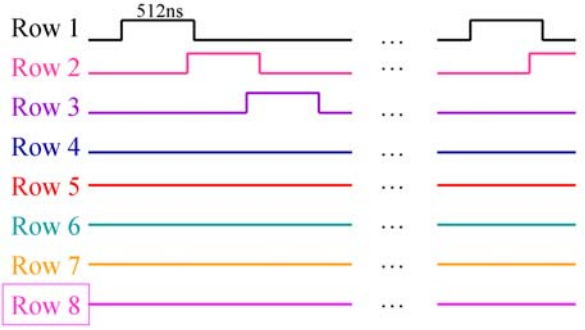


Sampling Speed Stabilization

It is found that to obtain the best performance, excellent bypassing of the ROVDD voltage line is necessary. Without temperature compensation, the sampling speed will vary for a fixed applied voltage. By monitoring the RCO signal, a correction to the ROVDD voltage can be made (via external DAC) to keep the sampling rate frequency locked.

Continuous Sampling

In order to provide seamless sampling, the strobes to each of the rows can be operated sequentially, as shown at the right. The degree of overlap depends upon the ability of the control loop to maintain the timebase stability. For full feedback in firmware, it should be possible to stitch together sampling windows without a seam. Upon receipt of trigger, random access to groups of 16 samples on 2 separate channels is possible. Further sampling of a given row needs to be blocked until all samples of interest have been converted.



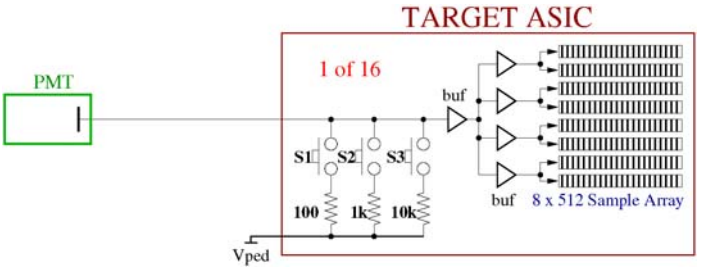
Multi-hit Capability

In order to reduce readout time, it is possible to continue sampling while readout continues, utilizing the rest of the sampling storage rows that are not in the held state. Not all combinations are possible since initiation of the write strobe via TSA1 corresponds to the odd numbered row enables (eTSA_1, eTSA_3, eTSA_5, eTSA_7), while TSA2 corresponds to the even numbered row enables (eTSA_2, eTSA_4, eTSA_6, eTSA_8). To take full advantage of this feature, future variants of the TARGET family will have individual trigger lines for each channel, so that upon a global trigger decision, it will be known which channels need to be read out, and making the multi-hit capability more useful.

Input Coupling

The TARGET input can be operated in either an AC or DC coupled mode. In AC mode, the detector bias is decoupled from the Vped value that sets the input baseline. In DC mode, the sensor must be capable of having a DC offset asserted, corresponding to the nominal termination voltage.

AC-coupled input configuration



DC-coupled input configuration

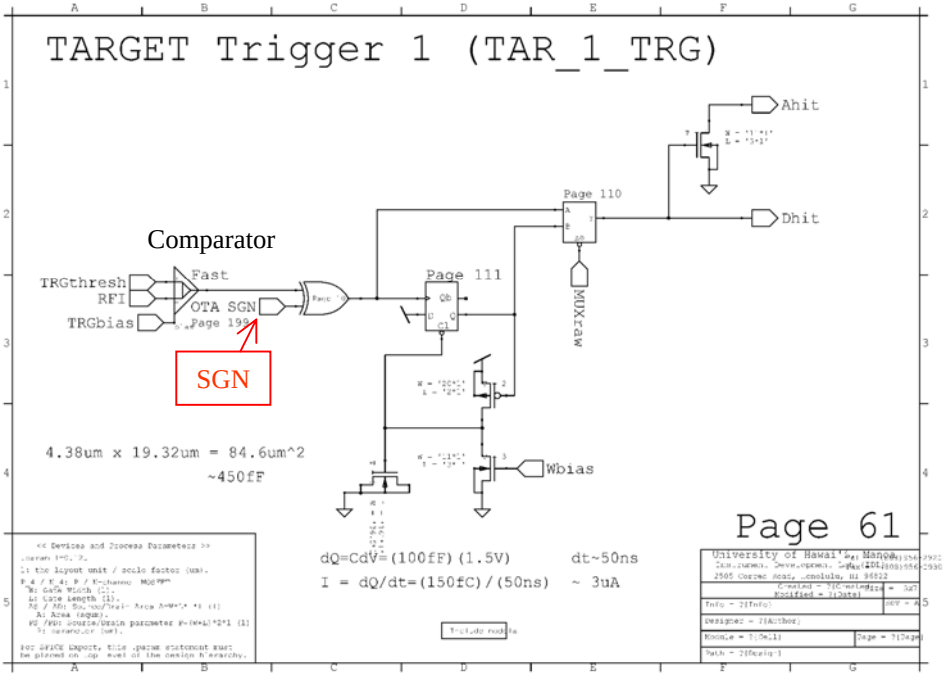
Input Termination

Three input termination resistors permit selection of a number of possible termination values. Each operates independently and the possible configurations are tabulated below.

TermSel_1	TermSel_2	TermSel_3	Termination [Ω]
0	0	0	High (external term)
0	0	1	10k
0	1	0	1k
0	1	1	9.09k
1	0	0	100
1	0	1	99
1	1	0	90.9
1	1	1	90.1

Trigger Functionality

For many applications, it is very useful to be able to provide self-triggering capability. While this could be implemented in by a companion FPGA [**JINST 1:P07001,2006], having to split the input signal and tie up routing and pin resources, in addition to exposing the signal to digital noise, may not be the best solution. A diagram of the trigger schematic for a single channel is below.**



Trigger Related Signals

The input signal in the above schematic is donoted RFI. All pins available external to chip are described below.

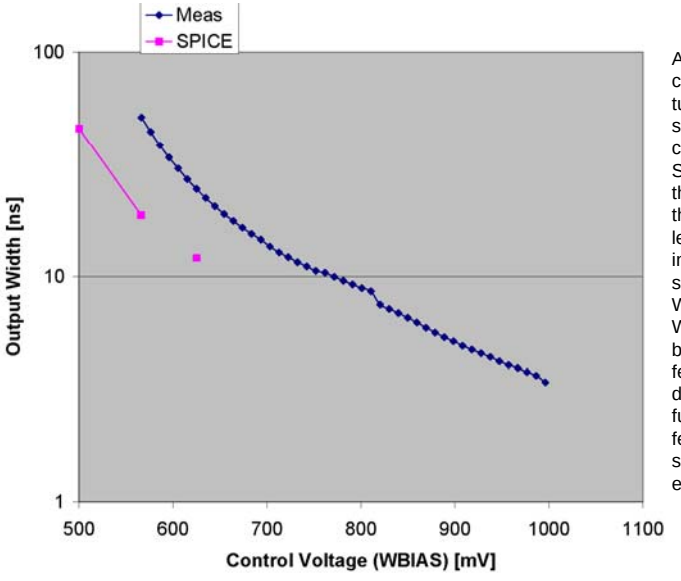
Inputs

TRGthresh	Trigger threshold (global)
TRGbias	Bias current for Comparator
SGN	Select signal polarity (0 = neg. signal; 1 = positive)
Wbias	1-shot width adjust (see next page)
MUXraw	Select either direct comparator or 1-shot output (0= 1-shot)

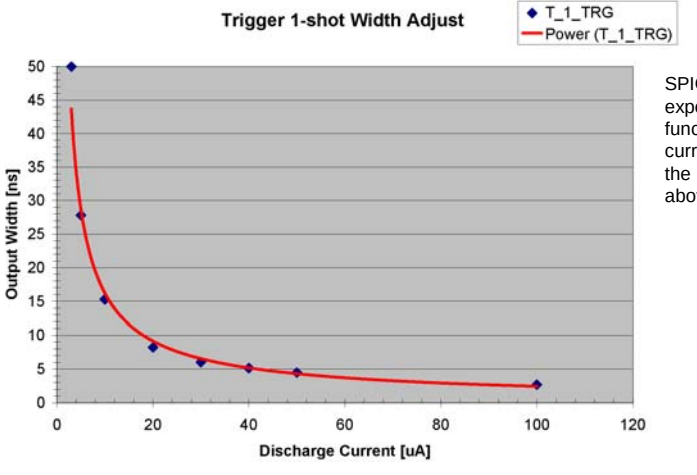
Outputs

Ahit	Analog pull down, with current sink capability proportional to number of trigger channels instantaneously on.
Dhit (eTRGsum)	OR of all trigger signals

Trigger Width Adjust



Adjustment of the WBIAS control voltage can be used to tune the 1-shot output width as seen in the figure at left. A comparison with a couple of SPICE reference points indicate that, apart from an observed threshold shift (in part due to level translation offset of an internal buffer amplifier, the same width dependence on WBIAS setting is observed. While narrow output signals can be reliably set, without feedback, temperature dependence is a concern. In future variants the ability to feedback lock using a reference signal will be an important enhancement.

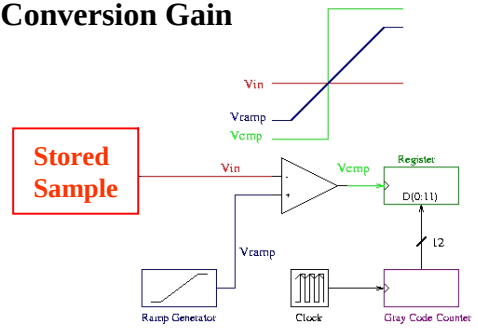


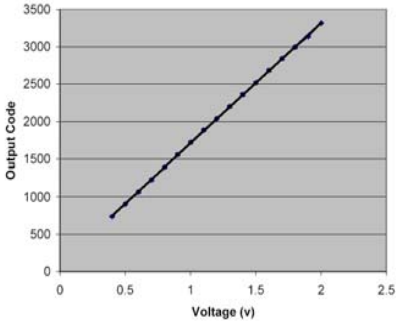
SPICE simulation of the expected output width as a function of the discharge current, which is independent of the threshold offset observed above.

Temperature Dependence

It has been observed that the trigger output width is temperature dependent. Some feedback control is likely to be needed.

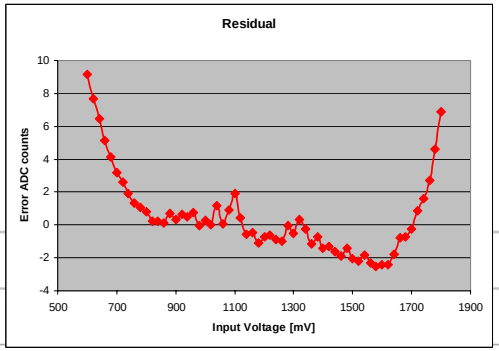
Conversion Gain



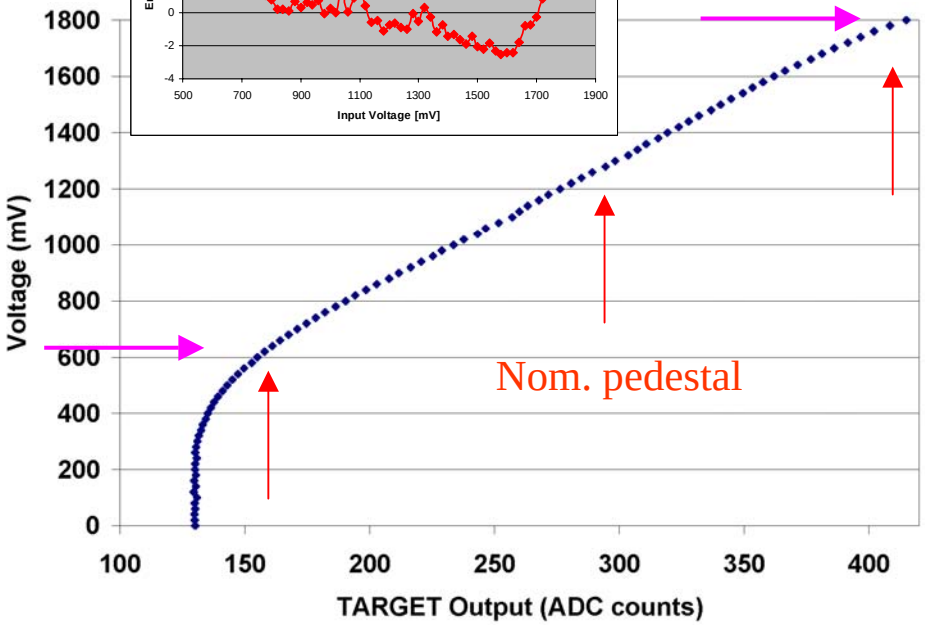


TARGET uses a classical Wilkinson architecture, where the Clock, Gray Code Counter and register are provided in companion FPGA, example above.

Example of ADC Performance

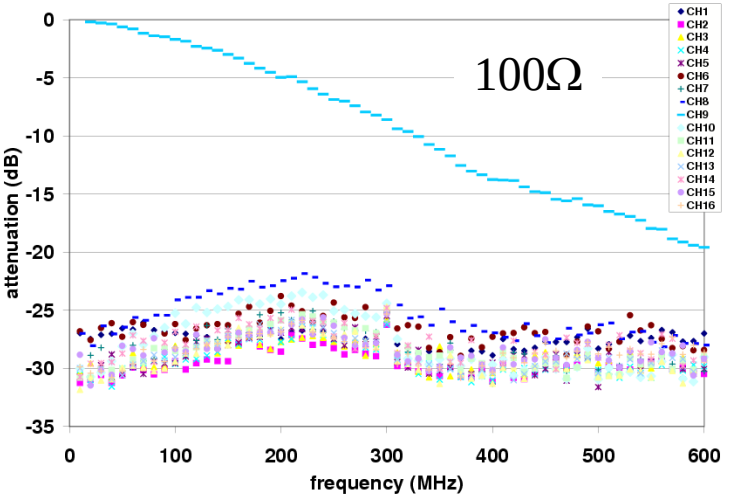


These plot are presented for illustration purposes only. A Look-Up-Table in the firmware/software is used to linearize the response and appropriately treat positive and negative amplitude saturation.

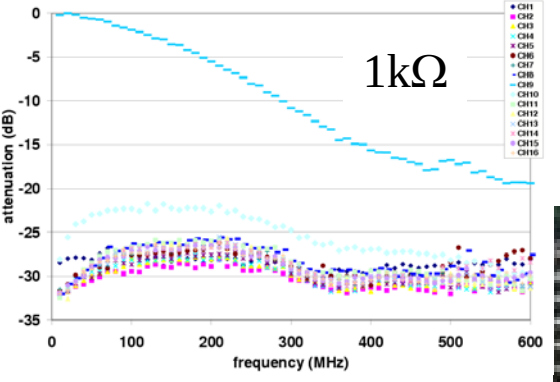


Analog Bandwidth

For many applications, the coupling of signals into the TARGET ASIC will be quite important. The figures below indicate the measured response, as well as observed cross-talk.



In both cases the reference signal is inserted into Channel 9. The –3dB bandwidth is about 150MHz (~1.7ns risetime) for the 100Ω case, and somewhat lower for the 1kΩ termination case. The cross is observed to be approximately largest in the nearest neighbors.



The increased coupling to nearest neighbor in the 1kΩ termination case can perhaps be understood as being related at least in part to direct coupling between the bond-wires, as there is no Vped wire in between.

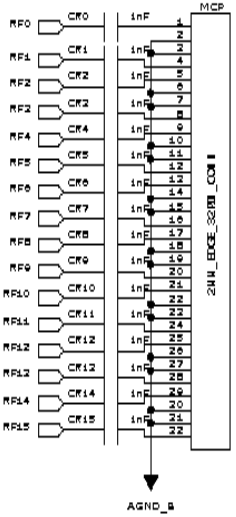
Observed Crosstalk

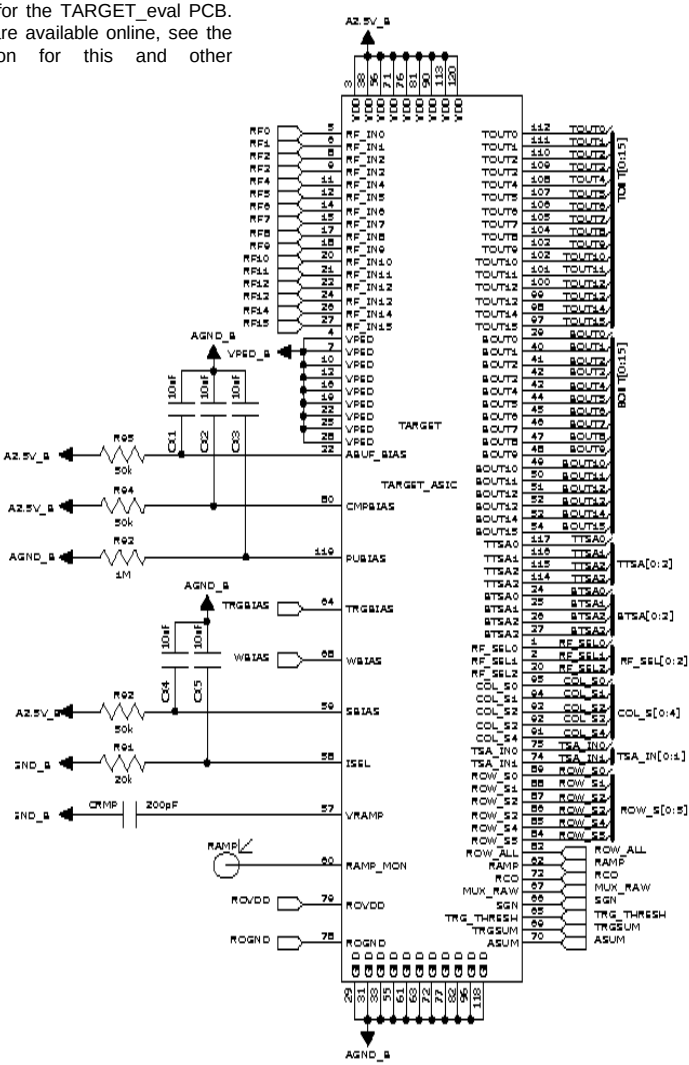
As seen in the figures above, a small amount of crosstalk is observed. However, given that these values are essentially at the noise floor, the absolute values should not be taken other than as indicative. Moreover, in these measurements, not effort has been made to determine the component due to direct inductive/capacitive coupling on the inputs, where the test configuration used is for the layout illustrated at the right.

Reference Design Implementation

Sample design and pin-out for the TARGET_eval PCB. A full set of PDF drawings are available online, see the **Online Resources** section for this and other documentation.

Example PMT connector interface

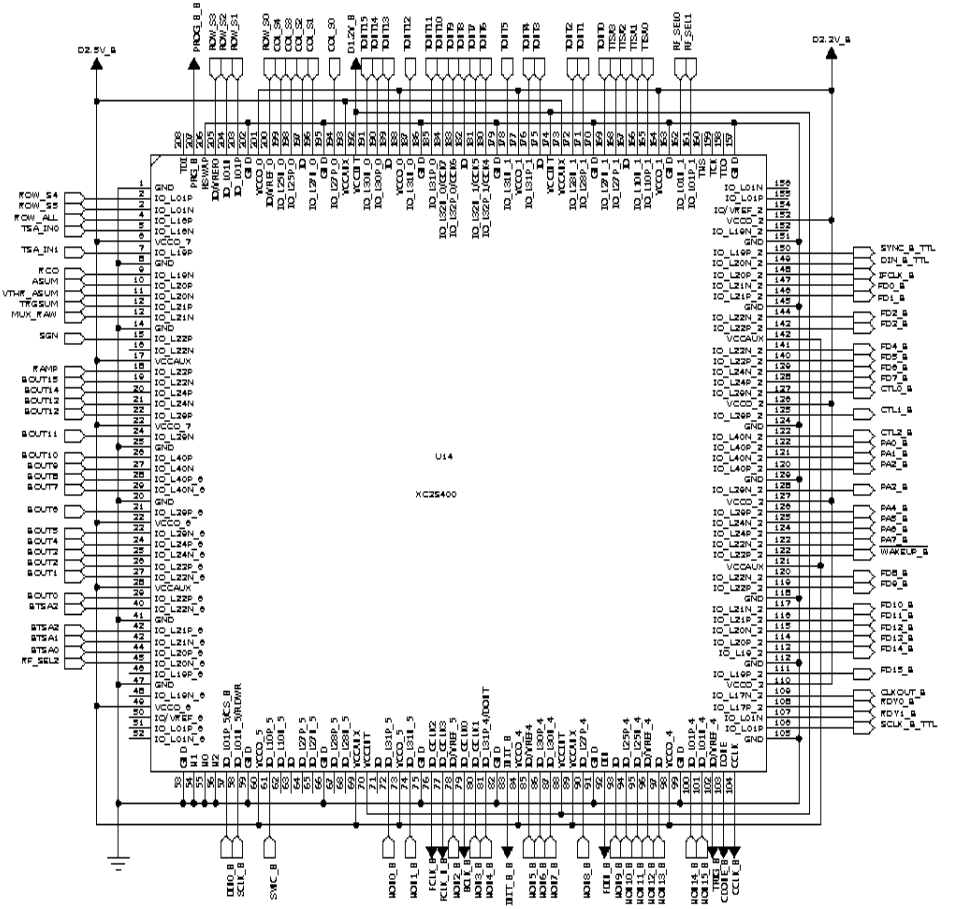




TARGET ASIC interconnects

FPGA Example

An example of the schematic for the FPGA implementation on the TARGET_eval board is included below.



Online Resources

TARGET_eval schematic: http://www.phys.hawaii.edu/~idlab/TARGET_eval_revC.pdf
TARGET_eval documentation: http://www.phys.hawaii.edu/~idlab/target-doc.pdf
TARGET_eval ISE firmware: http://www.phys.hawaii.edu/~idlab/TARGET_eval_revCv03.zip
TARGET_eval ISE firmware: http://www.phys.hawaii.edu/~idlab/TARGET_eval_software.zip

And likely a dedicated web page with information in the future.

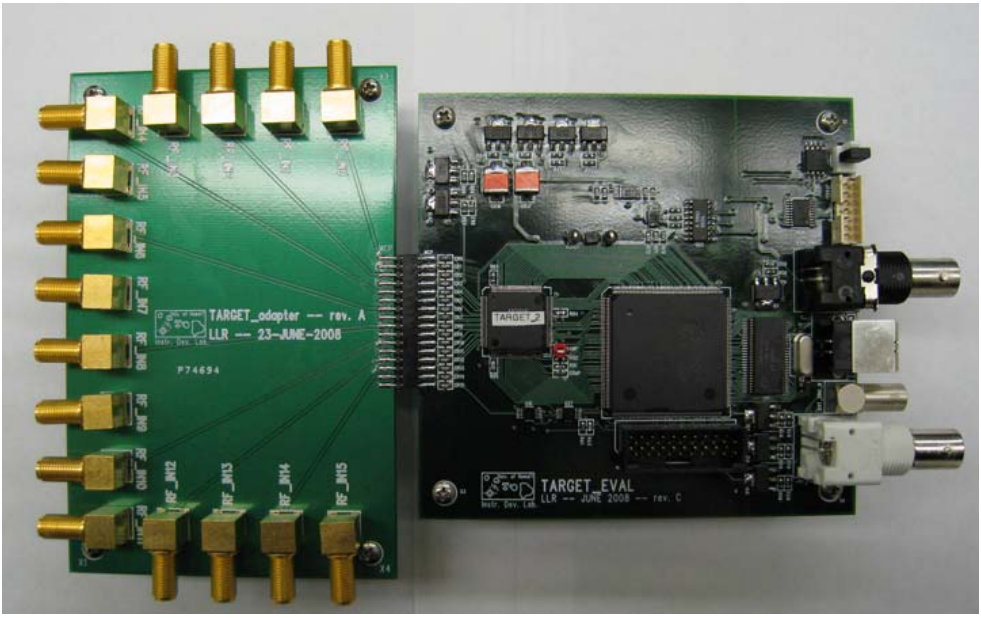
Required state machine

Sampling timing generation and readout requires at least one, or two state machines to perform the sequence of timing strobes and address selects to access the correct addresses with stored samples, convert those values to digital intervals and then broadcast the conversion samples to a data acquisition of some kind. A set of reference firmware for the initial TARGET_eval board may be found in the **Online Resources** section.

At right is the top-level symbol reflecting the logic needed to implement the requisite state machine. Further information on this logic functionality and required resources will be described in a companion Application Note.

TARGET Evaluation Board

In order to speed development and to gain experience with using the TARGET ASIC, an evaluation board has been fabricated, rudimentary firmware written and a USB-based software readout software tool suite developed. This acquisition program runs under Windows, Linux and Mac OS.



Packaging Mechanics

Mechanical drawing details are provided for the package used.

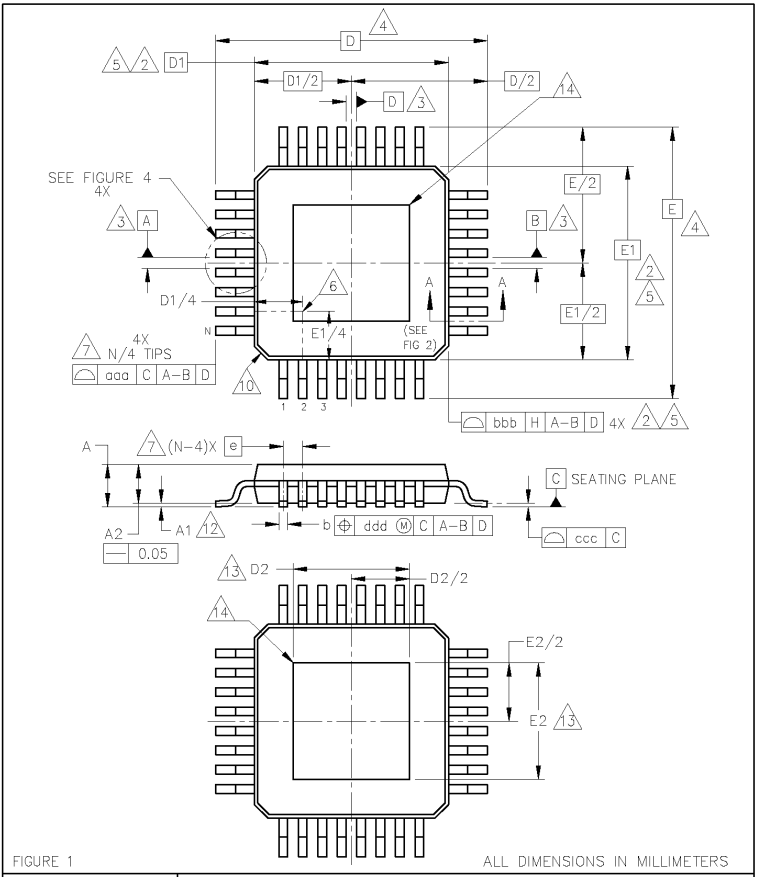
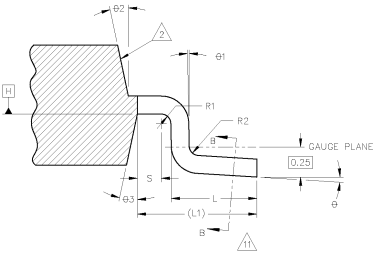
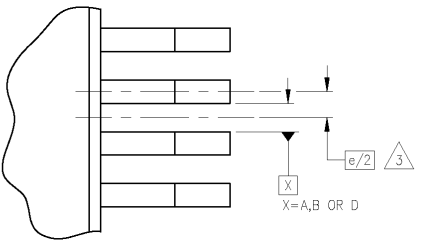


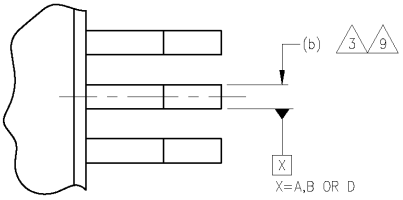
FIGURE 1 ALL DIMENSIONS IN MILLIMETERS





Package Details (cont'd).

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
θ	0°	3.5°	7°	
θ1	0°	–	–	
θ2	11°	12°	13°	
θ3	11°	12°	13°	
C	0.09	–	0.20	11
C1	0.09	–	0.16	11
D2	2.00	–	–	13
E2	2.00	–	–	13
L	0.45	0.60	0.75	
L1	1.00 REF			
R1	0.08	–	–	
R2	0.08	–	0.20	
S	0.20	–	–	
TOLERANCES OF FORM AND POSITION				
aaa	0.20			
bbb	0.20			
NOTE	1,8			
REF	11–411, 11–521S			
ISSUE	A, C			



14 X 14	1.00	52	AEA	AEA–HU / AEA–HD
14 X 14	0.80	64	AEB	AEB–HU / AEB–HD
14 X 14	0.65	80	AEC	AEC–HU / AEC–HD
14 X 14	0.50	100	AED	AED–HU / AED–HD
14 X 14	0.40	120	AEE	AEE–HU / AEE–HD

120-pin package relevant variation diagram is AEE.

SYMBOL	VARIATIONS											
	AEC SQUARE			NOTE	AED SQUARE			NOTE	AEE SQUARE			NOTE
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	–	–	1.20	14	–	–	1.20	14	–	–	1.20	14
A1	0.05		0.15	12	0.05	–	0.15	12	0.05	–	0.15	12
A2	0.95	1.00	1.05	14	0.95	1.00	1.05	14	0.95	1.00	1.05	14
b	0.22	0.32	0.38	9,11	0.17	0.22	0.27	9,11	0.13	0.18	0.23	9,11
b1	0.22	0.30	0.33	11	0.17	0.20	0.23	11	0.13	0.16	0.19	11
D	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
D1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
e	0.65 BSC				0.50 BSC				0.40 BSC			
E	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
E1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
N	80				100				120			
TOLERANCES OF FORM AND POSITION												
ccc	0.10				0.08				0.08			
ddd	0.13				0.08				0.07			
NOTE	1,8,15				1,8,15				1,8,15			
REF	11–411				11–411				11–411			
ISSUE	A				A				A			

Mechanical drawing details are provided for the leadframe used to package TARGET1.